National Semiconductor

May 2005

LM193JAN
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

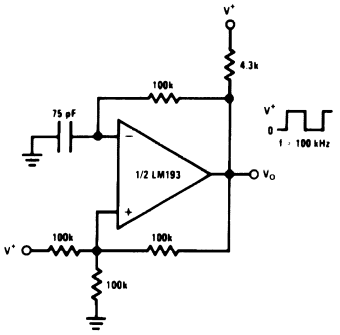
Features

- Wide supply
  - — Voltage range: $5.0V_{DC}$ to $36V_{DC}$
  - — Single or dual supplies: $\pm2.5V_{DC}$ to $\pm18V_{DC}$
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current: 25 nA typ
- Low input offset current: ±3 nA typ
- Maximum offset voltage +5mV Max @ 25˚C
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage,: 250 mV at 4 mA typ
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Ordering Information

NS Part Number	JAN Part Number	NS Package Number	Package Description
JL193BGA	JM38510/11202BGA	H08C	8LD T0-99 Metal Can
JL193BPA	JM38510/11202BPA	J08A	8LD CERDIP

Squarewave Oscillator



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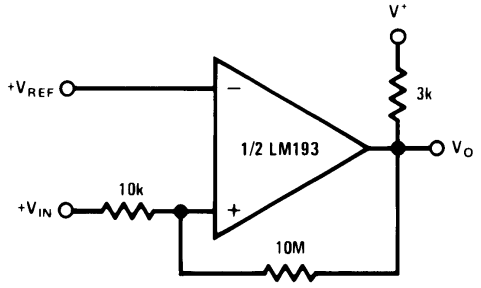
Non-Inverting Comparator with Hysteresis



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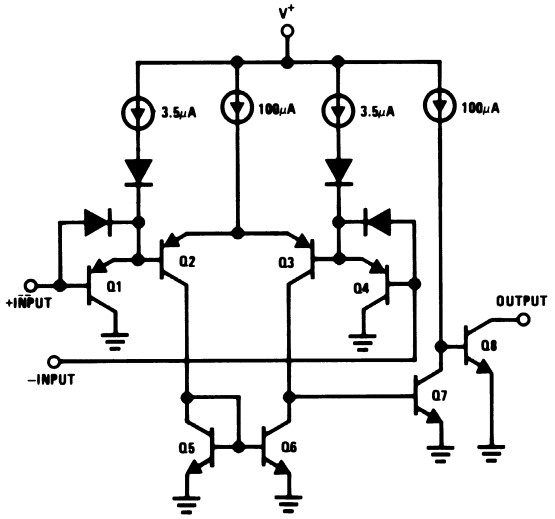
Schematic and Connection Diagrams



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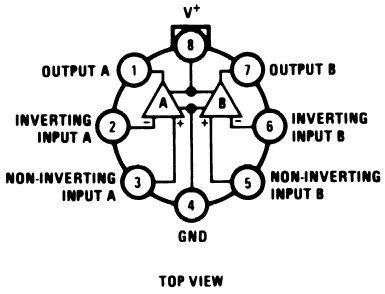
Metal Can Package



TOP VIEW

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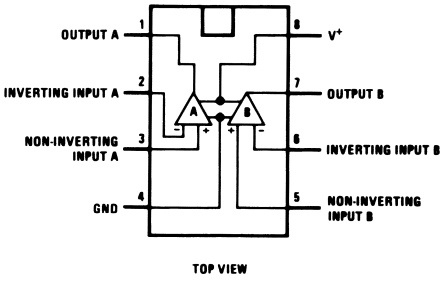
Dual-In-Line Package



TOP VIEW

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Absolute Maximum Ratings (Note 1)

Supply Voltage, V^+	$36V_{DC}$ or $\pm 18V_{DC}$
Differential Input Voltage (Note 5)	36V
Output Voltage	36V
Input Voltage	$-0.3V_{DC}$ to $+36V_{DC}$
Input Current ($V_{IN} < -0.3V_{DC}$) (Note 4)	50 mA
Power Dissipation (Note 2),	
CERDIP	400 mW @ $T_A = 125^\circ C$
Metal Can	330 mW @ $T_A = 125^\circ C$
Maximum Junction Temperature (T_{Jmax}	175˚C
Output Short-Circuit to Ground (Note 3)	Continuous
Operating Temperature Range	$-55^\circ C \le T_A \le +125^\circ C$
Storage Temperature Range	$-65^\circ C \le T_A \le +150^\circ C$
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air)	174˚C/W
Metal Can (500LF/Min Air flow)	99˚C/W
CERDIP (Still Air)	146˚C/W
CERDIP (500LF/Min Air flow)	85˚C/W
θ_{JC}	
Metal Can	44˚C/W
CERDIP	33˚C/W
Lead Temperature (Soldering, 10 seconds)	260˚C
ESD Tolerance (Note 6)	500V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM193 JAN Electrical Characteristics

DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
I_{IO}	Input offset Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V, R_S = 20KΩ	(Note 7)	-25	25	nA	1, 2
			(Note 7)	-75	75	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V, R_S = 20KΩ	(Note 7)	-25	25	nA	1, 2
			(Note 7)	-75	75	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V, R_S = 20KΩ	(Note 7)	-25	25	nA	1, 2
			(Note 7)	-75	75	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V, R_S = 20KΩ	(Note 7)	-25	25	nA	1, 2
			(Note 7)	-75	75	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V, R_S = 20KΩ	(Note 7)	-100	+0.1	nA	1, 2
			(Note 7)	-200	+0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V, R_S = 20KΩ	(Note 7)	-100	+0.1	nA	1, 2
			(Note 7)	-200	+0.1	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V, R_S = 20KΩ	(Note 7)	-100	+0.1	nA	1, 2
			(Note 7)	-200	+0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V, R_S = 20KΩ	(Note 7)	-100	+0.1	nA	1, 2
			(Note 7)	-200	+0.1	nA	3
CMRR	Input Voltage Common Mode Rejection	2V ≤ $+V_{CC}$ ≤ 30V, -28V ≤ $-V_{CC}$ ≤ 0V, -13V ≤ V_O ≤ 15V		76		dB	1, 2, 3
		2V ≤ $+V_{CC}$ ≤ 5V, -3V ≤ $-V_{CC}$ ≤ 0V, -1.6V ≤ V_O ≤ 1.4V		70		dB	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = +30V			1.0	µA	1, 2, 3
$+I_{IL}$	Input Leakage Current	$+V_{CC}$ = 36V, $-V_{CC}$ = 0V, $+V_I$ = 34V, $-V_I$ = 0V		-500	500	nA	1, 2, 3
$-I_{IL}$	Input Leakage Current	$+V_{CC}$ = 36V, $-V_{CC}$ = 0V, $+V_I$ = 0V, $-V_I$ = 34V		-500	500	nA	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = 0V, I_O = 4mA			0.4	V	1
					0.7	V	2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = 0V, I_O = 8mA			1.5	V	1
					2.0	V	2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{ID} = 15mV			2.0	mA	1, 2
					3.0	mA	3
		$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_{ID} = 15mV			3.0	mA	1, 2
					4.0	mA	3
Δ_{IO} / ΔT	Temperature Coefficient of Input Offset Voltage	25˚C ≤ T_A ≤ +125˚C	(Note 9)	-25	25	µV/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 9)	-25	25	µV/˚C	3

LM193 JAN Electrical Characteristics (Continued)

DC Parameters (Continued)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$\Delta I_{IO} / \Delta T$	Temperature Coefficient of Input Offset Current	25˚C ≤ T_A ≤ +125˚C	(Note 9)	-300	300	pA/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 9)	-400	400	pA/˚C	3
A_{VS}	Open Loop Voltage Gain	$+V_{CC}$ = 15V, $-V_{CC}$ = 0V, R_L = 15KΩ,	(Note 8)	50		V/mV	4
		1V ≤ V_O ≤ 11V	(Note 8)	25		V/mV	5, 6
V_{Lat}	Voltage Latch (Logical "1" Input)	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_I = 10V, I_O = 4mA			0.4	V	9

AC Parameters

The following conditions apply, unless otherwise specified. $+V_{CC}$ = 5V, $-V_{CC}$ = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 5mV			5.0	µS	7, 8B
					7.0	µS	8A
		V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 50mV			0.8	µS	7, 8B
					1.2	µS	8A
t_{RHL}	Response Time	V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 5mV			2.5	µS	7, 8B
					3.0	µS	8A
		V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 50mV			0.8	µS	7, 8B
					1.0	µS	8A
CS	Channel Separation	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, A to B		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, B to A		80		dB	7

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

Note 5: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

Note 6: Human body model, 1.5KΩ in series with 100pF.

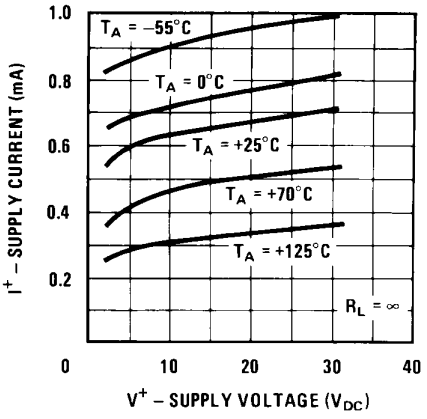
Note 7: S/S R_S = 20KΩ, tested with R_S = 100KΩ for better resolution

Note 8: K in datalog is equivalent to V/mV.

Note 9: Calculated parameter for $\Delta V_{IO} / \Delta T$ and $\Delta I_{IO} / \Delta T$.

Typical Performance Characteristics

Supply Current



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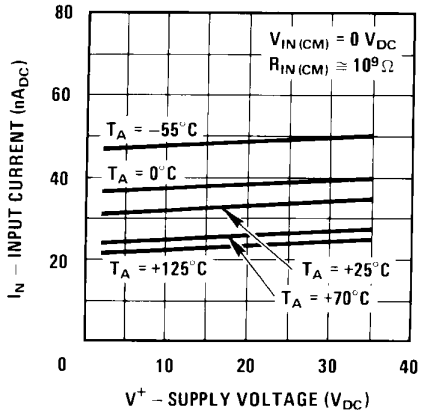
Input Current



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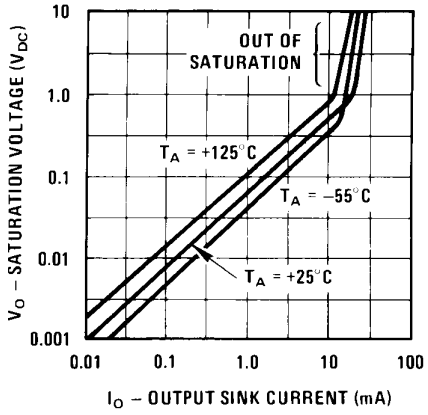
Output Saturation Voltage



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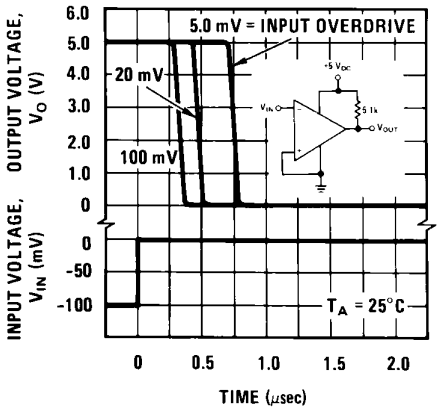
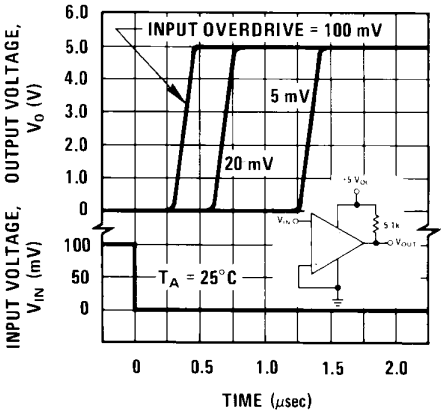
Response Time for Various Input Overdrives — Negative Transition



20143228

Response Time for Various Input Overdrives — Positive Transition



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Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

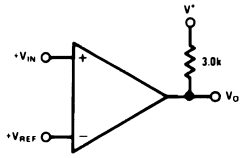
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (Note 5). Protection should be provided to prevent the input voltages from going negative more than –0.3 V_{DC} (at 25˚C). An input clamp diode can be used as shown in the applications section.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V^+=5.0 V_{DC})

Basic Comparator



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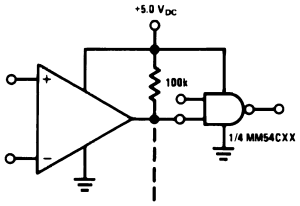
Driving CMOS



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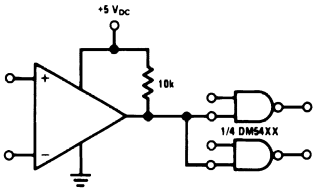
Driving TTL



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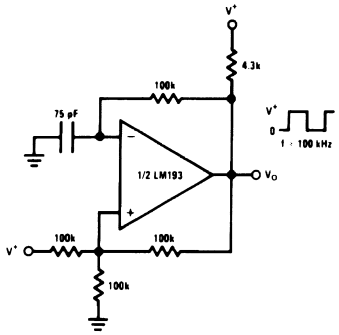
Squarewave Oscillator



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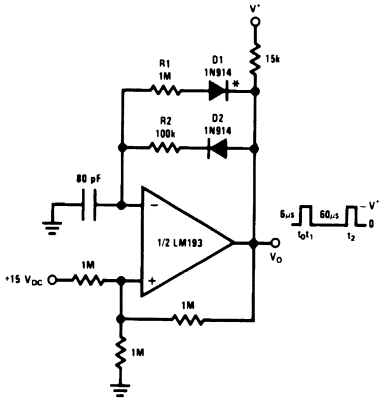
Pulse Generator



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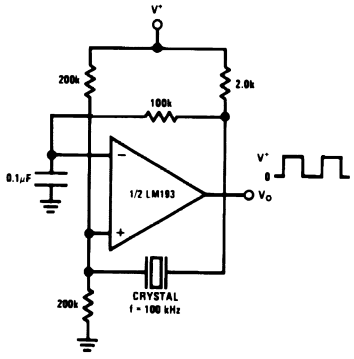
Crystal Controlled Oscillator



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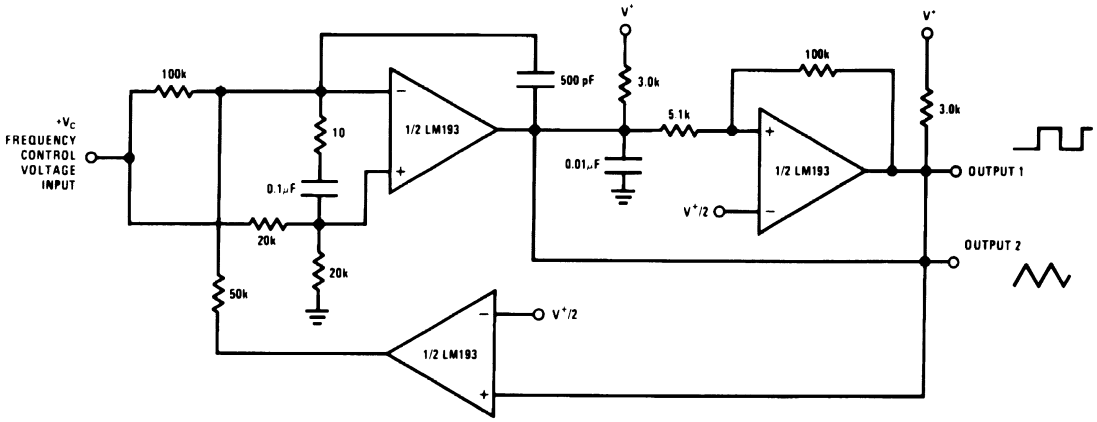
* For large ratios of R1/R2, D1 can be omitted.

Typical Applications (V^+=5.0 V_{DC}) (Continued)

Two-Decade High Frequency VCO



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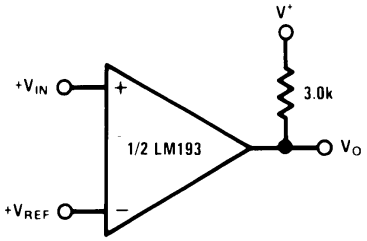
V^* = +30 V_{DC}
+250 $mV_{DC} \le V_C \le$ +50 V_{DC}
700Hz $\le f_o \le$ 100kHz

Basic Comparator



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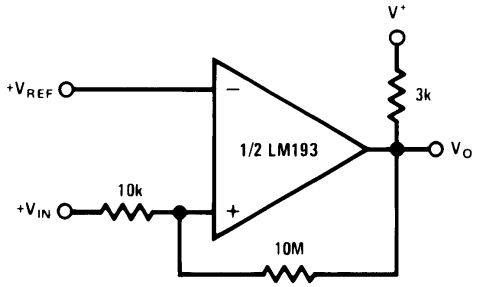
Non-Inverting Comparator with Hysteresis



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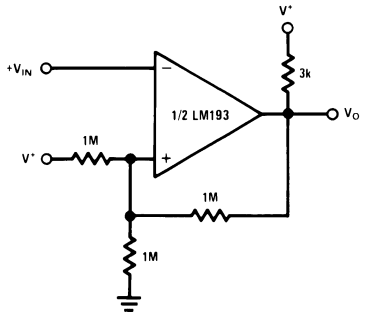
Inverting Comparator with Hysteresis



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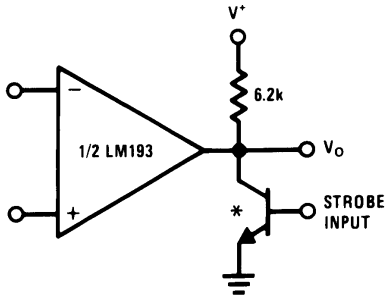
Output Strobing



* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

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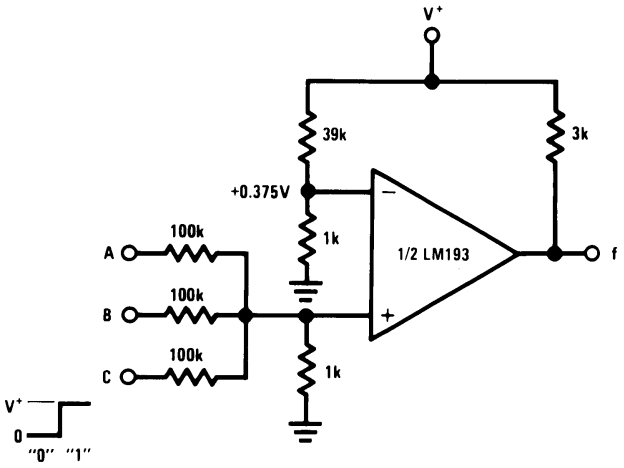
Typical Applications (V^+=5.0 V_{DC}) (Continued)

AND Gate



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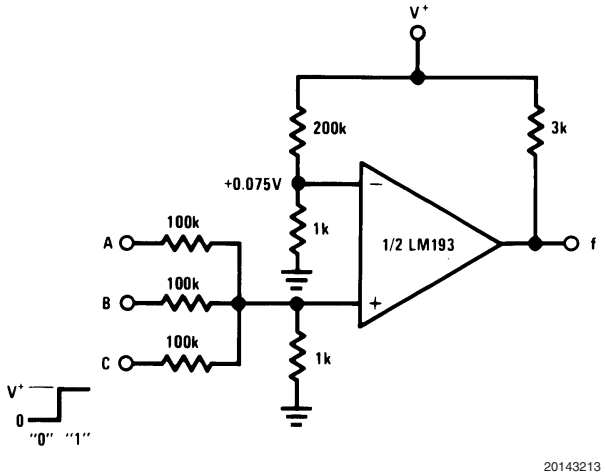
OR Gate



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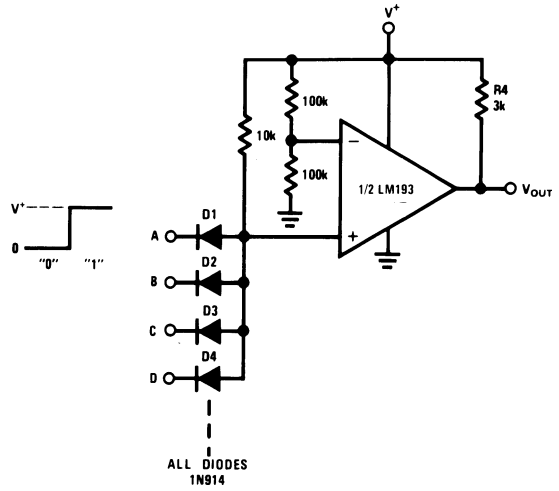
Large Fan-in AND Gate



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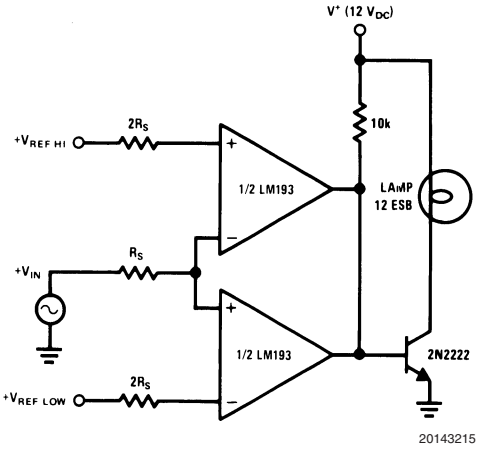
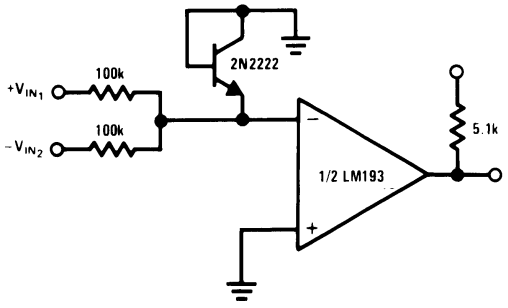
Limit Comparator



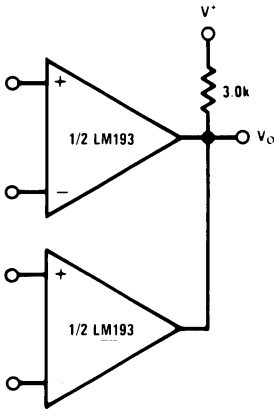
20143215

Comparing Input Voltages of Opposite Polarity



20143216

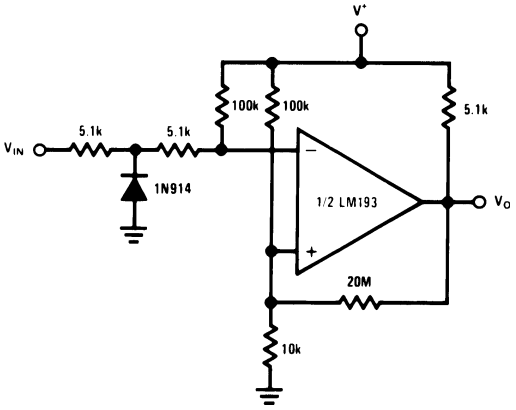
ORing the Outputs



20143217

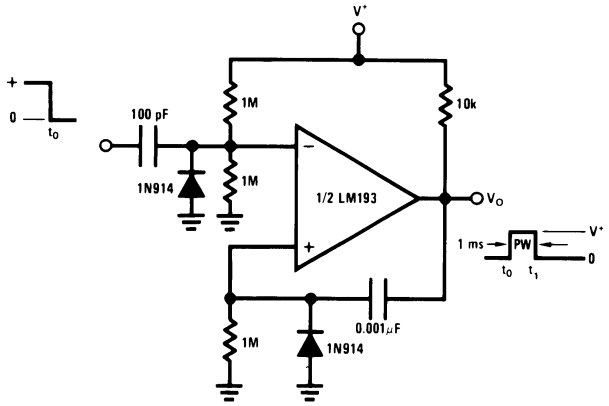
Typical Applications (V^+=5.0 V_{DC}) (Continued)

Zero Crossing Detector (Single Power Supply)



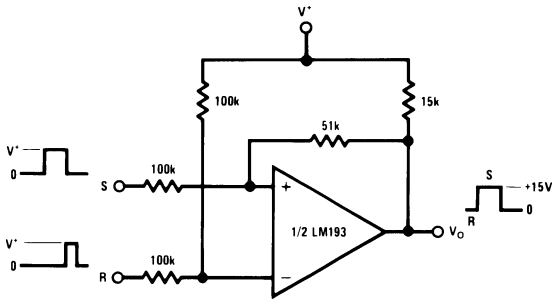
20143221

One-Shot Multivibrator



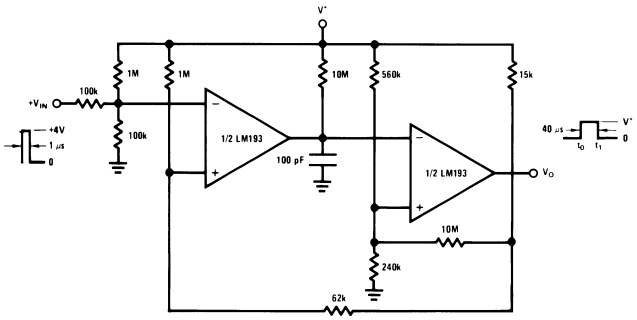
20143222

Bi-Stable Multivibrator



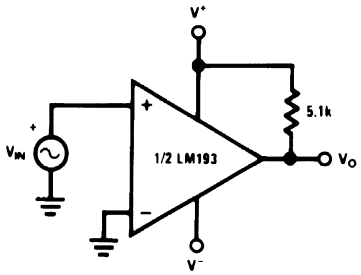
20143224

One-Shot Multivibrator with Input Lock Out



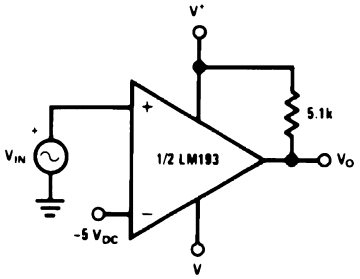
20143223

Zero Crossing Detector



20143243

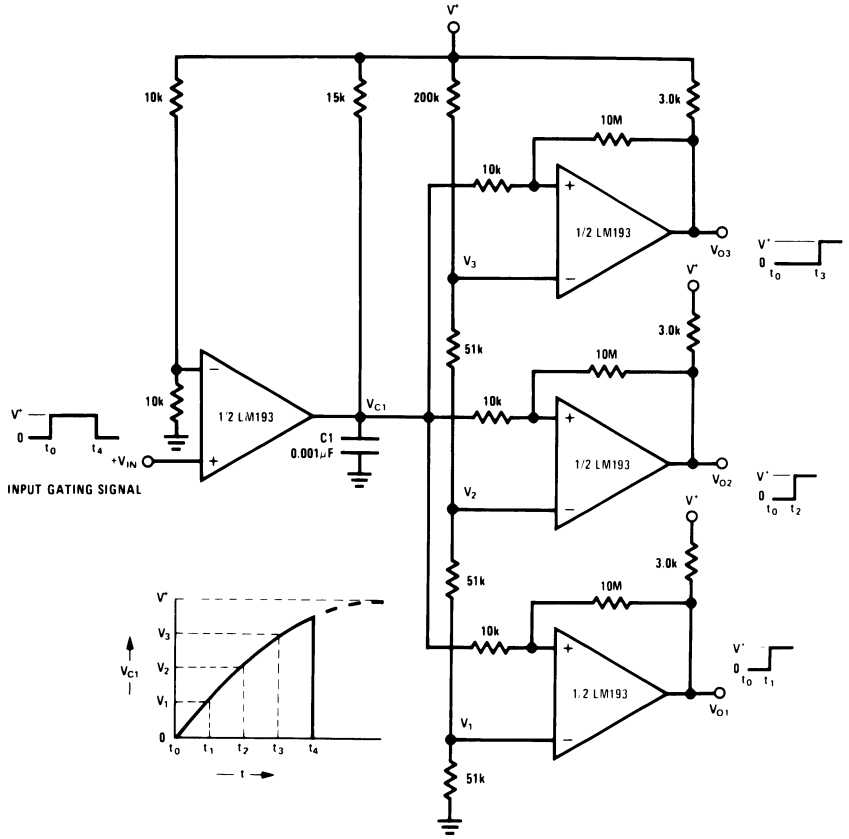
Comparator With a Negative Reference



20143244

Typical Applications (V^+=5.0 V_{DC}) (Continued)

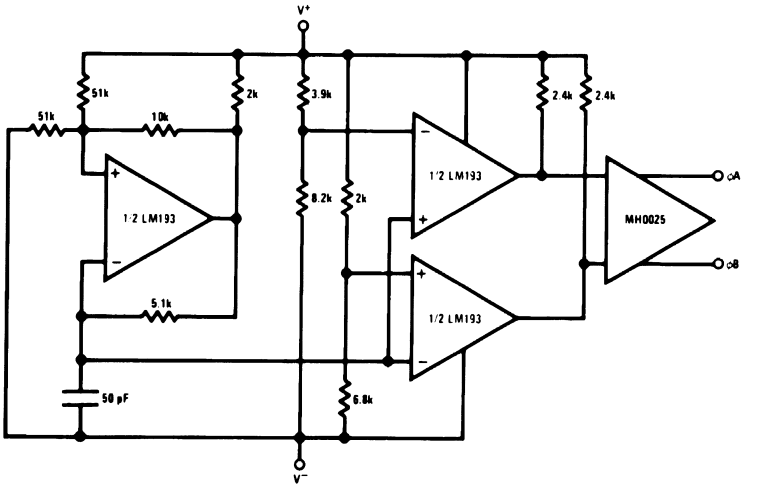
Time Delay Generator



20143207

Split-Supply Applications (V^+=+15 V_{DC} and V^-=–15 V_{DC})

MOS Clock Driver

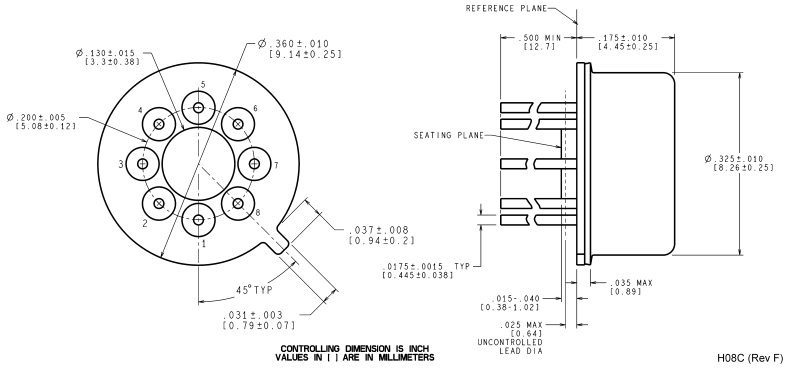


20143242

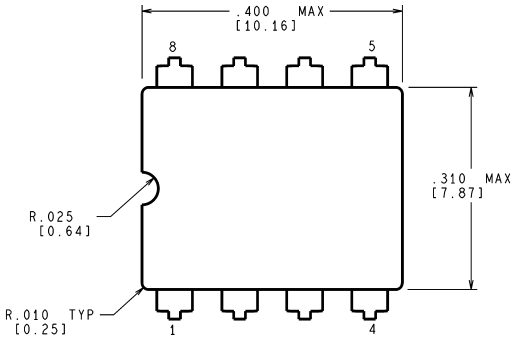
Revision History Section

Date Released	Revision	Section	Originator	Changes
05/09/05	A	New Release. Corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. DC Drift table was deleted due to no JANS product offerings. MJLM193-X Rev 1A1 MDS will be archived.

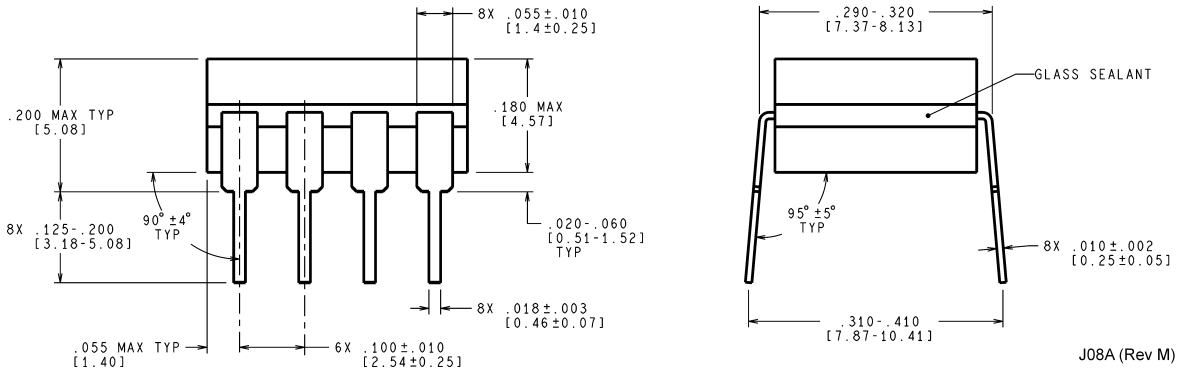
Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS



Ceramic Dual-In-Line Package
NS Package Number J08A

Notes

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