

MOS FIELD EFFECT TRANSISTOR NP100P06PLG

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The NP100P06PLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

<R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP100P06PLG-E1-AY ^{Note}	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)
NP100P06PLG-E2-AY ^{Note}			

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

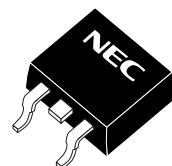
- Super low on-state resistance

$R_{DS(on)1} = 6.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -50 \text{ A)}$

$R_{DS(on)2} = 7.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -50 \text{ A)}$

- High current rating: $I_{D(DC)} = \mp 100 \text{ A}$
- Built-in gate protection diode

(TO-263)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 100	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 300	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	200	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	64	A
Single Avalanche Energy ^{Note2}	E_{AS}	420	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = -20 \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.75	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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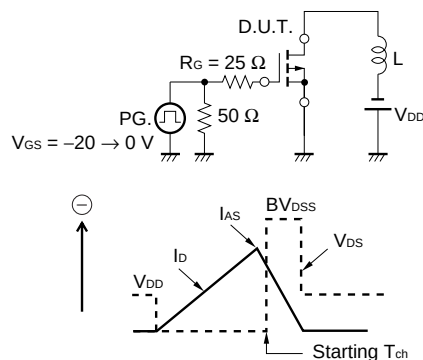
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

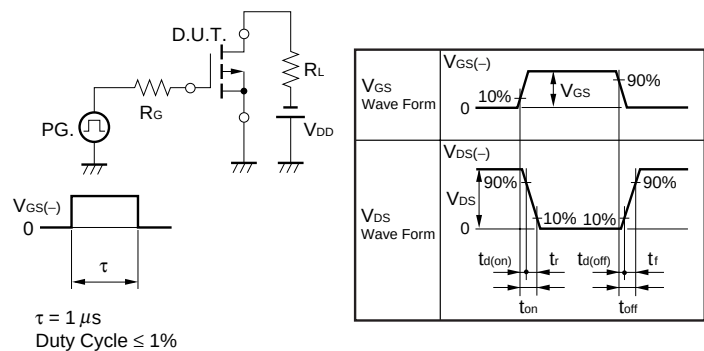
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = -10 V, I _D = -50 A	43	86		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = -10 V, I _D = -50 A		4.4	6.0	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -50 A		5.0	7.8	mΩ
Input Capacitance	C _{iss}	V _{DS} = -10 V,		15000		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		1810		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		840		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -30 V, I _D = -50 A,		28		ns
Rise Time	t _r	V _{GS} = -10 V,		35		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		275		ns
Fall Time	t _f			100		ns
Total Gate Charge	Q _G	V _{DD} = -48 V,		300		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V,		35		nC
Gate to Drain Charge	Q _{GD}	I _D = -100 A		85		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = -100 A, V _{GS} = 0 V		0.92	1.5	V
Reverse Recovery Time	t _{rr}	I _F = -100 A, V _{GS} = 0 V,		70		ns
Reverse Recovery Charge	Q _{rr}	di/dt = -100 A/μs		135		nC

Note Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

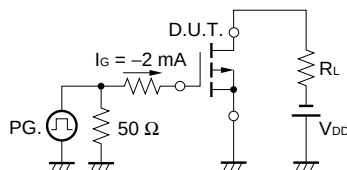
TEST CIRCUIT 1 AVALANCHE CAPABILITY



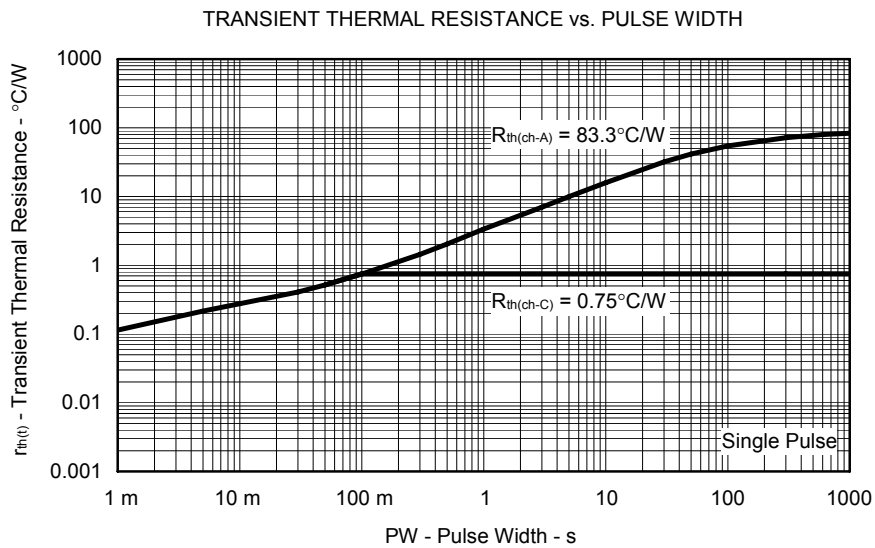
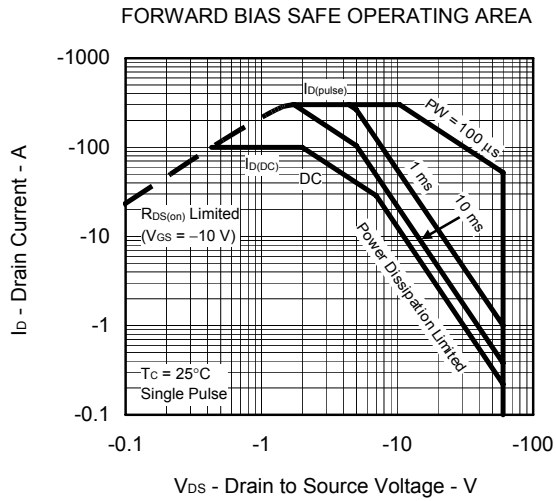
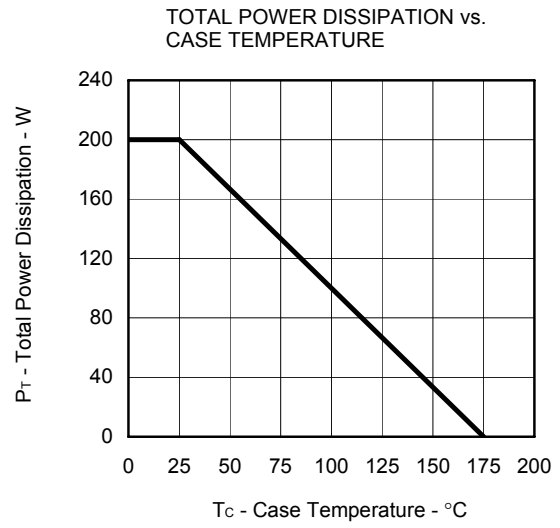
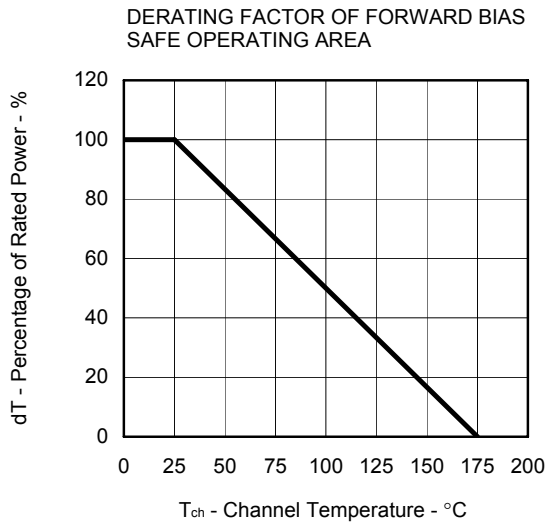
TEST CIRCUIT 2 SWITCHING TIME



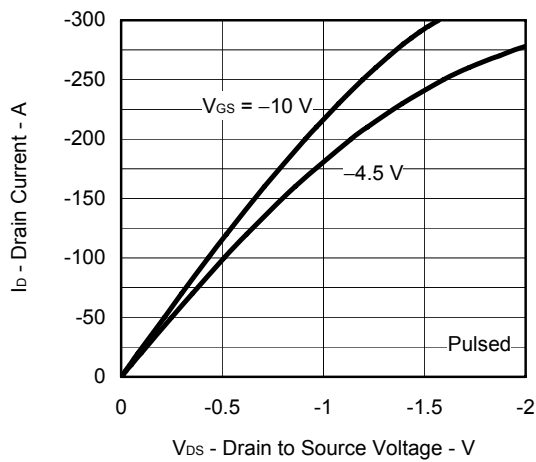
TEST CIRCUIT 3 GATE CHARGE



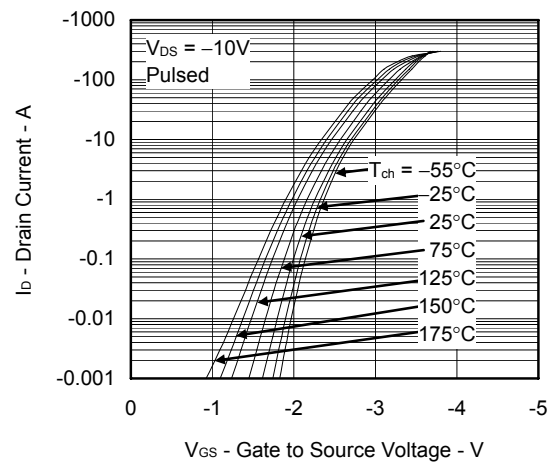
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



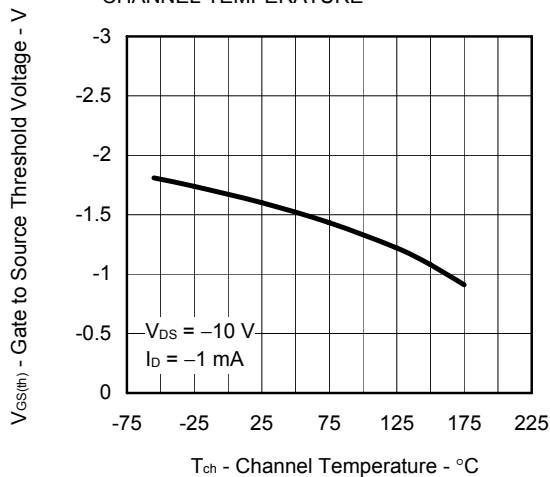
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



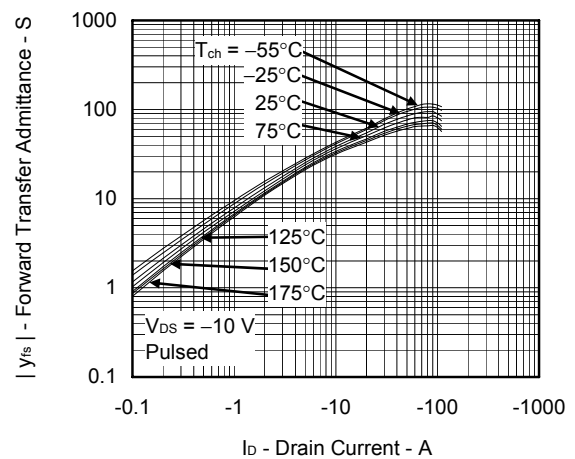
FORWARD TRANSFER CHARACTERISTICS



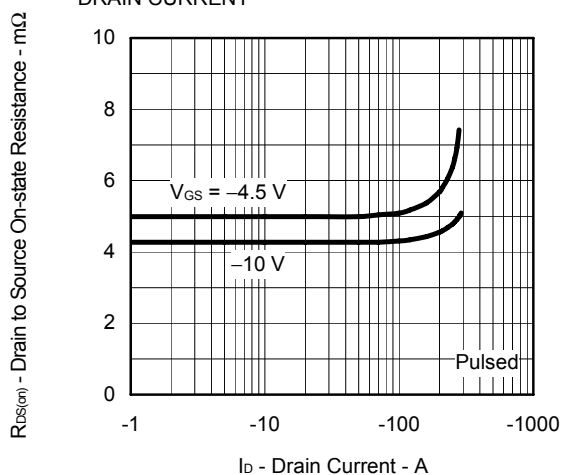
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



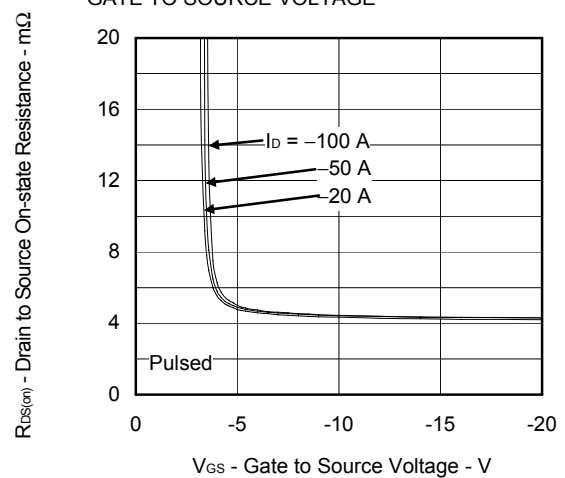
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT

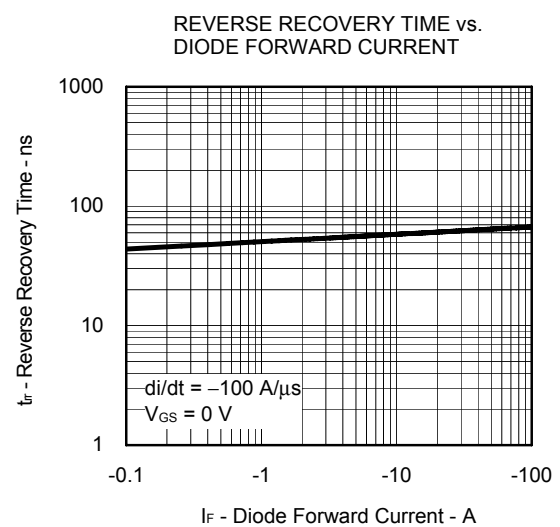
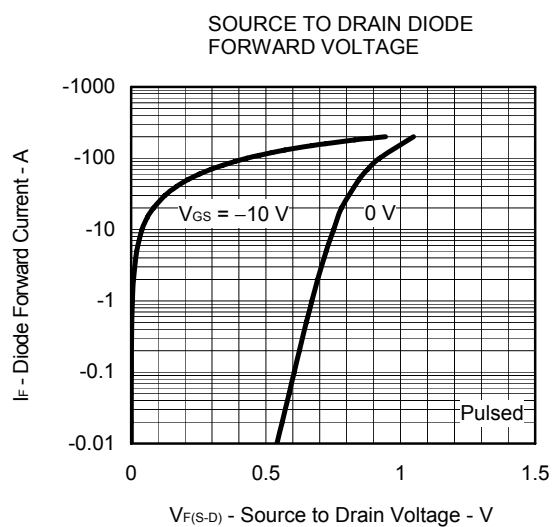
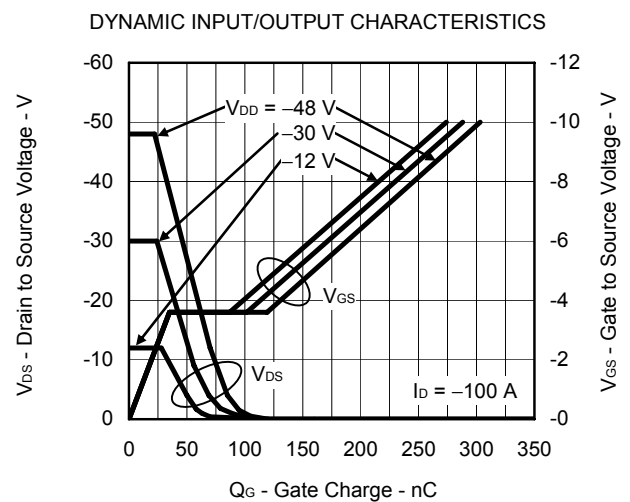
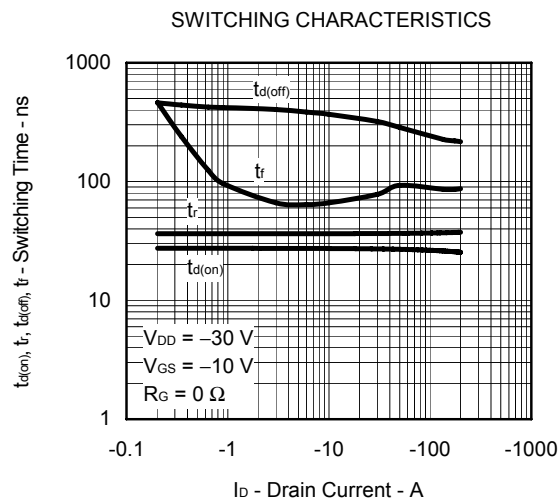
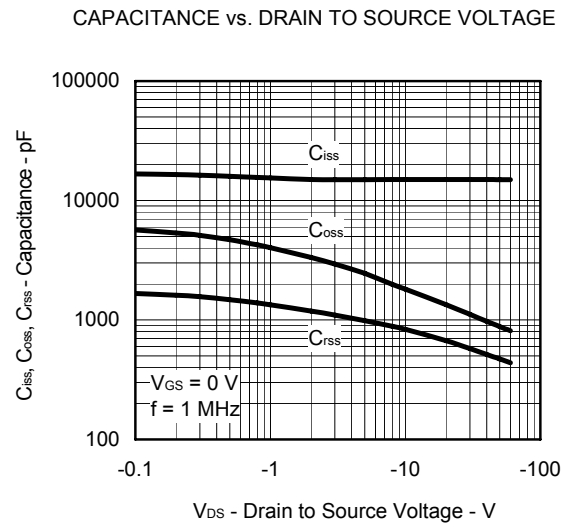
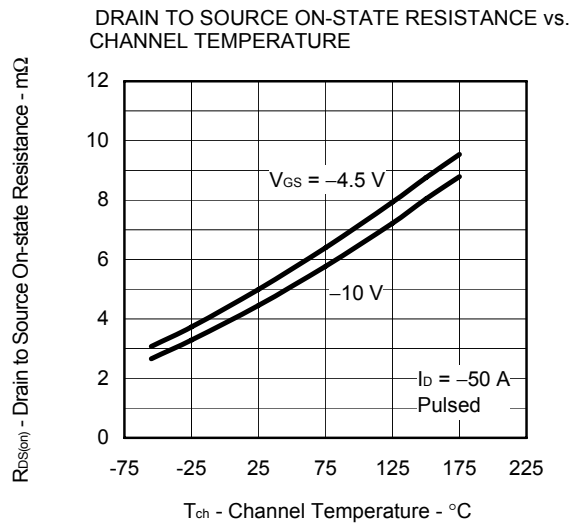


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



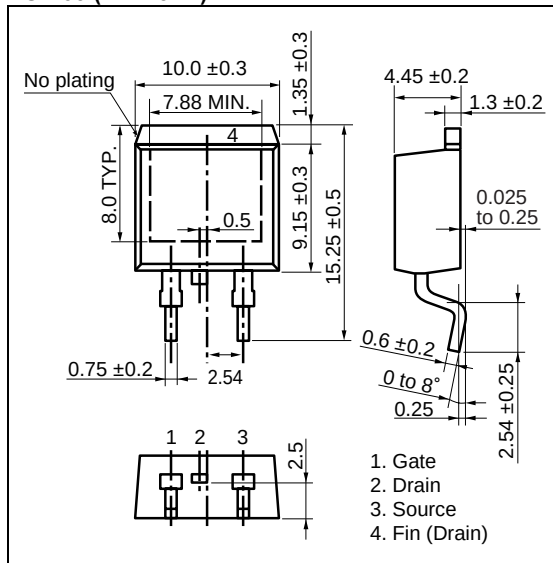
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



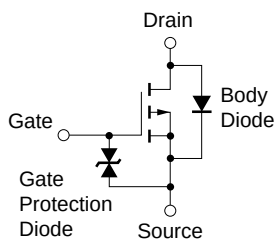


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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