

Document Title**4Mx16 bit Page Mode Uni-Transistor Random Access Memory****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft - Design Target	November 3, 2004	Preliminary
1.0	Finalize	April 06, 2005	Final

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4M x 16 bit Page Mode Uni-Transistor CMOS RAM**FEATURES**

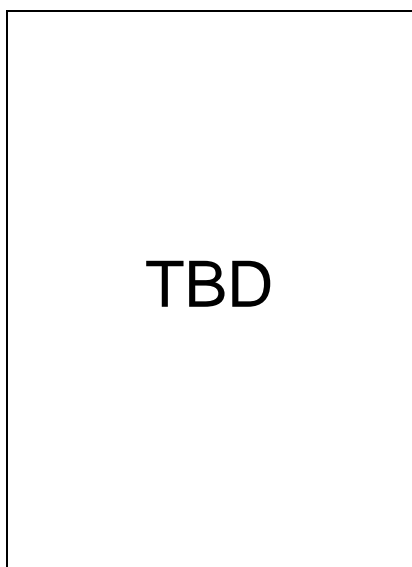
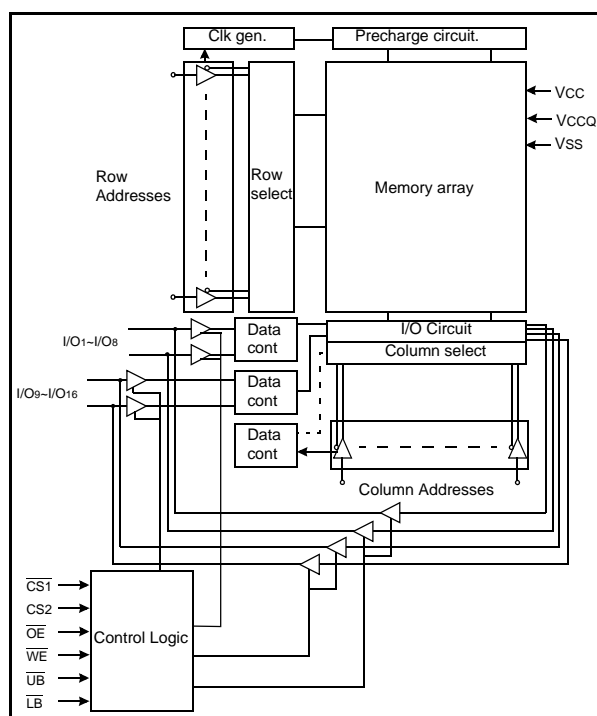
- Process Technology: CMOS
- Organization: 4M x16 bit
- Power Supply Voltage: 1.7~2.0V
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page read mode
- Package Type: TBD

GENERAL DESCRIPTION

The K1S6416BCC is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device supports dual chip selection for user interface. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (trc)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max.)	Operating (I _{CC2} , Max.)	
K1S6416BCC-I	Industrial(-40~85°C)	1.7~2.0V	70ns	120 μ A(< 40°C)	40mA	TBD
				180 μ A(< 85°C)		

PIN DESCRIPTION**FUNCTIONAL BLOCK DIAGRAM**

Name	Function	Name	Function
$\overline{CS1}, CS2$	Chip Select Inputs	Vcc/Vccq ²⁾	Power Supply(core / I/O)
\overline{OE}	Output Enable Input	Vss	Ground
\overline{WE}	Write Enable Input	\overline{UB}	Upper Byte(I/O _{9~16})
A _{0~A21}	Address Inputs	\overline{LB}	Lower Byte(I/O _{1~8})
I/O _{1~I/O16}	Data Inputs/Outputs	NC	No Connection ¹⁾

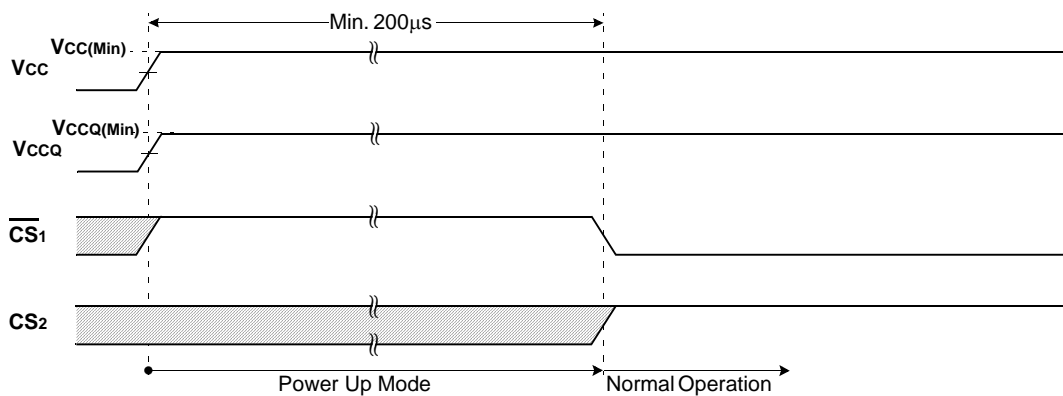
1) Reserved for future use

2) Vcc and Vccq should be the same level

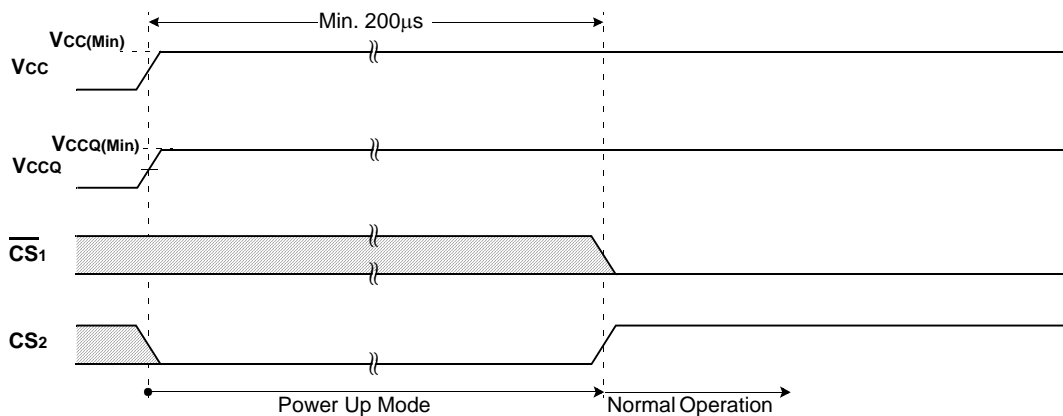
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POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power (V_{CC} min. and V_{CCQ} min.=1.7V) for a minimum 200 μ s with $\overline{CS1}$ =high.or $CS2$ =low.

TIMING WAVEFORM OF POWER UP(1) ($\overline{CS1}$ controlled)**POWER UP(1)**

1. After V_{CC} reaches $V_{CC}(\text{Min.})$ and $V_{CCQ}(\text{Min.})$, wait 200 μ s with $\overline{CS1}$ high. Then the device gets into the normal operation.

TIMING WAVEFORM OF POWER UP(2) ($CS2$ controlled)**POWER UP(2)**

1. After V_{CC} reaches $V_{CC}(\text{Min.})$ and $V_{CCQ}(\text{Min.})$, wait 200 μ s with $CS2$ low. Then the device gets into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS1}}$	CS2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CCQ} +0.3V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

PRODUCT LIST

Industrial Temperature Product(-40~85°C)	
Part Name	Function
K1S6416BCC	70ns, 1.85V

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	1.7	1.85	2.0	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	0.8 x V _{CCQ}	-	V _{CCQ} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.

2. Overshoot: V_{CCQ}+1.0V in case of pulse width ≤20ns.

3. Undershoot: -1.0V in case of pulse width ≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

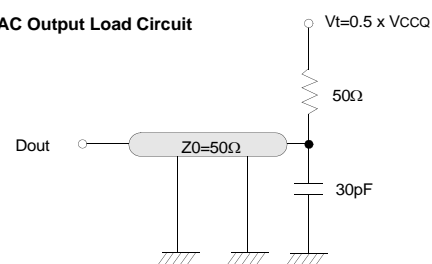
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CCQ}		-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CCQ}		-1	-	1	μA
Average operating current	I _{CC2}	Cycle time=t _{RC} +3t _{PC} , I _{IO} =0mA, 100% duty, $\overline{CS1}=V_{IL}$, $CS2=V_{IH}$, $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}		-	-	40	mA
Output low voltage	V _{OL}	I _{OL} =0.1mA		-	-	0.2	V
Output high voltage	V _{OH}	I _{OH} =-0.1mA		1.4	-	-	V
Standby Current(CMOS)	I _{SB1} ¹⁾	Other inputs=0~V _{CCQ} 1) $\overline{CS1} \geq V_{CCQ}-0.2V$, $CS2 \geq V_{CCQ}-0.2V$ ($\overline{CS1}$ controlled) or 2) $0V \leq CS2 \leq 0.2V$ (CS2 controlled)	< 40°C	-	-	120	μA
			< 85°C	-	-	180	μA

1. Standby mode is supposed to be set up after at least one active operation.after power up.

I_{SB1} is measured after 60ms from the time when standby mode is set up.

AC OPERATING CONDITIONS**TEST CONDITIONS**(Test Load and Test Input/Output Reference)Input pulse level: 0.2 to V_{CCQ}-0.2V

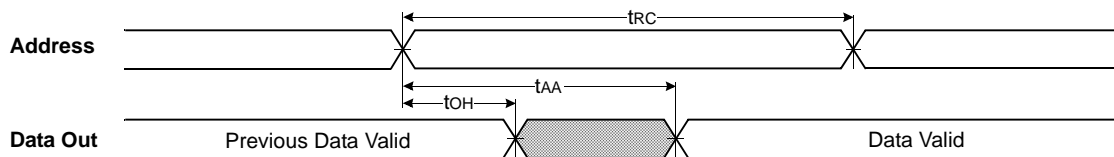
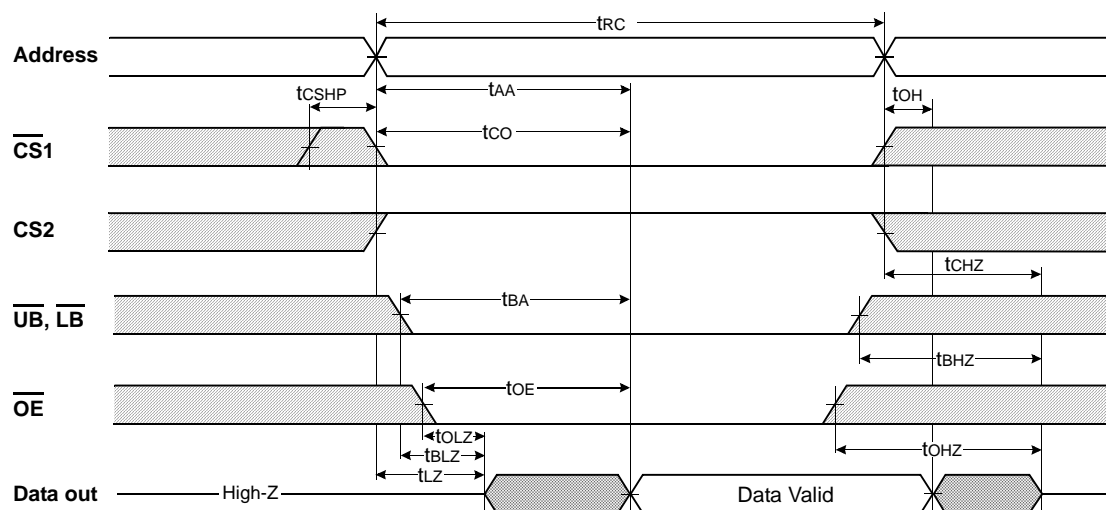
Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V_{CCQ}Output load (See right): C_L=30pF**AC Output Load Circuit****AC CHARACTERISTICS** (V_{CC}=V_{CCQ}=1.7~2.0V, T_A=-40 to 85°C)

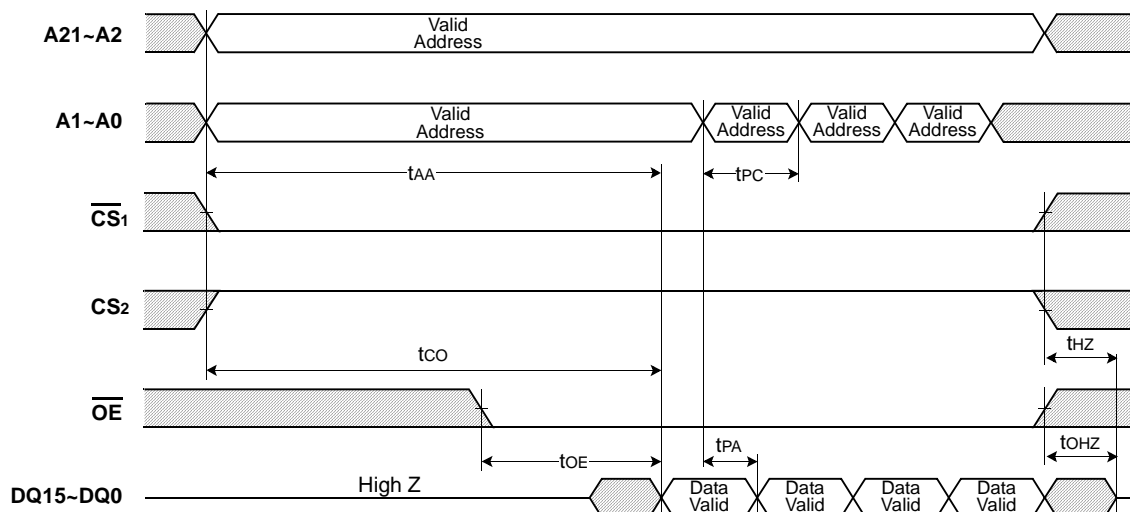
Parameter List		Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Common	$\overline{\text{CS}}$ High Pulse Width	tCSHP	10	-	ns
Read	Address Access Time	tAA	-	70	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	tBA	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	25	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	tBHZ	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	25	ns
	Output Hold from Address Change	tOH	3	-	ns
	Page Cycle	tPC	25	-	ns
	Page Access Time	tPA	-	20	ns
Write	Write Cycle Time	tWC	70	-	ns
	Chip Select to End of Write	tCW	60	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	55 ¹⁾	-	ns
	$\overline{\text{WE}}$ High Pulse Width	tWHP	5	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	25	ns
	Data to Write Time Overlap	tdW	30	-	ns
	Data Hold from Write Time	tdH	0	-	ns
	End Write to Output Low-Z	tOW	5	-	ns

1. t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

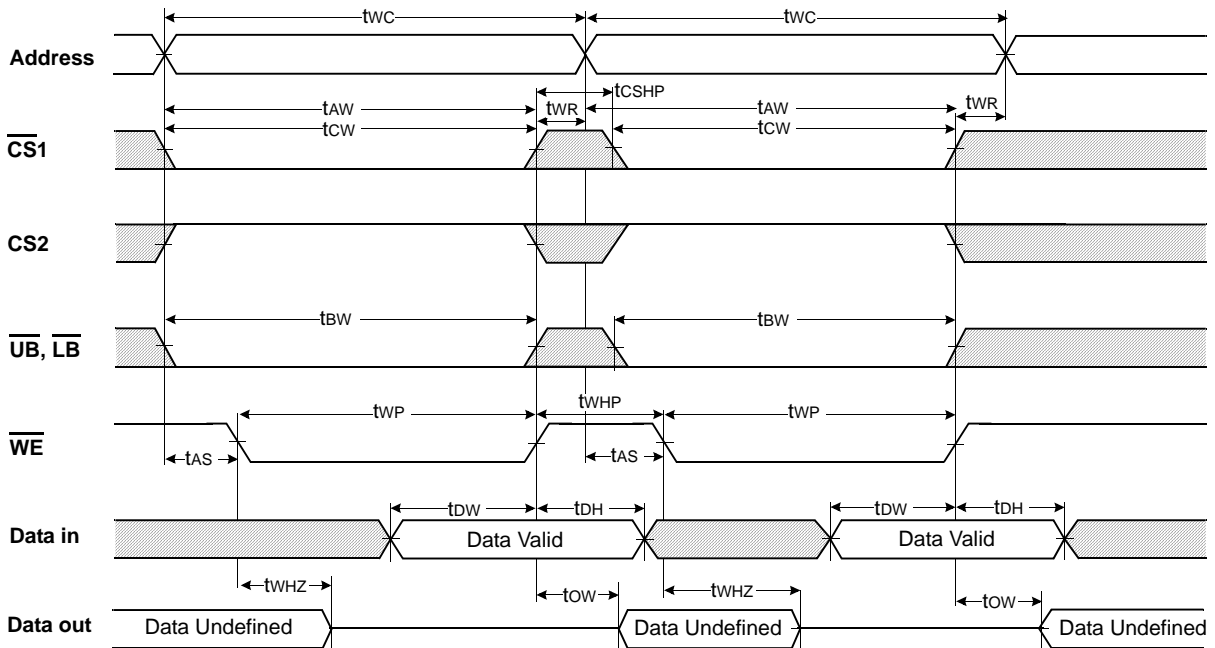
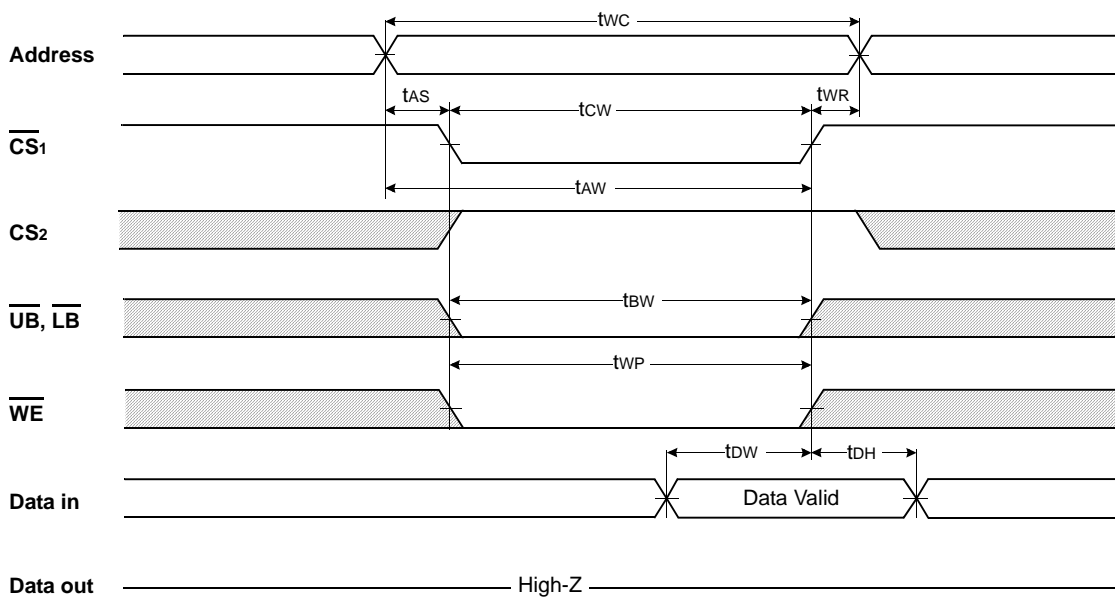
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)TIMING WAVEFORM OF READ CYCLE(2)($\overline{WE}=V_{IH}$)

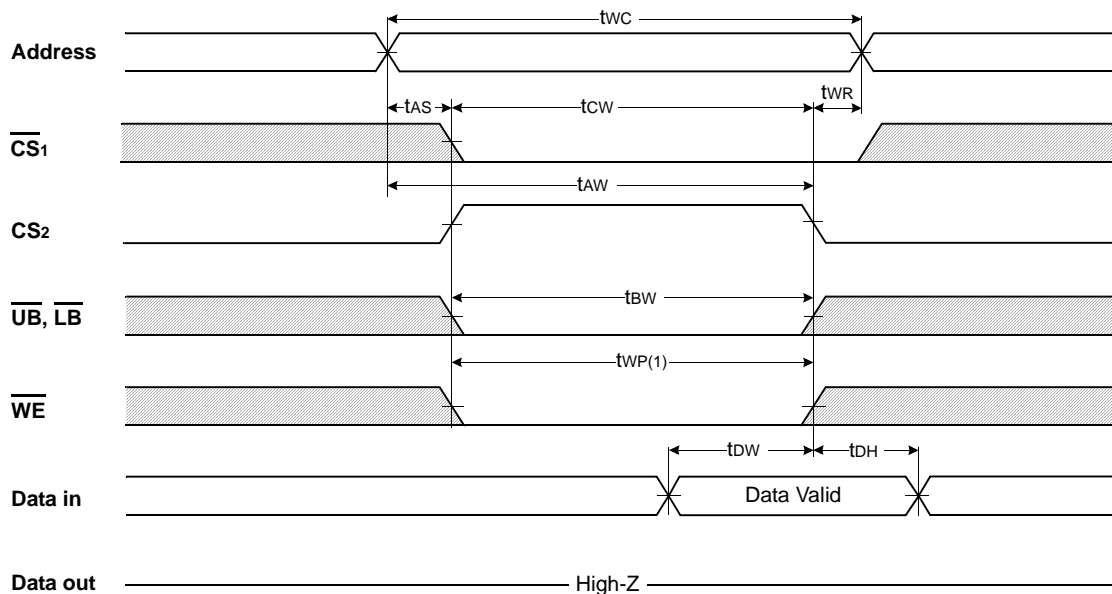
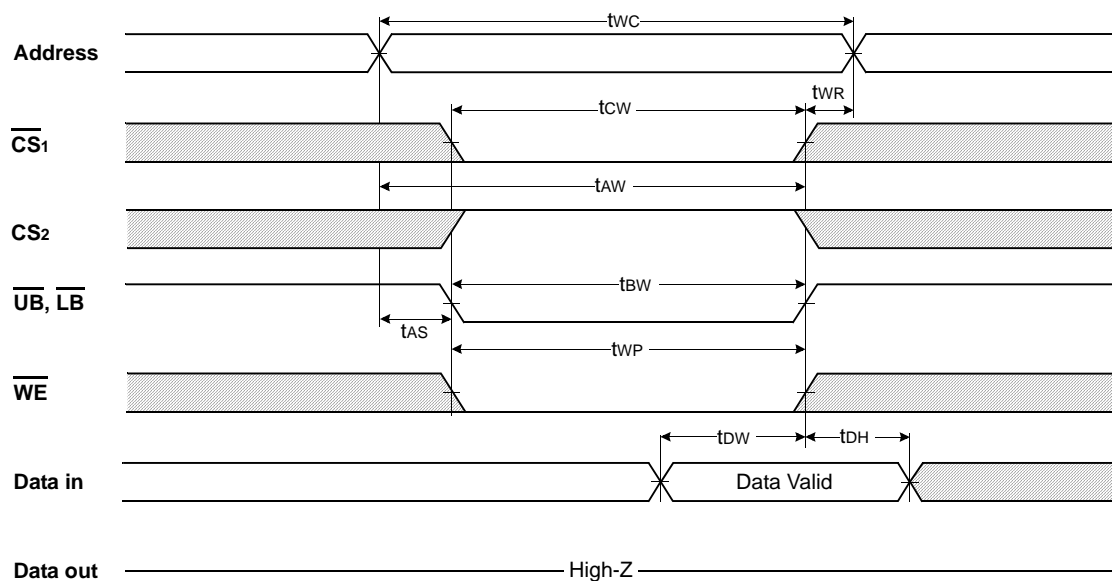
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. $t_{OE}(\text{max})$ is met only when \overline{OE} becomes enabled after $t_{AA}(\text{max})$.
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4 μ s, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4 μ s.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)

TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)TIMING WAVEFORM OF WRITE CYCLE(4) (\overline{UB} , \overline{LB} Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$ and low \overline{WE} . A write begins when $\overline{CS_1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS_1}$ or \overline{WE} going high.

PACKAGE DIMENSION

TBD