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KB3302

2Amp, 2MHz Step-up Switching regulator with Soft-Start

FEATURES

- Up to 95% Efficiency
- TDB uA No Load Current
- 1000mA Output Current
- 1.5V to 16V Input Voltage Range
- Programmable switching frequency up to 2MHz
- Output voltage up to 32V
- Constant switching frequency current-mode control
- 1.23V Reference Allows Low Output Voltages
- Shutdown Mode Draws ≤ 10 μA Supply Current
- Low saturation voltage switch: 220mV at 2A
- Overtemperature Protected,Soft-Start function
- 8-Pin MSOP Packages

DESCRIPTION

The KB3302 is a high-frequency current-mode step-up switching regulator with an integrated 2A power transistor. Its high switching frequency (programmable up to 2MHz) allows the use of tiny surface-mount external passive components. Programmable soft-start eliminates high inrush current during start-up. The internal switch is rated at 32V making the converter suitable for high voltage applications such as Boost, SEPIC and Flyback.

The operating frequency of the KB3302 can be set with an external resistor. The ability to set the operating frequency gives the KB3302 design flexibilities. A dedicated COMP pin allows optimization of the loop response. The KB3302 is available in thermally enhanced 8-Pin MSOP packages.

APPLICATIONS

- Flat screen LCD bias supplies
- TFT bias supplies
- XDSL power supplies
- Medical equipment
- Digital video cameras
- Portables devices
- White LED power supplies

TYPICAL APPLICATION

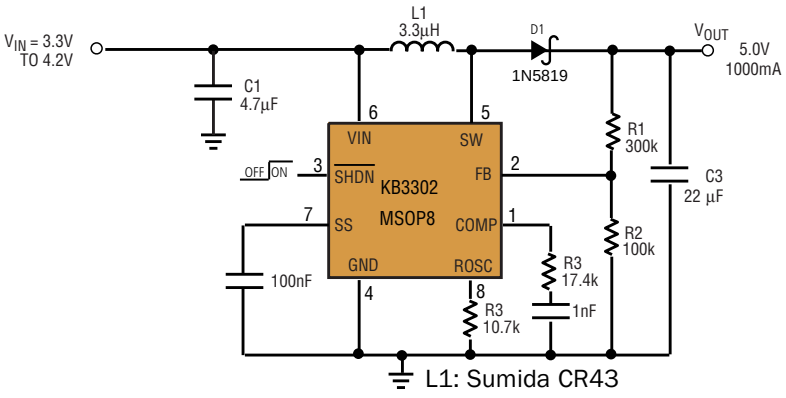
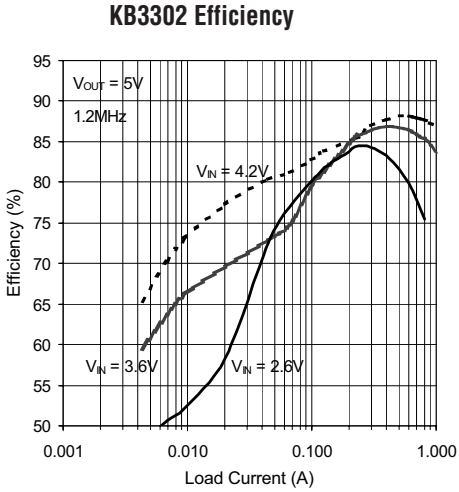


Figure 1. 1.2MHzAll Ceramic Capacitor Single Li-ion Cell to 5V Boost Converter.

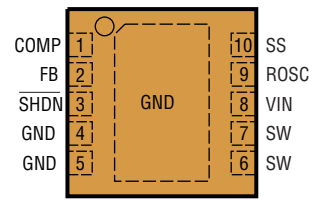


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage ..... −0.3V to 18V
SHDN, V_{FB} Voltages ..... −0.3V to 5V
SW Voltage ..... −0.3V to 32V

Peak SW Sink and Source Current 2A
Operating Temperature Range (Note 2) .. −40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACkAGE/ORDER INFORMATION

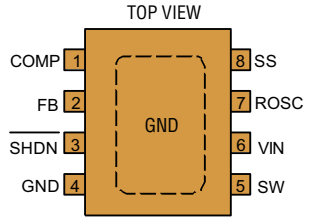


DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

EXPOSED PAD IS PGND (PIN 11)
MUST BE CONNECTED TO GND

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER
KB3302DD
3000 Units on Tape and Reel
DD PART MARKING



8-LEAD PLASTIC MSOP

EXPOSED PAD IS PGND
MUST BE CONNECTED TO GND

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER
KB3302EMS
2500 Units on Tape and Reel
EMS PART MARKING

ELECTRICAL CHARACTERISTICS

Unless specified: V_{IN} = 2V, $\overline{SHDN}$ = 1.5V, R_{osc} = 7.68kΩ, -40°C < T_A = T_J < 85°C

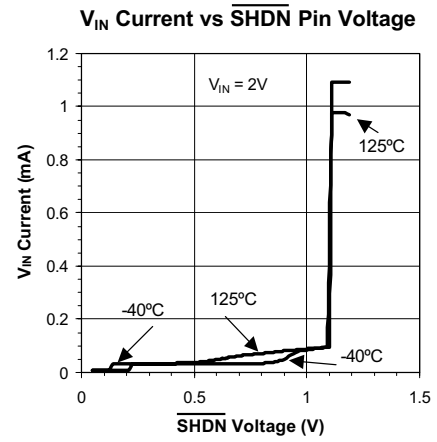
Parameter	Test Conditions	Min	Typ	Max	Unit
Undervoltage Lockout Threshold			1.3	1.4	V
Maximum Operating Voltage				16	V
Feedback Voltage	T_A = 25°C	1.224	1.242	1.260	V
	-40°C < T_A < 85°C	1.217		1.267	V
Feedback Voltage Line Regulation	1.5V < V_{IN} < 16V		0.01		%
FB Pin Bias Current			40	80	nA
Error Amplifier Transconductance			60		$\mu\Omega^{-1}$
Error Amplifier Open-Loop Gain			49		dB
COMP Source Current	V_{FB} = 1.1V		5		µA
COMP Sink Current	V_{FB} = 1.4V		5		µA
V_{IN} Quiescent Supply Current	$V_{\overline{SHDN}}$ = 1.5V, V_{COMP} = 0 (Not Switching)		1.1	1.6	mA
V_{IN} Supply Current in Shutdown	$V_{\overline{SHDN}}$ = 0		10	18	µA
Switching Frequency		1.3	1.5	1.7	MHz
Maximum Duty Cycle		85	90		%
Minimum Duty Cycle				0	%
Switch Current Limit		2	2.8		A
Switch Saturation Voltage	I_{SW} = 2A		220	350	mV

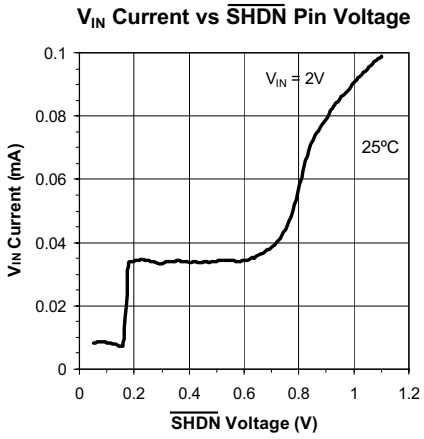
ELECTRICAL CHARACTERISTICS

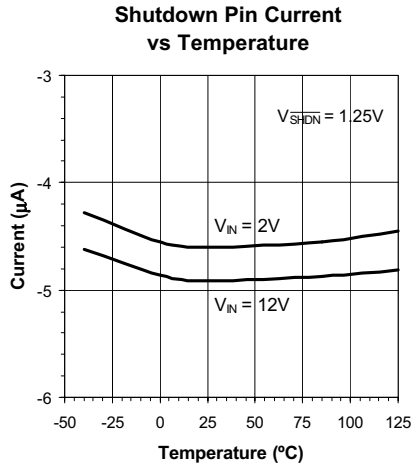
Unless specified: V_{IN} = 2V, $\overline{SHDN}$ = 1.5V, R_{OSC} = 7.68kΩ, -40°C < T_A = T_J < 85°C

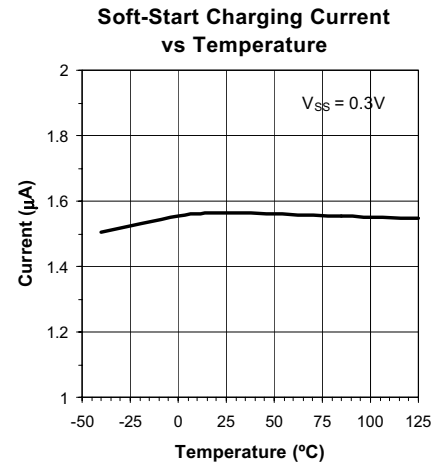
Parameter	Test Conditions	Min	Typ	Max	Unit
Switch Leakage Current	V_{SW} = 5V		0.01	1	μA
Shutdown Threshold Voltage		1.02	1.1	1.18	V
Shutdown Pin Current	$V_{\overline{SHDN}}$ = 1.2V		-4.6		μA
	$V_{\overline{SHDN}}$ = 0		0	0.1	μA
Soft-Start Charging Current	V_{SS} = 0.3V		1.5		μA
Thermal Shutdown Temperature			160		°C
Thermal Shutdown Hysteresis			10		°C

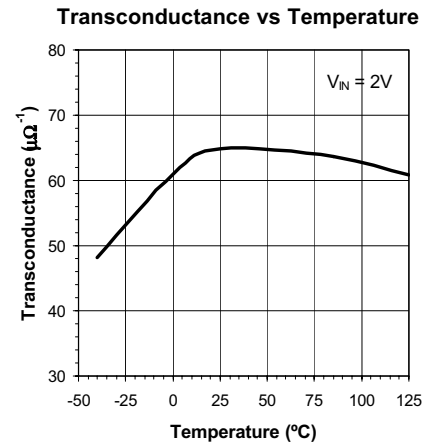
TYPICAL PERFORMANCE CHARACTERISTICS





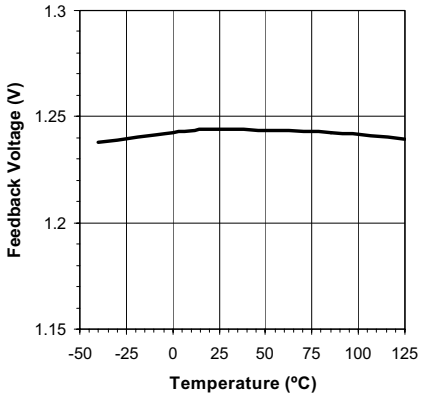




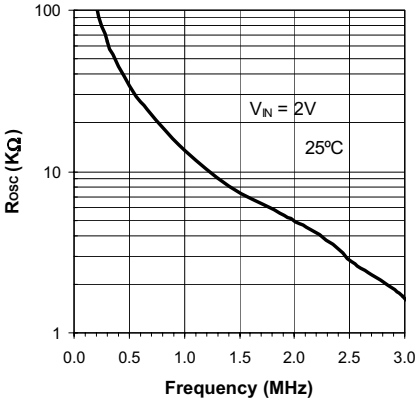


TYPICAL PERFORMANCE CHARACTERISTICS

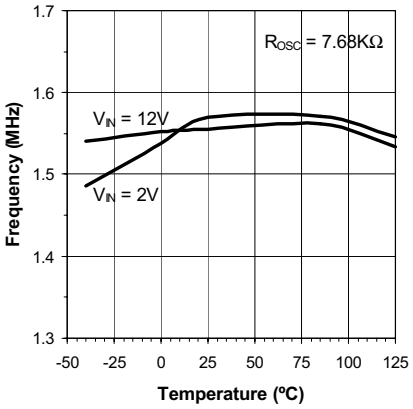
Feedback Voltage vs Temperature



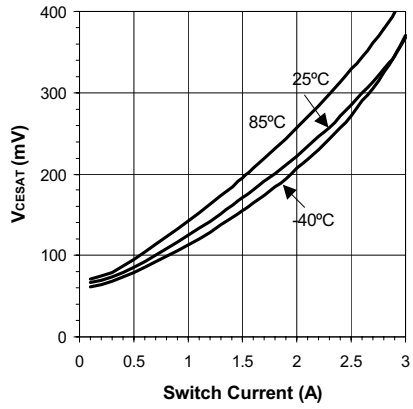
R_{OSC} vs Switching Frequency



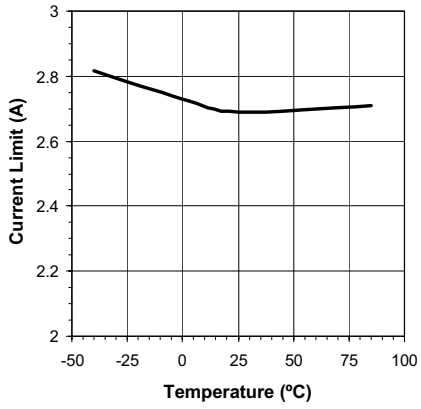
Switching Frequency vs Temperature



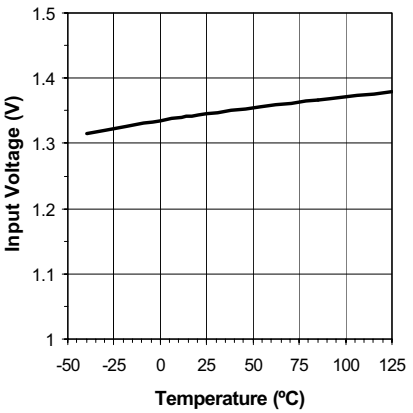
Switch Saturation Voltage vs Switch Current



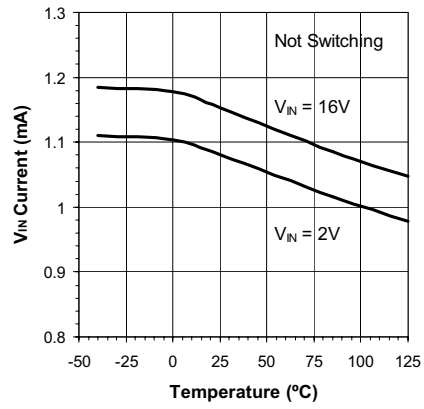
Switch Current Limit vs Temperature



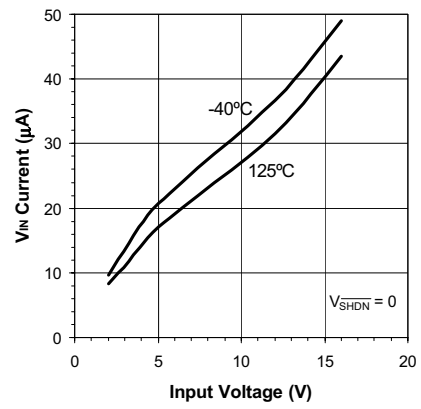
Minimum V_{IN} vs Temperature



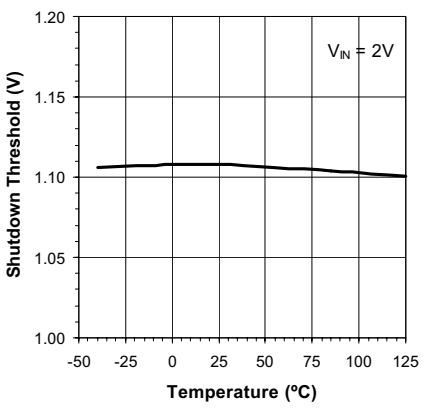
V_{IN} Quiescent Current vs Temperature



V_{IN} Current in Shutdown vs Input Voltage



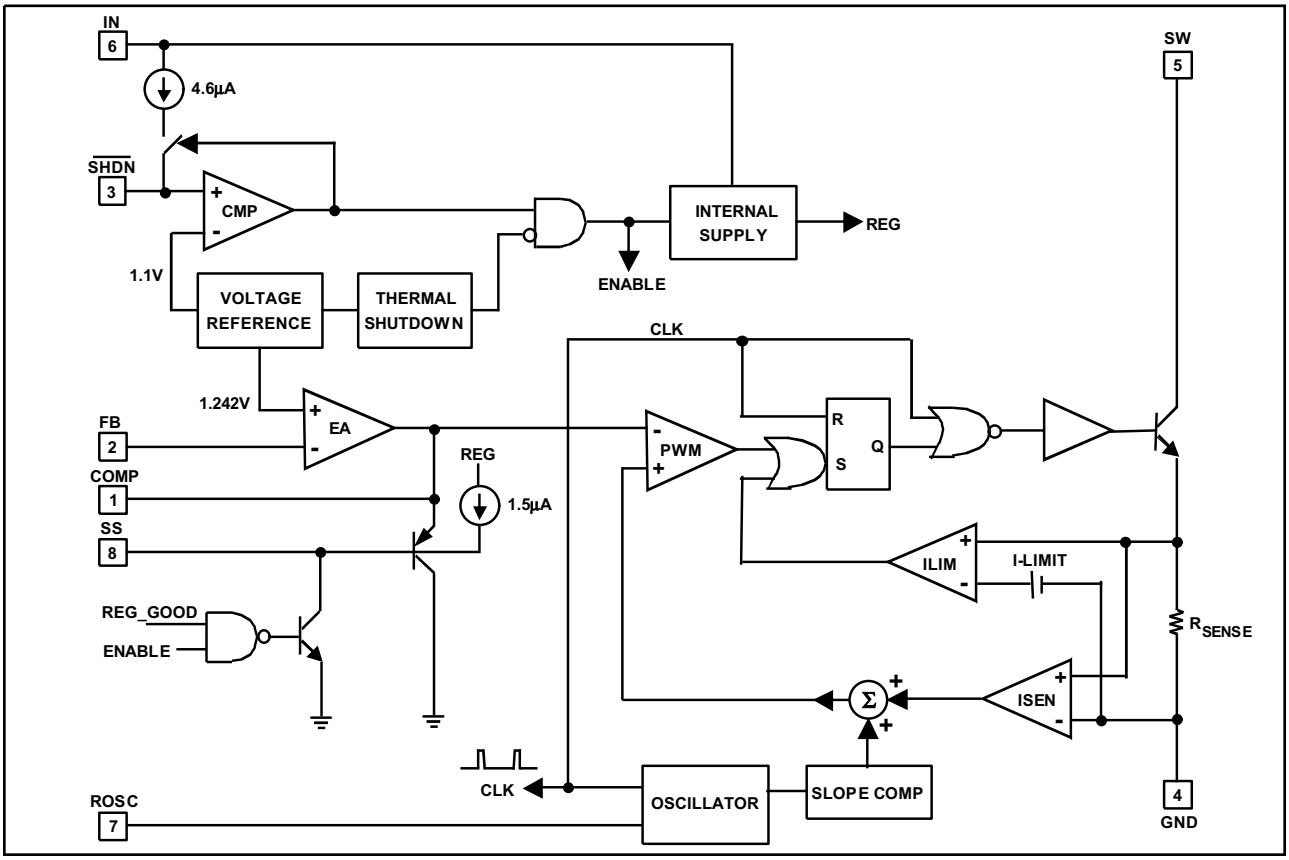
Shutdown Threshold vs Temperature



PIN FUNCTIONS

Pin	Pin Name	Pin Function
1	COMP	The output of the internal transconductance error amplifier. This pin is used for loop compensation.
2	FB	The inverting input of the error amplifier. Tie to an external resistive divider to set the output voltage.
3	$\overline{\text{SHDN}}$	Shutdown Pin. The accurate 1.1V shutdown threshold and the 4.6uA shutdown pin current hysteresis allow the user to set the undervoltage lockout threshold and hysteresis for the switching regulator. Pulling this pin below 0.1V causes the converter to shut down to low quiescent current. Tie this pin to IN if the UVLO and the shutdown features are not used. This pin should not be left floating.
4	GND	Ground. Tie to the ground plane.
5	SW	Collector of the internal power transistor. Connect to the boost inductor and the rectifying diode.
6	IN	Power Supply Pin. Bypassed with capacitors close to the pin.
7	ROSC	A resistor from this pin to the ground sets the switching frequency.
8	SS	Soft-Start Pin. A capacitor from this pin to the ground lengthens the start-up time and reduces start-up current.
	Exposed Pad	The exposed pad must be soldered to the ground plane on the PCB for good thermal conduction.

SIMPLIFIED BLOC DIAGRAM



OPERATION

The KB3302 is a programmable constant-frequency peak current-mode step-up switching regulator with an integrated 2A power transistor. Referring to the block diagrams in Figures 2 and 3, the power transistor is switched on at the trailing edge of the clock. Switch current is sensed with an integrated sense resistor. The sensed current is summed with the slope-compensating ramp before compared to the output of the error amplifier EA. The PWM comparator trip point determines the switch turn-on pulse width. The current-limit comparator ILIM turns off the power switch when the switch current exceeds the 2.8A current-limit threshold. ILIM therefore provides cycle-by-cycle current limit. Current-limit is not affected by slope compensation because the current comparator ILIM is not in the PWM signal path.

Current-mode switching regulators utilize a dual-loop feedback control system. In the KB3302 the amplifier output COMP controls the peak inductor current. This is the inner current loop. The double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop, easing loop compensation. Fast transient response can be obtained with a simple Type-2 compensation network. In the outer loop, the error amplifier regulates the output voltage.

The switching frequency of the KB3302 can be programmed up to 2MHz with an external resistor from the ROSC pin to the ground. For converters requiring extreme duty cycles, the operating frequency can be lowered to maintain the necessary minimum on time or the minimum off time.

The KB3302 requires a minimum input of 1.4V to operate. A voltage higher than 1.1V at the shutdown pin enables the internal linear regulator REG in the KB3302. After V_{REG} becomes valid, the soft-start capacitor is charged with a 1.5μA current source. A PNP transistor clamps the output of the error amplifier as the soft-start capacitor voltage rises. Since the COMP voltage controls the peak inductor current, the inductor current is ramped gradually during soft-start, preventing high input start-up current. Under fault conditions (V_{IN}<1.4V or over temperature) or when the shutdown pin is pulled below 1.1V, the soft-start capacitor is discharged to ground. Pulling the shutdown pin below 0.1V reduces the total supply current to 10μA.

APPLICATIONS INFORMATION

Setting the Output Voltage

An external resistive divider R_1 and R_2 with its center tap tied to the FB pin (Figure 4) sets the output voltage.

$$R_1 = R_2\left(\frac{V_{OUT}}{1.242V} - 1\right) \quad (1)$$

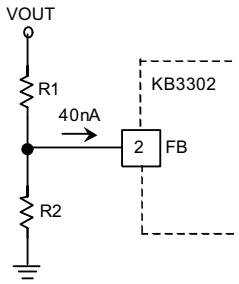


Figure 4. The Output Voltage is set with a Resistive Divider

The input bias current of the error amplifier will introduce an error of:

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{40nA(R_1 // R_2)100}{1.242V}\% \quad (2)$$

The percentage error of a V_{OUT} = 5V converter with R_1 = 100KΩ and R_2 = 301KΩ is

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{40nA(100K // 301K)100}{1.242V} = 0.24\%$$

Operating Frequency and Efficiency

Switching frequency of KB3302 is set with an external resistor from the ROSC pin to the ground. A graph showing the relationship between R_{OSC} and switching frequency is given in the “Typical Characteristics”.

High frequency operation reduces the size of passive components but switching losses are higher. The efficiencies of 5V to 12V converters operating at 700KHz, 1.35MHz and 2MHz are shown in Figure 1(b). The peak efficiency of the KB3302 appears to decrease 0.5% for every 100KHz increase in frequency.

APPLICATIONS INFORMATION

Duty Cycle

The duty cycle D of a boost converter is:

$$D = \frac{1 - \frac{V_{IN}}{V_{OUT} + V_D}}{1 - \frac{V_{CESAT}}{V_{OUT} + V_D}} \quad (3)$$

where V_{CESAT} is the switch saturation voltage and V_D is voltage drop across the rectifying diode.

Maximum Output Current

In a boost switching regulator the inductor is connected to the input. The DC inductor current is the input current. When the power switch is turned on, the inductor current flows into the switch. When the power switch is off, the inductor current flows through the rectifying diode to the output. The output current is the average diode current. The diode current waveform is trapezoidal with pulse width (1 – D)T (Figure 5). The output current available from a boost converter therefore depends on the converter operating duty cycle. The power switch current in the KB3302 is internally limited to 2A. This is also the maximum inductor or the input current. By estimating the conduction losses in both the switch and the diode, an expression of the maximum available output current of a boost converter can be derived:

$$I_{OUTMAX} = \frac{I_{LIM} V_{IN}}{V_{OUT}} \left[1 - \frac{D}{45} - \frac{V_D - D(V_D - V_{CESAT})}{V_{IN}} \right] \quad (4)$$

where I_{LIM} is the switch current limit.

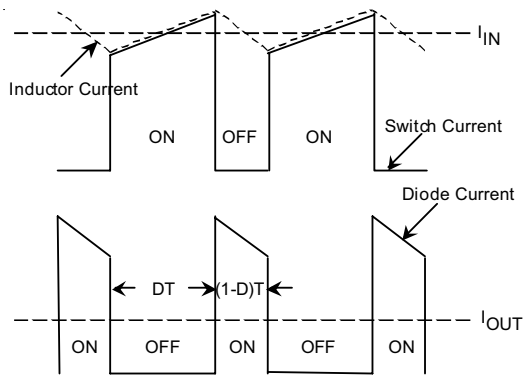


Figure 5. Current Waveforms in a Boost Regulator

It is worth noting that I_{OUTMAX} is directly proportional to the ratio $\frac{V_{IN}}{V_{OUT}}$. Equation (4) over-estimates the maximum output current at high frequencies (>1MHz) since switching losses are neglected in its derivation. Nevertheless it is a useful first-order approximation.

Using V_{CESAT} = 0.3V, V_D = 0.5V and I_{LIM} = 2A in (3) and (4), the maximum output currents for three V_{IN} and V_{OUT} combinations are shown in Table 1.

V_{IN} (V)	V_{OUT} (V)	D	I_{OUTMAX} (A)
2.5	12	0.820	0.35
3.3	5	0.423	1.14
5	12	0.615	0.76

Table 1. Calculated Maximum Output Current [Equation (4)]

Considerations for High Frequency Operation

The operating duty cycle of a boost converter decreases as V_{IN} approaches V_{OUT}. The PWM modulating ramp in a current-mode switching regulator is the sensed current ramp of the control switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum switch on time. Regulator closed-loop measurement shows that the KB3302 has a minimum on time of about 150ns at room temperature. The power switch in the KB3302 is either not turned on at all or for at least 150ns. If the required switch on time is shorter than the minimum on time, the regulator will either skip cycles or it will start to jitter.

Example: Determine the maximum operating frequency of a Li-ion cell to 5V converter using the KB3302. Assuming that V_D=0.5V, V_{CESAT}=0.3V and V_{IN}=2.6 - 4.2V, the minimum duty ratio can be found using (3).

$$D_{MIN} = \frac{1 - \frac{4.2}{5 + 0.5}}{1 - \frac{0.3}{5 + 0.5}} = 0.25$$

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The absolute maximum operating frequency of the converter is therefore $\frac{D_{MIN}}{150ns}=\frac{0.25}{150ns}=1.67MHz$. The actual operating frequency needs to be lower to allow for modulating headroom.

The power transistor in the KB3302 is turned off every switching period for an interval determined by the discharge time of the oscillator ramp and the propagation delay of the power switch. This minimum off time limits the maximum duty cycle of the regulator at a given switching frequency. A boost converter with high $\frac{V_{OUT}}{V_{In}}$ ratio requires long switch on time and high duty cycle. If the required duty cycle is higher than the attainable maximum, then the converter will operate in dropout. (Dropout is a condition in which the regulator cannot attain its set output voltage below current limit.)

The minimum off times of closed-loop boost converters set to various output voltages were measured by lowering their input voltages until dropout occurs. It was found that the minimum off time of the KB3302 ranged from 80 to 110ns at room temperature.

Beware of dropout when operating at very low input voltages (1.5-2V) and with off times approaching 110ns. Shorten the PCB trace between the power source and the device input pin, as line drop may be a significant percentage of the input voltage. A regulator in dropout may appear as if it is in current limit. The cycle-by-cycle current limit of the KB3302 is duty-cycle and input voltage invariant and is typically 2.8A. If the switch current limit is not at least 2A, then the converter is likely in dropout. The switching frequency should then be lowered to improve controllability.

Both the minimum on time and the minimum off time reduce control range of the PWM regulator. Bench measurement showed that reduced modulating range started to be a problem at frequencies over 2MHz. Although the oscillator is capable of running well above 2MHz, controllability limits the maximum operating frequency.

Inductor Selection

The inductor ripple current ΔI_L of a boost converter operating in continuous-conduction mode is

$$\Delta I_L=\frac{D(V_{IN}-V_{CESAT})}{fL} \quad (5)$$

where f is the switching frequency and L is the inductance.

Substituting (3) into (5) and neglecting V_{CESAT},

$$\Delta I_L=\frac{V_{IN}}{fL}\left(1-\frac{V_{IN}}{V_{OUT}+V_D}\right) \quad (6)$$

In current-mode control, the slope of the modulating (sensed switch current) ramp should be steep enough to lessen jittery tendency but not so steep that large flux swing decreases efficiency. Inductor ripple current ΔI_L between 25-40% of the peak inductor current limit is a good compromise. Inductors so chosen are optimized in size and DCR. Setting ΔI_L = 0.3•(2) = 0.6A, V_D=0.5V in (6),

$$L=\frac{V_{IN}}{f\Delta I_L}\left(1-\frac{V_{IN}}{V_{OUT}+V_D}\right)=\frac{V_{IN}}{0.6f}\left(1-\frac{V_{IN}}{V_{OUT}+0.5}\right) \quad (7)$$

where L is in µH and f is in MHz.

Equation (6) shows that for a given V_{OUT}, ΔI_L is the highest when $V_{IN}=\frac{(V_{OUT}+V_D)}{2}$. If V_{IN} varies over a wide range, then choose L based on the nominal input voltage.

The saturation current of the inductor should be 20-30% higher than the peak current limit (2.8A). Low-cost powder iron cores are not suitable for high-frequency switching power supplies due to their high core losses. Inductors with ferrite cores should be used.

Input Capacitor

The input current in a boost converter is the inductor current, which is continuous with low RMS current ripples. A 2.2-4.7µF ceramic input capacitor is adequate for most applications.

Output Capacitor

Both ceramic and low ESR tantalum capacitors can be used as output filtering capacitors. Multi-layer ceramic capacitors, due to their extremely low ESR (<5mΩ), are the best choice. Use ceramic capacitors with stable temperature and voltage characteristics. One may be tempted to use Z5U and Y5V ceramic capacitors for output filtering because of their high capacitance and

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small sizes. However these types of capacitors have high temperature and high voltage coefficients. For example, the capacitance of a Z5U capacitor can drop below 60% of its room temperature value at –25°C and 90°C. X5R ceramic capacitors, which have stable temperature and voltage coefficients, are the preferred type.

The diode current waveform in Figure 5 is discontinuous with high ripple-content. In a buck converter the inductor ripple current ΔI_L determines the output ripple voltage. The output ripple voltage of a boost regulator is however much higher and is determined by the absolute inductor current. Decreasing the inductor ripple current does not appreciably reduce the output ripple voltage. The current flowing in the output filter capacitor is the difference between the diode current and the output current. This capacitor current has a RMS value of:

$$I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}-1} \qquad (8)$$

If a tantalum capacitor is used, then its ripple current rating in addition to its ESR will need to be considered.

When the switch is turned on, the output capacitor supplies the load current I_{OUT} (Figure 5). The output ripple voltage due to charging and discharging of the output capacitor is therefore:

$$\Delta V_{OUT} = \frac{I_{OUT}DT}{C_{OUT}} \qquad (9)$$

For most applications, a 10-22μF ceramic capacitor is sufficient for output filtering. It is worth noting that the output ripple voltage due to discharging of a 10μF ceramic capacitor (9) is higher than that due to its ESR.

Rectifying Diode

For high efficiency, Schottky barrier diodes should be used as rectifying diodes for the KB3302. These diodes should have a RMS current rating of at least 1A and a reverse blocking voltage of at least a few Volts higher than the output voltage. For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use rectifying diodes with somewhat higher RMS current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The rectifying diodes should be placed close to the SW pins of the KB3302 to minimize ringing due to trace inductance. Surface-mount equivalents of 1N5817, 1N5819, MBRM120 (ON Semi) and 10BQ015 (IRF) are all suitable.

Soft-Start

Soft-start prevents a DC-DC converter from drawing excessive current (equal to the switch current limit) from the power source during start up. If the soft-start time is made sufficiently long, then the output will enter regulation without overshoot. An external capacitor from the SS pin to the ground and an internal 1.5μA charging current source set the soft-start time. The soft-start voltage ramp at the SS pin clamps the error amplifier output. During regulator start-up, COMP voltage follows the SS voltage. The converter starts to switch when its COMP voltage exceeds 0.7V. The peak inductor current is gradually increased until the converter output comes into regulation. If the shutdown pin is forced below 1.1V or if fault is detected, then the soft-start capacitor will be discharged to ground immediately.

The SS pin can be left open if soft-start is not required.

Shutdown

The input voltage and shutdown pin voltage must be greater than 1.4V and 1.1V respectively to enable the KB3302. Forcing the shutdown pin below 1.1V stops switching. Pulling this pin below 0.1V completely shuts off the KB3302. The total V_{IN} current decreases to 10μA at 2V. Figure 6 shows several ways of interfacing the control logic to the shutdown pin. Beware that the shutdown pin is a high impedance pin. It should always be driven from a low-impedance source or tied to a resistive divider. Floating the shutdown pin will result in undefined voltage. In Figure 6(c) the shutdown pin is driven from a logic gate whose V_{OH} is higher than the supply voltage of the KB3302. The diode clamps the maximum shutdown pin voltage to one diode voltage above the input power supply.

APPLICATIONS INFORMATION

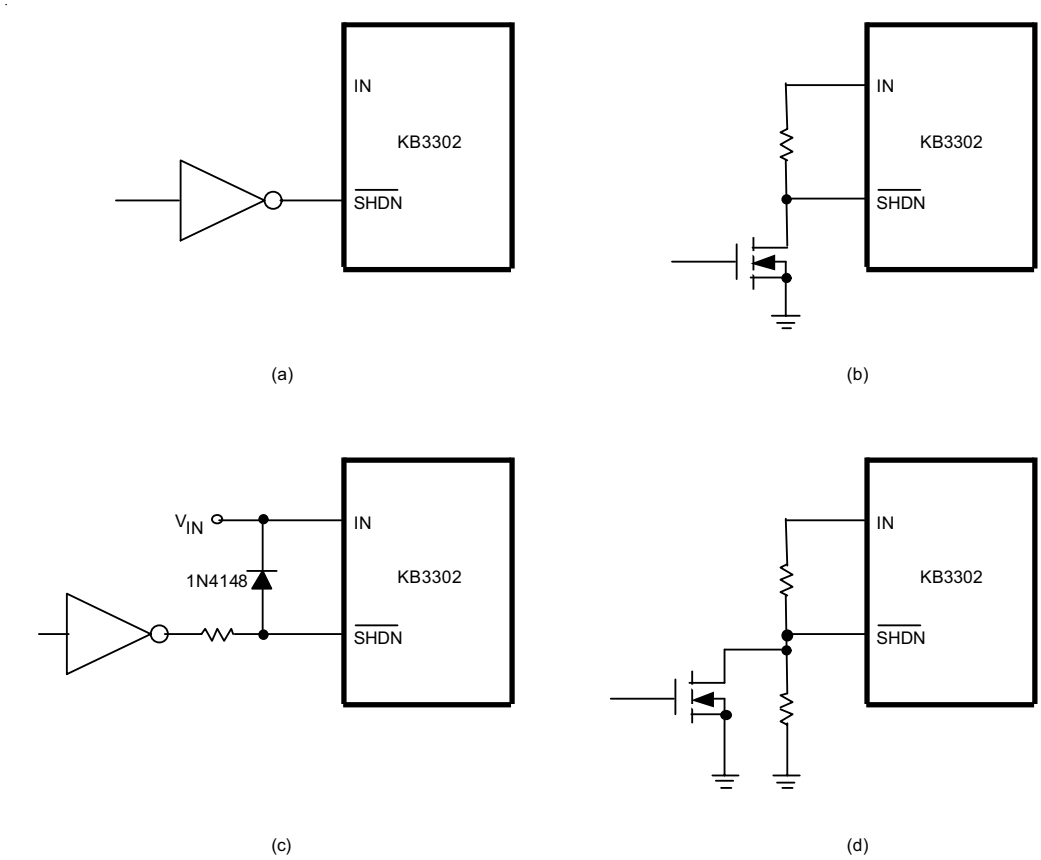

Figure 6. Methods of Driving the Shutdown Pin
(a) Directly Driven from a Logic Gate
(b) Driven from an Open-drain N-channel MOSFET or an Open-Collector NPN Transistor (V_{OL} < 0.1V)
(c) Driven from a Logic Gate with V_{OH} > V_{IN}
(d) Combining Shutdown with Programmed UVLO (See Section Below).

Programming Undervoltage Lockout

The KB3302 has an internal V_{IN} undervoltage lockout (UVLO) threshold of 1.4V. The transition from idle to switching is abrupt but there is no hysteresis. If the input voltage ramp rate is slow and the input bypass is limited, then sudden turn on of the power transistor will cause a dip in the line voltage. Switching will stop if V_{IN} falls below the internal UVLO threshold. The resulting output voltage rise may be non-monotonic. The 1.1V disable threshold of the KB3302 can be used in conjunction with a resistive voltage divider to raise the UVLO threshold and to add an UVLO hysteresis. Figure 7 shows the scheme. Both V_H and V_L (the desired upper and the lower UVLO threshold voltages) are determined by the 1.1V threshold crossings,

V_H and V_L are therefore:

$$V_H = \left(1 + \frac{R_3}{R_4}\right)(1.1V)$$
$$V_L = V_H - V_{HYS} = V_H - I_{HYS}R_3 \quad (10)$$

Re-arranging,

$$R_3 = \frac{V_{HYS}}{I_{HYS}} \quad (11)$$

$$R_4 = \frac{R_3}{\frac{V_H}{1.1} - 1} \quad (12)$$

APPLICATIONS INFORMATION

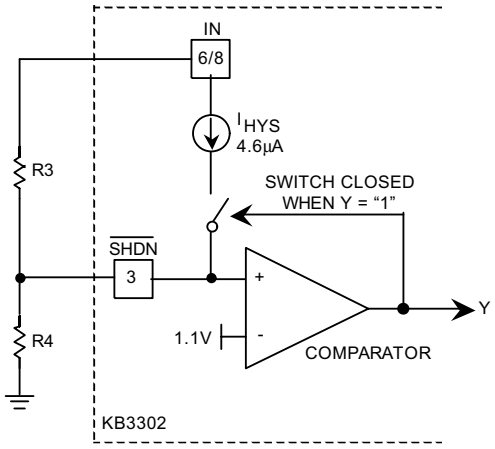

Figure 7. Programmable Hysteretic UVLO Circuit

with $V_L > 1.4V$.

Example: Increase the turn on voltage of a V_{IN} = 3.3V boost converter from 1.4V to 2.75V.

Using V_H = 2.75V and R_4 = 100KΩ in (12),

$$R_3 = 150K\Omega .$$

The resulting UVLO hysteresis is:

$$V_{HYS} = I_{HYS}R_3 = 4.6\mu A \bullet 150K\Omega = 0.69V .$$

The turn off voltage is:

$$V_L = V_H - V_{HYS} = 2.75 - 0.69 = 2.06V > 1.4V .$$

Frequency Compensation

Figure 8 shows the equivalent circuit of a boost converter using the KB3302. The output filter capacitor and the load form an output pole at frequency:

$$\omega_{p2} = -\frac{2I_{OUT}}{V_{OUT}C_2} = -\frac{2}{R_{OUT}C_2} \quad (13)$$

where C_2 is the output capacitor and $R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$ is the equivalent load resistance.

The zero formed by C_2 and its equivalent series resistance (ESR) is neglected due to low ESR of the ceramic output capacitor.

There is also a right half plane (RHP) zero at angular frequency:

$$\omega_{Z2} = \frac{R_{OUT}(1-D)^2}{L} \quad (14)$$

ω_{z2} decreases with increasing duty cycle D and increasing I_{OUT}. Using the 5V to 12V boost regulator (1.35MHz) in Figure 1(a) as an example,

$$R_{OUT} \geq \frac{5V}{0.74A} = 6.8\Omega$$

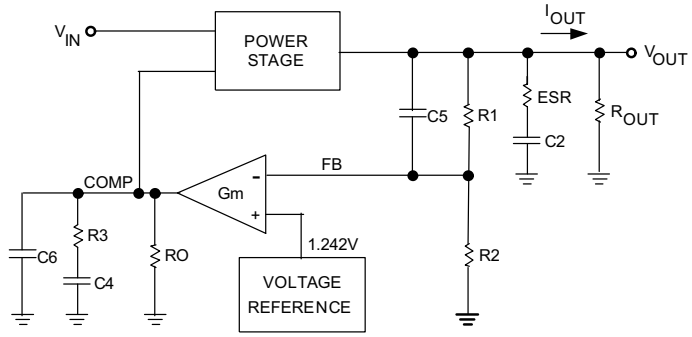

Figure 8. Simplified Block Diagram of a Boost Converter

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$$D = \frac{1 - \frac{5}{12 + 0.5}}{1 - \frac{0.3}{12 + 0.5}} = 0.62$$

Therefore

$$|\omega_{p2}| \le \frac{2}{(6.8\Omega) \bullet (10\mu F)} = 29.4 Krads^{-1} = 4.68KHz$$

and

$$\omega_{Z2} \ge \frac{6.8\Omega \bullet (1 - 0.62)^2}{4.7\mu H} = 209 Krads^{-1} = 33.3KHz$$

The spacing between p_2 and z_2 is the closest when the converter is delivering the maximum output current from the lowest V_{IN}. This represents the worst-case compensation condition. Ignoring C_5 and C_6 for the moment, C_4 forms a low frequency pole with the equivalent output resistance R_0 of the error amplifier:

$$R_0 = \frac{\text{Amplifier Open Loop Gain}}{\text{Transconductance}} = \frac{49dB}{60\mu\Omega^{-1}} = 4.7M\Omega$$

$$\omega_{p1} = -\frac{1}{R_0 C_4} = -\frac{1}{4.7M\Omega \bullet 820pF}$$

$$= -260 \text{ rads}^{-1} = -41Hz$$

C_4 and R_3 also forms a zero with angular frequency:

$$\omega_{Z1} = -\frac{1}{R_3 C_4} = -\frac{1}{30.9K\Omega \bullet 820pF}$$

$$= -39.5 \text{ Krads}^{-1} = -6.3KHz$$

The poles p_1, p_2 and the RHP zero z_2 all increase phase shift in the loop response. For stable operation, the overall loop gain should cross 0dB with -20dB/decade slope. Due to the presence of the RHP zero, the 0dB crossover frequency should not be higher than $\frac{z_2}{3}$. Placing z_1 near p_2 nulls its effect and maximizes loop bandwidth. Thus

$$R_3 C_4 \approx \frac{V_{OUT} C_2}{2 I_{OUT(MAX)}} \qquad (15)$$

R_3 determines the mid-band loop gain of the converter. Increasing R_3 increases the mid-band gain and the crossover

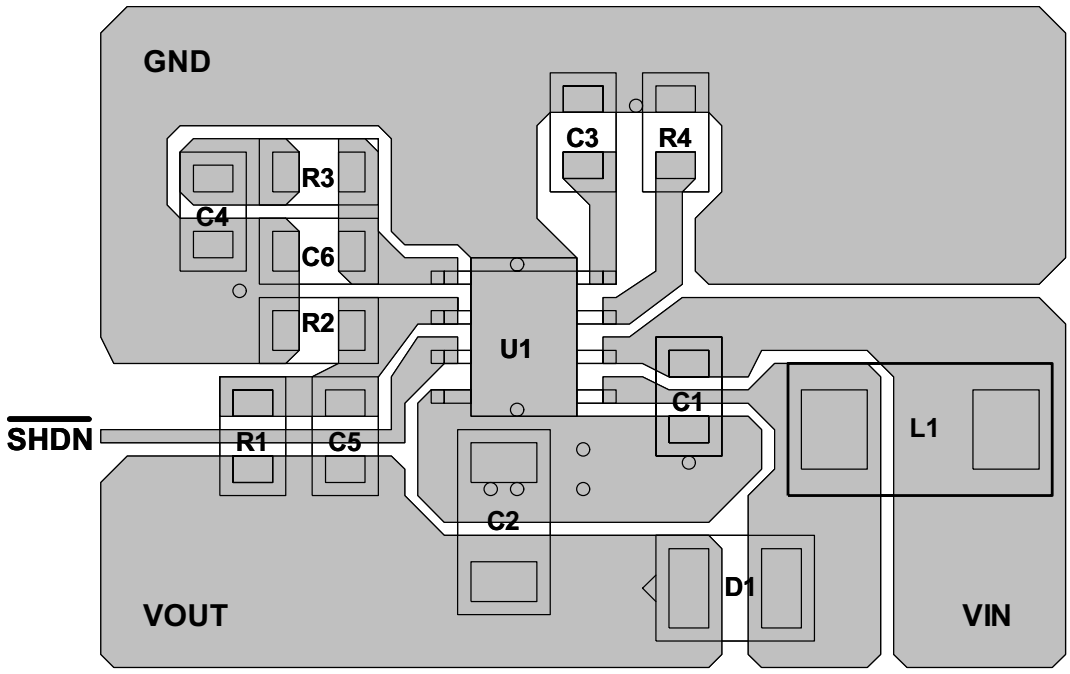

Figure 9. Suggested PCB Layout for the KB3302. Notice that there is no via directly under the device. All vias are 12mil in diameter.

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frequency. However it reduces the phase margin. The values of R_3 and C_4 can be determined empirically by observing the inductor current and the output voltage during load transient. Compensation is optimized when the largest R_3 and the smallest C_4without producing ringing or excessive overshoot in its inductor current and output voltage are found.

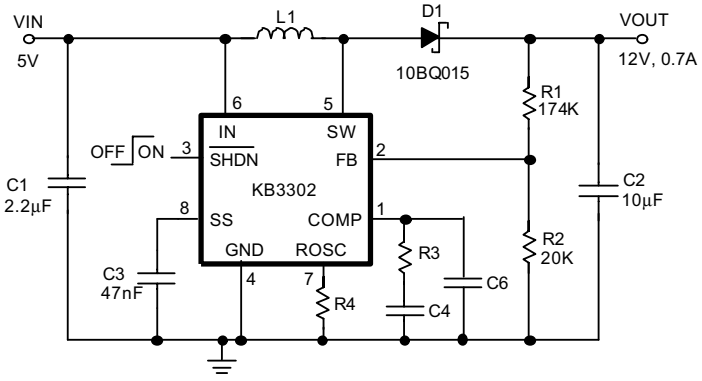
C_5 adds a feedforward zero to the loop response. In some cases it improves the transient speed of the converter. C_6 rolls off the gain at high frequency. This helps to stabilize the loop. C_5 and C_6 are often not needed.

Board Layout Considerations

In a step-up switching regulator, the output filter capacitor, the main power switch and the rectifying diode carry switched currents with high di/dt. For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switch is integrated inside the KB3302, grounding the output filter capacitor next to the KB3302 ground pin minimizes size of the high di/dt current loop. The input bypass capacitors should also be placed close to the input pins. Shortening the trace at the SW node reduces the parasitic trace inductance. This not only reduces EMI but also decreases the sizes of the switching voltage spikes and glitches.

Figure 9 shows how various external components are placed around the KB3302. The frequency-setting resistor should be placed near the ROSC pin with a short ground trace on the PC board. These precautions reduce switching noise pickup at the ROSC pin.

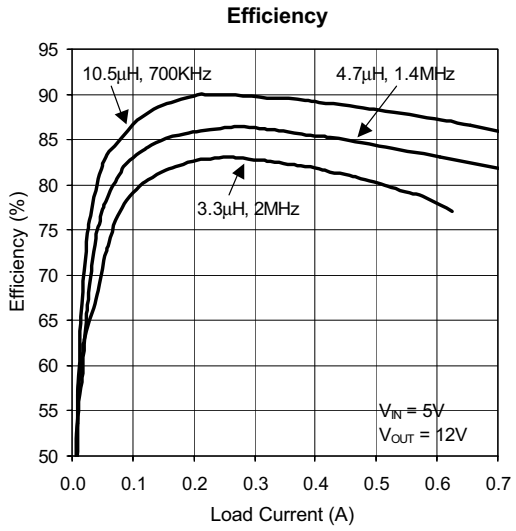
To achieve a junction to ambient thermal resistance (θ_{JA}) of 40°C/W, the exposed pad of the KB3302 should be properly soldered to a large ground plane. Use only 12mil diameter vias in the ground plane if necessary. Avoid using larger vias under the device. Molten solder may seep through large vias during reflow, resulting in poor adhesion, poor thermal conductivity and low reliability.



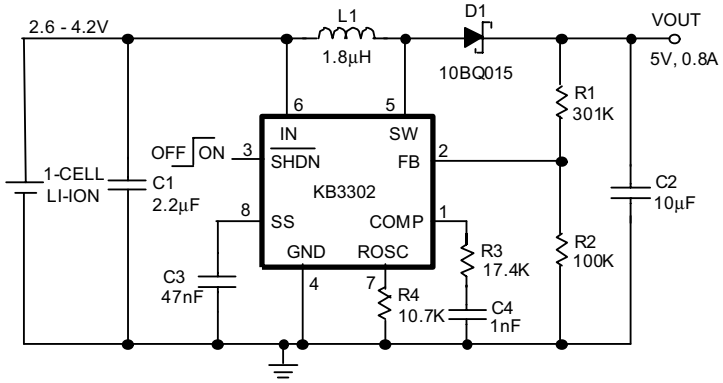
All Capacitors are Ceramic.
MSOP-8 Pinout

f / MHz	R_3 / KΩ	R_4 / KΩ	C_4 / pF	C_6 / pF	L_1 / µH
0.7	22.1	22.1	2200	-	10.5 (Falco D08019)
1.35	30.9	9.31	820	-	4.7 (Falco D08017)
2	63.4	4.75	470	22	3.3 (Coilcraft DO1813P)

Figure 10(a). 1.35 MHz All Ceramic Capacitor 5V to 12V Boost Converter. Pinout Shown is for MSOP-8



PACAGE DESCRIPTION



L1: Sumida CR43

Figure 11(a). 1.2 MHz All Ceramic Capacitor Single Li-ion Cell to 5V Boost Converter.

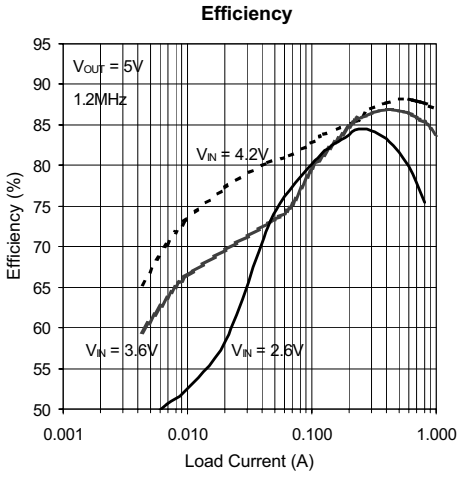
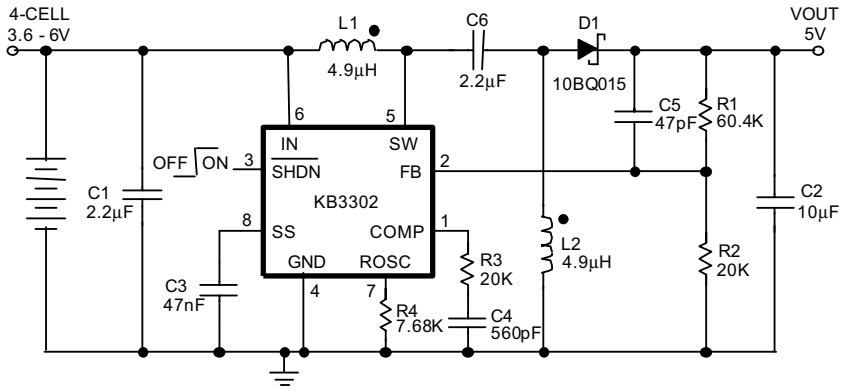


Figure 11(b). Efficiency of the Single Li-ion Cell to 5V Boost Converter in Figure 11(a).



L1 and L2: Coiltronics CTX5-1

Figure 12(a). 1.5 MHz All Ceramic Capacitor 4-Cell to 5V SEPIC Converter. Pinout Shown is for MSOP-8.

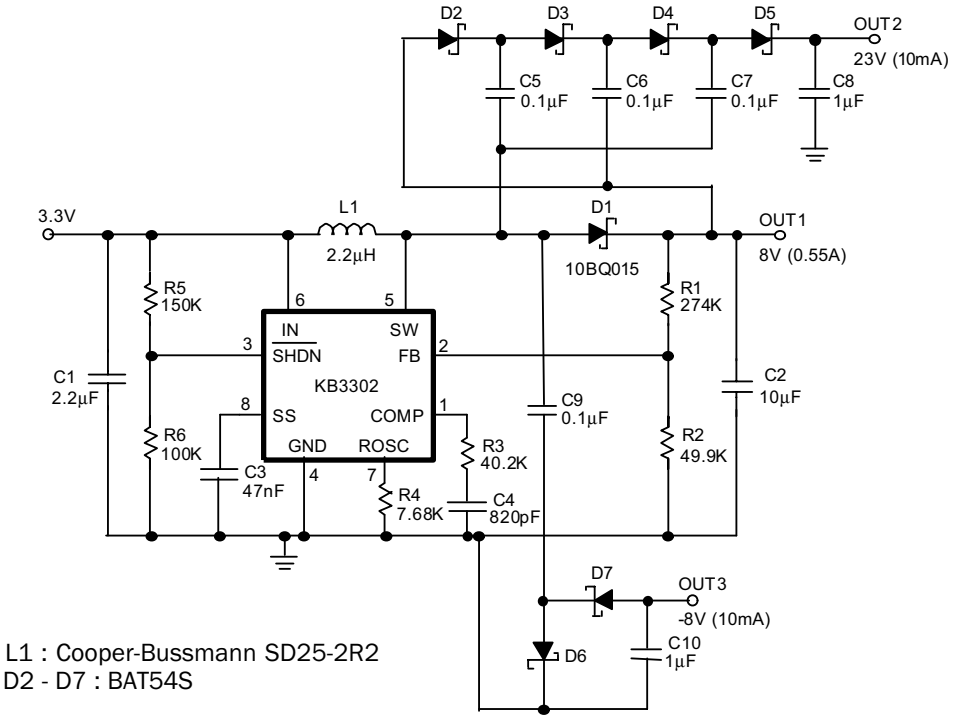


Figure 13(a). 1.5MHz Triple-Output TFT Power Supply.

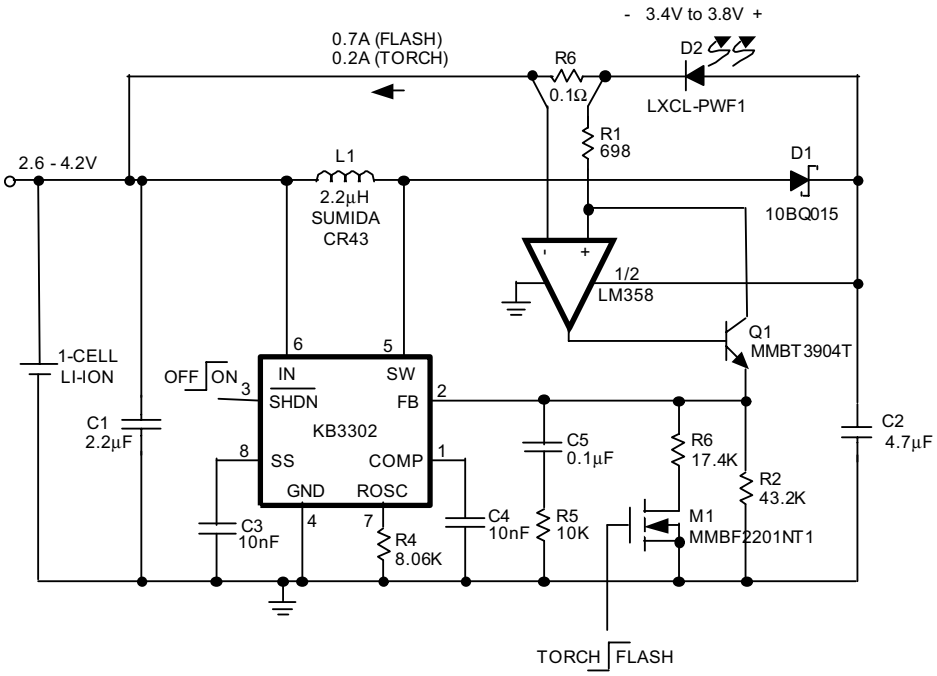
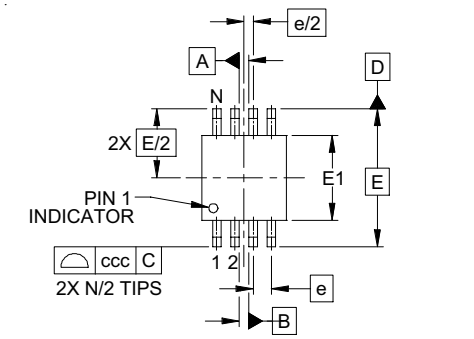
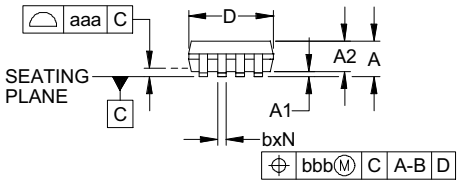
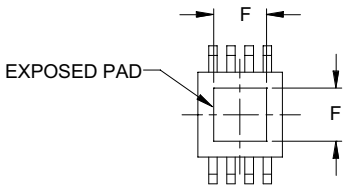


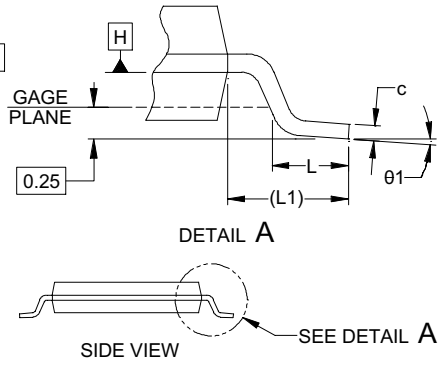
Figure 14(a). 1.4MHz Luxeon™ Flash White LED Driver for Camera Phones

PACAGE DESCRIPTION - MSOP8







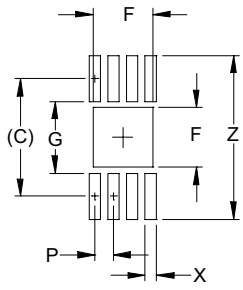


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
F	.068	.076	.080	1.73	1.93	2.03
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(0.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION AA-T.

Land Pattern - MSOP-8L-EDP

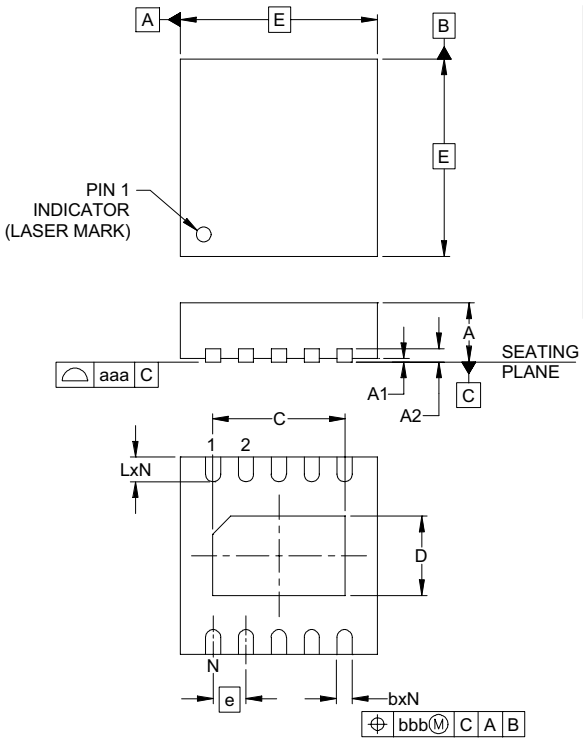


DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
F	.081	2.08
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PACAGE DESCRIPTION - DFN33

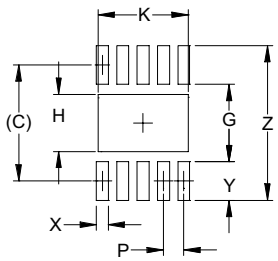


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.011	0.18	0.23	0.30
C	.074	.079	.083	1.87	2.02	2.12
D	.042	.048	.052	1.06	1.21	1.31
E	.114	.118	.122	2.90	3.00	3.10
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern - DFN33-10



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.020	0.50
X	.012	0.30
Y	.037	0.95
Z	.150	3.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.