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MV6001

HDLC/DMA CONTROLLER

The MV6001 is a combined HDLC transceiver and DMA controller capable of providing serial communications at rates up to 128K bits/second, and handling direct memory access clock rates up to 8MHz.

FEATURES

- Data Rates up to 128K Bits/s
- DMA Rate up to 8MHz
- Low Power CMOS
- Simple Interfacing to Popular 8-Bit Processors
- Frame Length up to 2K Bytes
- Low Host-Processor Overhead
- Conforms to ECMA40 and Related Standards (CCITT X25, X75, 1.440, ISO3309, ANSI X3.66, FED-STD 1003, FIPS71)

APPLICATIONS

- ISDN Terminals
- LANs
- X25 p.s.s. Networks

ORDERING INFORMATION

MV6001 B0 DP (Commercial Plastic DIP)
MV6001 B0 DG (Commercial Ceramic DIP)

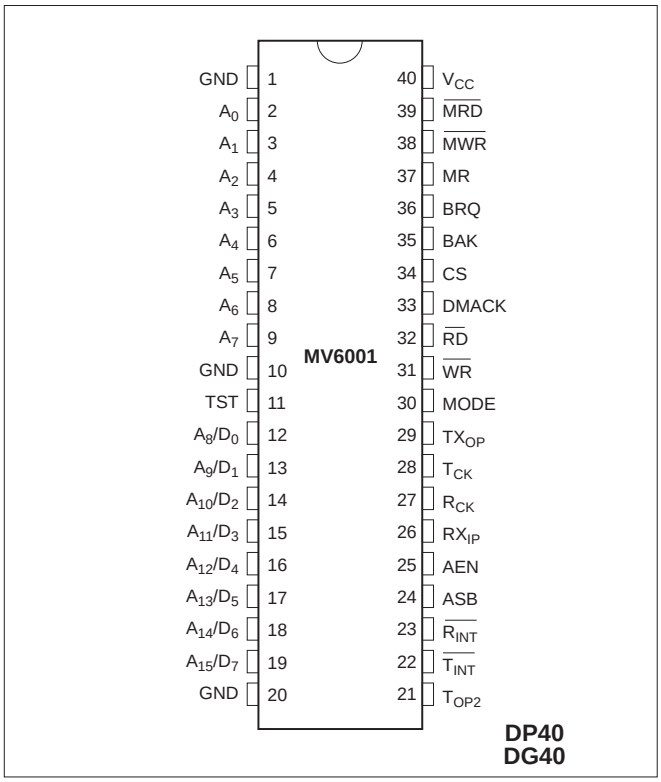

Figure 1: Pin connections - top view

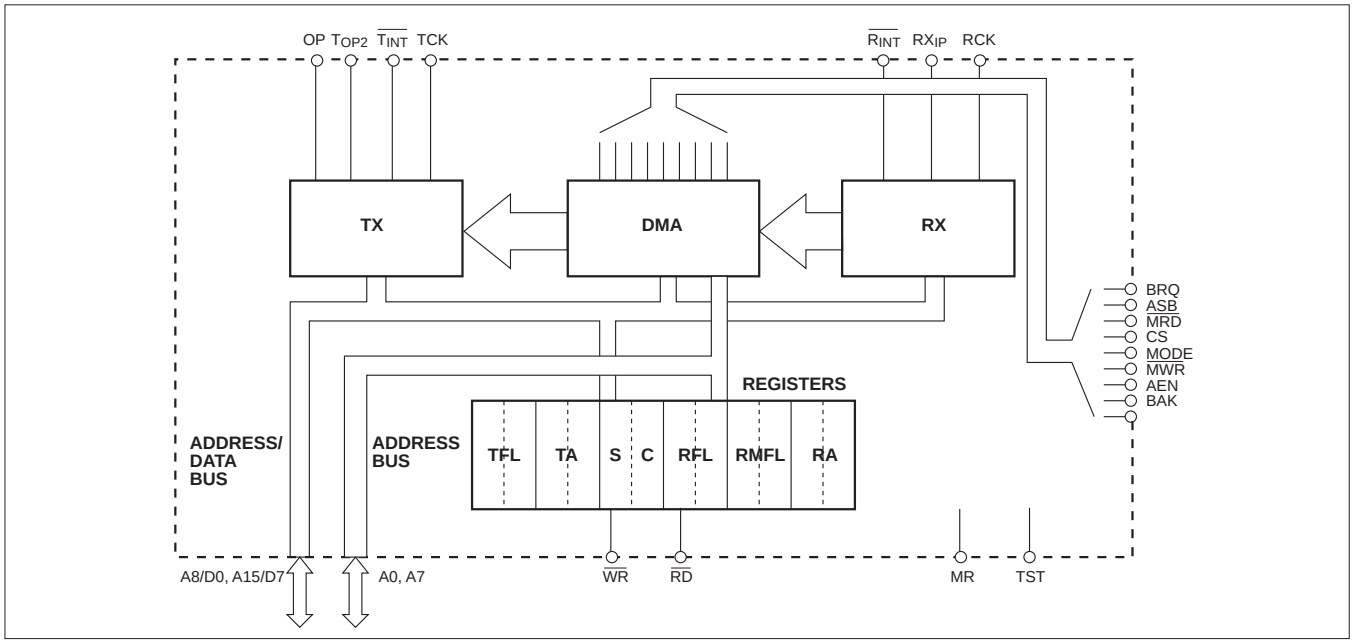

Figure 2: Block diagram

PIN DESCRIPTION

Pin No.	Name	I/O	Function
1,10,20	GND		**0V supply**. All 3 pins must be connected.
2 - 9	A_0 - A_7	I/O	**Address Bus**. Output for memory A_0 - A_7 addressing. Input for register addresses A_0- A_3.
11	TST	I	**Test Enable**. Tie to GND for normal operation.
12-19	A_8/D_0- A_{15}/D_7	I/O	**Data Bus/High Order Address**. Multiplexed data and address bus.
21	TOP2	O	**Transmitter Out**. Alternative output to TX_{OP}. This output is not affected by loop back (see Operating Notes - LOOPBACK).
22	$\overline{T}_{INT}$	O	**Transmitter Interrupt**. An interrupt is generated whenever transmission of a frame is ended, either following the last FCS byte of a complete frame of when an abort sequence is transmitted. The interrupt is reset by the control register.
23	$\overline{R}_{INT}$	O	**Receiver Interrupt**. An interrupt is generated whenever a frame is received. The interrupt is reset by the counter register.
24	ASB	O	**Address Strobe**. Strobes the Address High byte from the Data/Address Bus into an external latch.
25	AEN	O	**Address Enable**. Enables the external address latch.
26	RX_{IP}	I	**Receiver Input**. Serial HDLC data input, clocked in by RCK.
27	RCK	I	**Receiver Data Clock**. Provides clock to the receiver section, frequency should be at the required data rate, this need not necessarily the the same as the transmit data rate.
28	TCK	I	**Transmitter Data Clock**. This input provides a clock signal for the transmitter section and should be set to the desired transmit data rate.
29	TX_{OP}	O	**Transmitter output.** Main transmitter output for serial data.
30	MODE	I	**Bus Control Mode Select**. Controls the polarity of BAK and BRQ. MODE = V_{CC} gives active LOW, MODE = GND gives active HIGH.
31	$\overline{WR}$	I	**Write Register.** Loads data from data bus into register addressed by A_0- A_3.
32	$\overline{RD}$	I	**Read Register**. Reads addressed register onto data bus
33	DMACK	I	**DMA Clock.** This input provides clock to the DMA section. The DMA clock rate should be at least ten times the sum of the transmit and receive data rates.
34	CS	I	**Chip Select**. Enables $\overline{RD}$ and $\overline{WR}$ inputs.
35	BAK	I	**Bus Acknowledge**. Input from processor relinquishing control of bus. See pin 30, Bus Mode Select.
36	BRQ	O	**Bus Request**. Output to processor requesting the bus for a DMA cycle. See pin 30, Bus Mode Select.
37	MR	I	**Master Reset**. Resets everything.
38	$\overline{MWR}$	O	**Memory Write**. This is a three-state output to write data into memory during DMA cycles.
39	$\overline{MRD}$	O	**Memory Read**. 3-state output to read data from memory during DMA cycles.
40	V_{CC}		±5V ±10% supply.

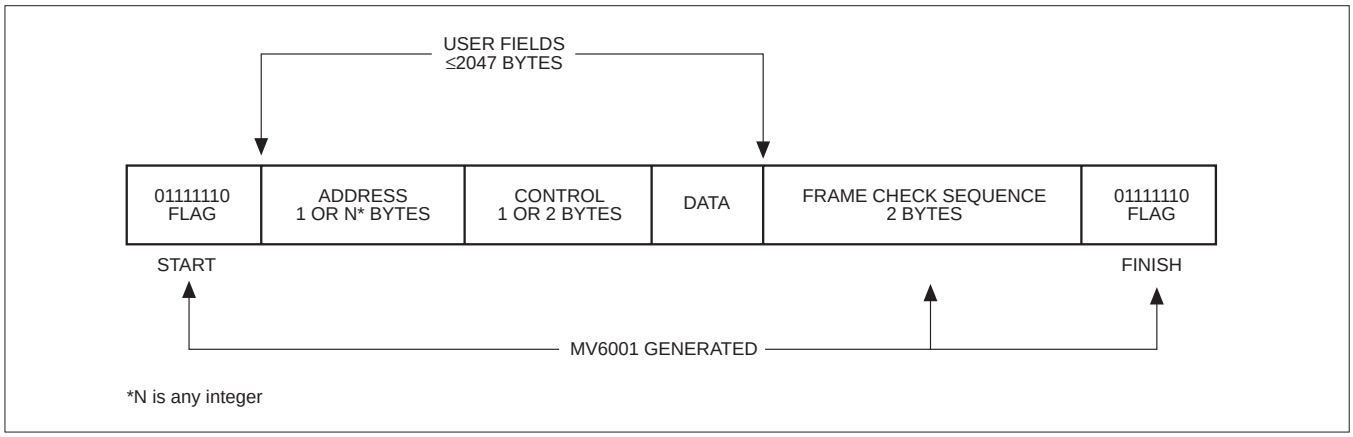

Figure 3

Fig.3 shows the construction of an HDLC frame. The start and finish of the frame are determined by FLAGS (the binary pattern 01111110). To prevent spurious recognition of flags in the user fields, the transmitter automatically inserts a '0' after five successive '1 's. The inserted '0's are removed by the receiver, and hence are not seen by the user. Each HDLC frame contains a 2 byte frame check sequence produced by a cyclic redundancy generator in the transmitter. This sequence is checked by the receiver to validate the frame.

There are two other sequences which have specific meanings - IDLE and ABORT. The IDLE state is the transmission of at least 15 continuous '1's without inserted zeros. ABORT is 7 to 14 consecutive '1's without inserted zeros sandwiched between two zeros.

FUNCTIONAL DESCRIPTION

The MV6001 consists of four main sections; transmitter, receiver, DMA unit and register bank. Each of the transminer~ receiver and DMA unit have their own clocks running at the required data rates. There are no restrictions on the relative timing between transmit and receive clocks, the DMA clock rate should be greater than ten times the sum of the transmit and receive clock rates.

TRANSMISSION

In its steady state the transmitter produces a continuous stream of FLAGS until the control register is loaded with a transmit instruction. The transmitter then, at intervals, requests the DMA unit to fetch a byte of data. This is then transferred from the system memory via the data bus to the transmitter. (If the DMA unit should fail to fetch a byte of data by the time the next request arrives then an under-run will occur and the transmitter will transmit an ABORT sequence). Data is converted into a serial stream with inserted zeros after five ones, and the 16-bit frame check sequence is appended at the end of each frame. As soon as the last bit of the FCS has been clocked out, the TINT OUtPUt goes low to inform the processor that transmission has ended.

INITIALISATION

To start transmission, two items of information are required - the start address for the data to be transmitted, and the length of the user fields are loaded into the TA and TFL registers respectively, after which the transmit enable bit (D0) can be set at any time to start transmission. Once a transmission has been started, the only way it can by stopped is to set the abort bit (D1). The transmitter will then transmit the abort sequence followed by flags. Transmitter reset (D2) resets the transmitter interrupt TINT, clears the TA and TFL registers and bits D0 and D1 of the status register. Transmitter reset is disabled during a transmission.

INTERRUPT

A transmitter interrupt ($\overline{T_{INT}}$) is generated whenever a transmission ceases, the status register can then be read to check if the frame was aborted or not. The interrupt is reset by writing a transmitter reset to the control register. NB. The status register must be read before a transmitter reset as this will alter the contents of the status register.

STATUS

The transmitter has two status bits - transmitting data (Do) and abort (D1) The transmitting data bit should always be low after $\overline{T_{INT}}$ signifying that transmission is ended. The abort bit will be high whenever a frame is aborted either by an abort instruction to the control register, or internally due to an under-run .

RECEPTION

The receiver accepts serlal data, removes inserted zeros and checks the frame check sequence. For each byte of data received, the receiver section generates a DMA request to transfer the data to memory. If the DMA controller fails to make the transfer before the next request from the receiver, then the receiver will drop out and give a receiver. interrupt with the code in the status register for overrun. If the number of bytes received reaches the number in the receive maximum frame length registerthe receiverwilldropoutand give an interrupt with the code in the status register for frame too long.

INITIALISATION

The RA register (2 bytes) is loaded with the address where the first received byte of data is to be stored. The RMFL register (11 bits) is loaded with the maximum number of bytes in the user fields plus 3 bytes (+2 bytes for the FCS, +1 byte because an interrupt will occur when the frame length is equal to the length set by the number in the register) .

CONTROL

The receiver has two control bits in the control register, receive enable (D3) and receive reset (D4). Once the RA and RMFL registers have been loaded, the receive enable bit can be set at any time to allow the receiver to receive a frame. Once set, the receive enable bit cannot be overwritten and receive reset is disabled until a frame has been received.

Receiver reset will reset the $\overline{R_{INT}}$ interrupt bit, registers RFL, RMFL, RA and bits D2 - D7 of the status register.

INTERRUPT

A receive interrupt ($\overline{R_{INT}}$) is generated whenever a frame is received. The status register can then be read to check the status of the received frame. The interrupt is reset by writing a receiver reset to the control register. Since the reset will clear the receiver bits in the status register, the register must be read before writing the reset to the control register.

STATUS

The receiver uses bits D2 - D7 of the status register (see Figs. 5 and 6). A valid frame is indicated by both 'overrun' (D6) and 'frame too long' (D7) bits being high. Following $\overline{R_{INT}}$ the 'free to receive' bit (D2) should be low, indicating that a frame has been received. The abort, overrun and long frame bits will be set according to the state of the frame received. The flag (D4) and idle (D3) bits monitor the incoming signal continuously even when the receiver is disabled.

FRAME LENGTH REGISTER

Having received a frame and read the status reqister, the received frame length can be read from the RFL register. The frame length is given as an eleven bit number and includes the 2 FCS bytes in the count. The reqister should be read before a receiver reset.

LOOPBACK

Bit D7 of the control register, the loopback bit is provided for testing purposes. When the bit is set high an internal connection is made between the transmitter output and receiver input. The main transmitter output (TX_{OP}) transmits IDLE (transmitted data is always available on T_{OP2}). The receiver is clocked from TCK. The loopback bit will respond to every write to the control register.

DIRECT MEMORY ACCESS (FIG.11)

All data transfers to or from memory are carried out by the DMA controller. Each time it receives a request from the transmitter or receiver it will carry out one DMA cycle, i.e. only one byte is transferred at a time. Clashes between transmitter and receiver are resolved in favour of the receiver, otherwise operation is on a first come, first served basis.

REGISTERS

Fig.7 shows the addresses for the various instruction and status registers. All registers are readable from and writable to except for S, C and RFL. The S and C registers have the same address, which one is accessed is determined by whether a read (status) or write (control) operation is carried out. Transmitter registers should not be written to when transmitting (except to ABORT a frame), likewise receiver registers should not be written to when receiving. The TA and RA registers update continuously during transmission and reception respectively, giving the next address to be read from or written to.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
LOOPBACK ENABLE	DON'T CARE	DON'T CARE	RECEIVE RESET	RECEIVE ENABLE	TRANSMIT RESET	TRANSMIT ABORT	TRANSMIT ENABLE

Figure 4: Control register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RECEIVED FRAME TOO LONG	RECEIVED OVERRUN FRAME	RECEIVED ABORT	RECEIVING FLAGS	RECEIVING IDLE	FREE TO RECEIVE	TRANS-MISSION ABORTED	TRANS-MITTING DATA

RECEIVE BITS — TRANSMIT BITS

Figure 5: Status register

Status Register								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Condition**
X	X	X	X	X	X	0	1	Currently transmitting data
X	X	X	X	X	X	0	0	Transmitter disabled, transmission COMPLETE (status read after an interrupt)
X	X	X	X	X	X	1	0	Transmitter disabled, transmission ABORTED (status read after an interrupt)
X	X	X	X	X	1	X	X	Receiver enabled, free to receive
X	X	X	0	0	X	X	X	Currently receiving data
X	X	X	0	1	X	X	X	Receiving IDLE
X	X	X	1	0	X	X	X	Receiving FLAGS
0	0	1	X	X	0	X	X	Receiver disabled, ABORTED frame received (status read after an interrupt)
0	1	0	X	X	0	X	X	Receiver disabled, OVERRUN frame received (status read after an interrupt)
1	0	0	X	X	0	X	X	Receiver disabled, TOO LONG frame received (status read after an interrupt)
1	1	0	X	X	0	X	X	Receiver disabled, VALID frame received (status read after an interrupt)

Figure 6: Status interrupt

Regisler	**Function**	**Length (Bits)**	**Address (Hex)**	**A3**	**A2**	**A1**	**A0**	**R/W**
TFL	Transmitter Frame Length LS Byte Transmitter Frame Length MS Byte	8 3	2 3	0 0	0 0	1 1	0 1	R/W R/W
TA	Transmitter Address LS Byte Transmitter Address MS Byte	8 8	6 7	0 0	1 1	1 1	0 1	R/W R/W
S	Status	8	9	1	0	0	1	R
C	Control	8	9	1	0	0	1	W
RFL	Receiver Frame Length LS Byte Receiver Frame Length MS Byte	8 3	A B	1 1	0 0	1 1	0 1	R R
RMFL	Receiver Maximum Frame Length LS Byte Receiver Maximum Frame Length MS Byte	8 3	C D	1 1	1 1	0 0	0 1	R/W R/W
RA	Receiver Address LS Byte Receiver Address MS Byte	8 8	E F	1 1	1 1	1 1	0 1	R/W R/W

Figure 7: Register addresses

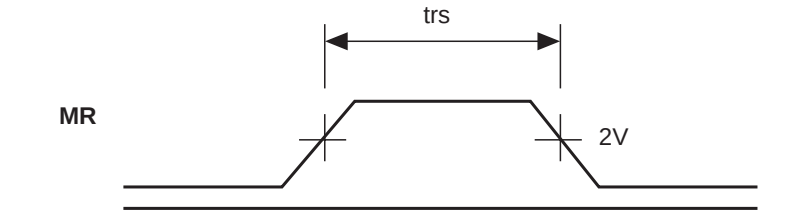

Figure 8(a)

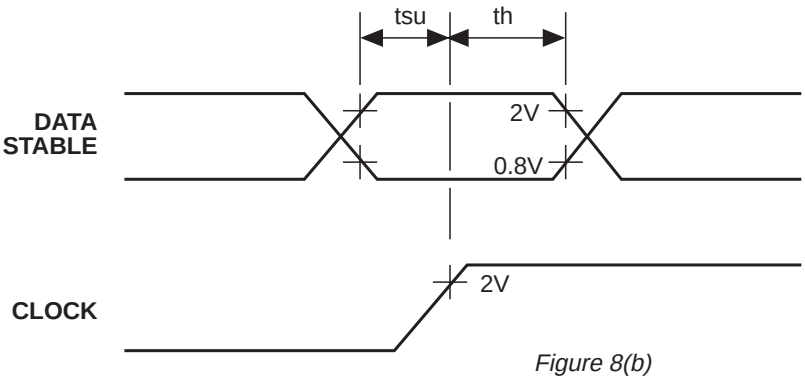

Figure 8(b)

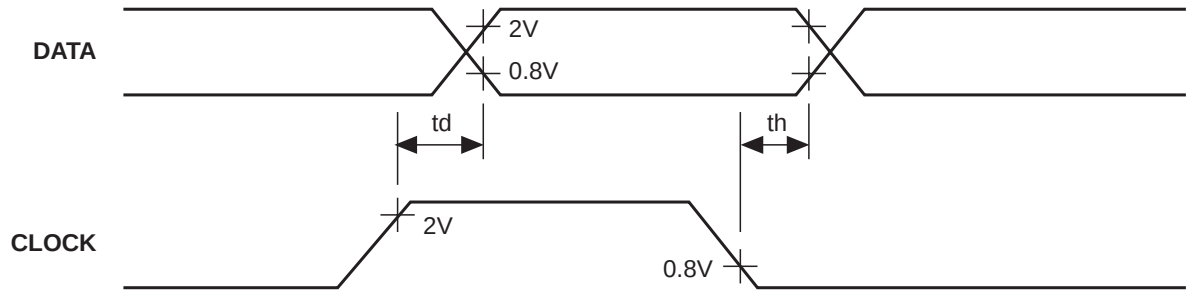

Figure 8(c)

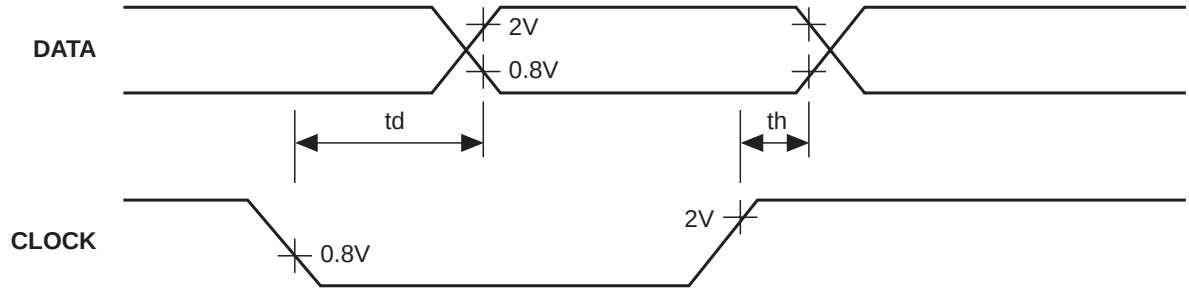

Figure 8(d)

Figure 8: Timing diagram

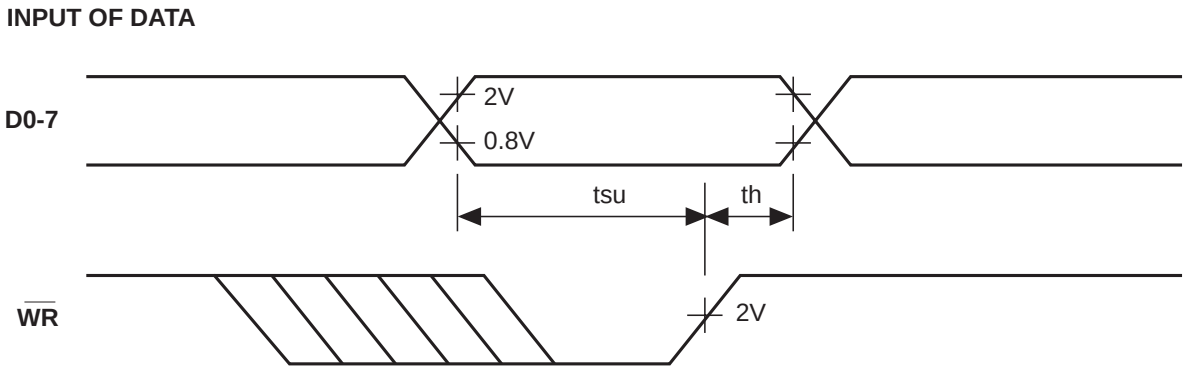

Figure 9(a)

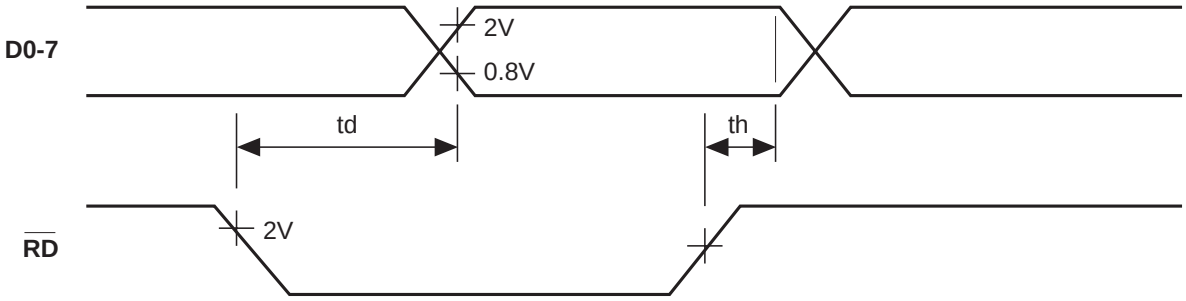

Figure 9(b)

Figure 9: Register timing

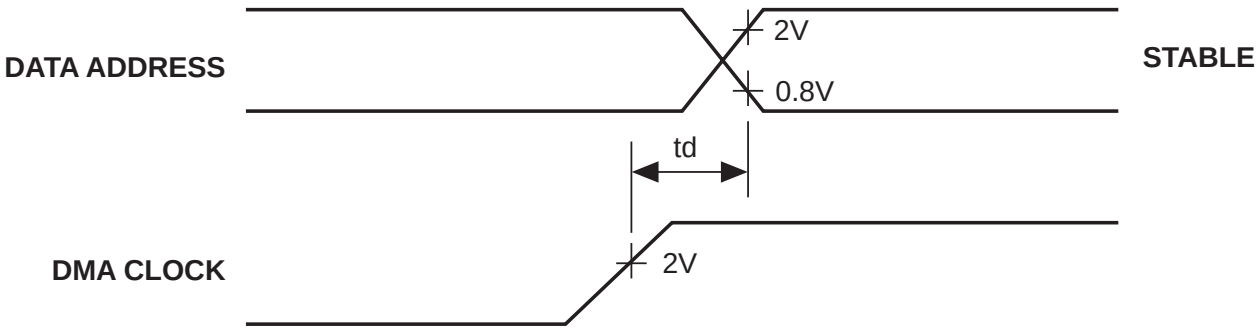

Figure 10: DMA timing

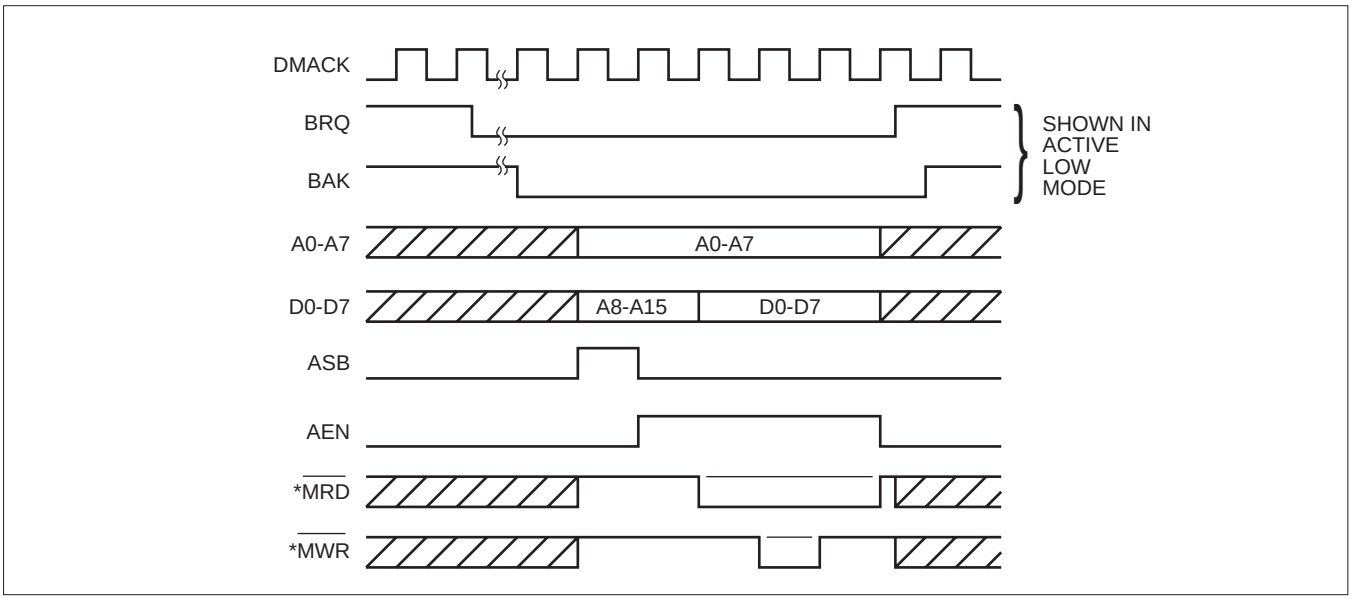

Figure 11: DMA cycle timing

*During a read cycle, $\overline{MWR}$ stays high and similarly during a write cycle $\overline{MRD}$ stays high. All other external signals are the same for both cycles.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.3V to 7.0V
Input voltage V_{IN}	-0.3V to V_{CC} +0.3V
Output voltage V_{OUT}	-0.3V to V_{CC} +0.3V
Clamp diode current per pin IK (See Note 2)	±18mA
Static discharge voltage	
Storage temperature Ts	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-40°C to +85°C

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied
2. Maximum dissipation of 1 second should not be exceeded, only one output to be tested at any one time

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless othetwise stated):

T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ±10%, Ground = 0V

STATIC CHARACTERISTICS

Characterislic	Symbol	Value			Unlts	Conditions
		Mln.	Typ	Max.		
Output high voltage	V_{OH}	V_{CC}-2			V	IOH = 0.8mA
Output low voltage	V_{OL}			0.4	V	I OL = 1 .6mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		+10	µA	GND ≤ V_{IN} ≤ V_{CC}
V_{CC} current	I_{CC}			1	mA	T_{amb} = -40°C to +85 °C
Output leakage current	I_{OZ}	-50		+50	µA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	15		80	mA	V_{CC} = Max

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum DMA clock frequency	FDMACK	8			MHz	
Maximum TX clock frequency	FTCK	128			kHz	
Maximum RX clock frequency	FRCK	128			kHz	
Minimum MR duration	t_{rs}				ns	Fig.8(a)
RXIP to RCK set-up time	t_{su}	0			ns	Fig.8(b)
RXIP to RCK hold time	t_h	90			ns	Fig.8(b)
BAK to DMACK set-up time	t_{su}	0			ns	Fig.8(b)
BAK to DMACK hold time	t_h	25			ns	Fig.8(b)
Delay DMA clock to $\overline{MRD}$	t_d		40	55	ns	Fig.8(c)
Delay DMA clock to $\overline{MWR}$	t_d		40	55	ns	Fig.8(c)
Delay RCK $\Downarrow$ to $\overline{RINT}$	t_d		50	110	ns	Fig.8(d)
Delay, TCK to $\overline{TINT}$	t_d		60	90	ns	Fig.8(c)
Delay, TCK $\Uparrow$ or RCK $\Downarrow$ to BRQ	t_d		70	90	ns	Fig.8(c) & (d)
Delay, DMACK to AEN	t_d		40	55	ns	Fig.8(c)
Delay, DMACK to ASB	t_d		40	55	ns	Fig.8(c)
Delay, TCK to TXoP	t_d		70	115	ns	Fig.8(c)
Delay, TCK to ToP2	t_d		60	115	ns	Fig.8(c)
Hold, DMACK to $\overline{MRD}$	t_h		90	130	ns	Fig.8(d)
Hold, DMACK to $\overline{MWR}$	t_h		50	75	ns	Fig.8(d)
Hold, DMACK to BRQ	t_h		60		ns	Fig.8(d)
Hold, DMACK to AEN	t_h		30	55	ns	Fig.8(d)
Hold, DMACK to ASB	t_h		40	55	ns	Fig.8(d)
Data to WR set-up	t_{su}				ns	Fig.9(a)
WR to data hold	t_h				ns	Fig.9(a)
RD to data delay	t_d		50		ns	Fig.9(b)
RD to data hold	t_h				ns	Fig.9(b)
DMACK to data/address delay	t_d		60		ns	Fig.10

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