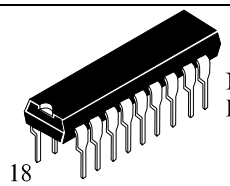
PULSE DIALER WITH REDIAL

KK5851

The KK5851 is a monolithic CMOS integrated circuit which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with 32 digit redial.

- Wide operating voltage range (2.0~6.0V)
- Low power dissipation
- Use either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard
- Make/Break ratio can be selected
- Redial with * or #
- Continuous MUTE
- Power up clear circuitry on chip
- 10 pps/20 pps can be selected

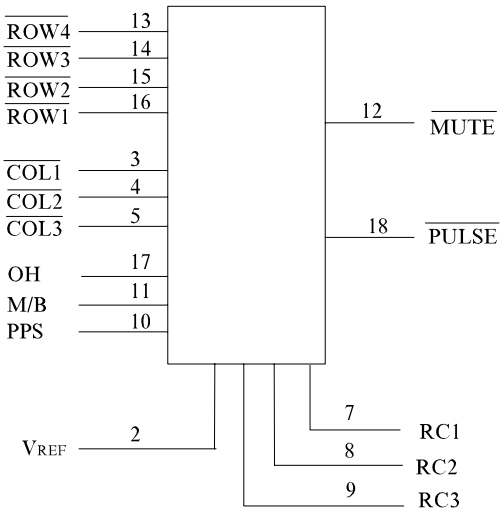


ORDERING INFORMATION

KK5851N Plastic

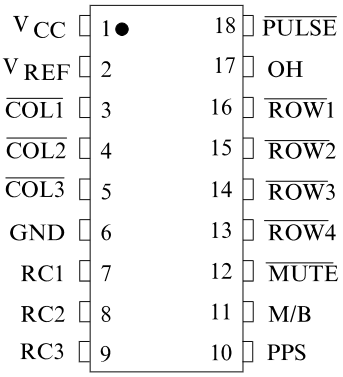
T_A = -20° to 70° C

LOGIC DIAGRAM

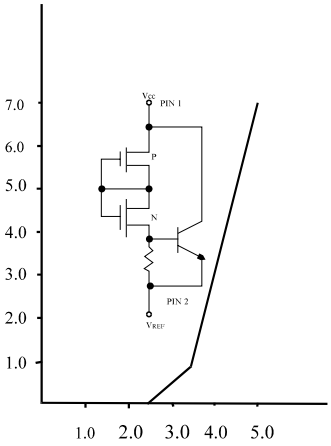
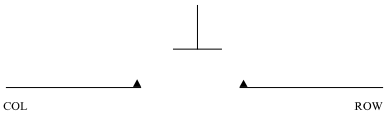
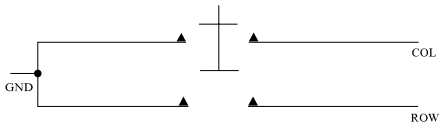
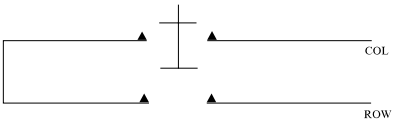
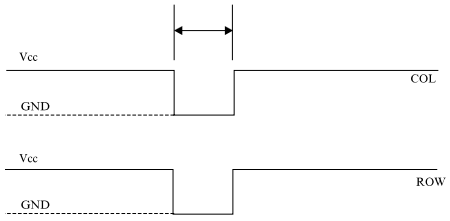


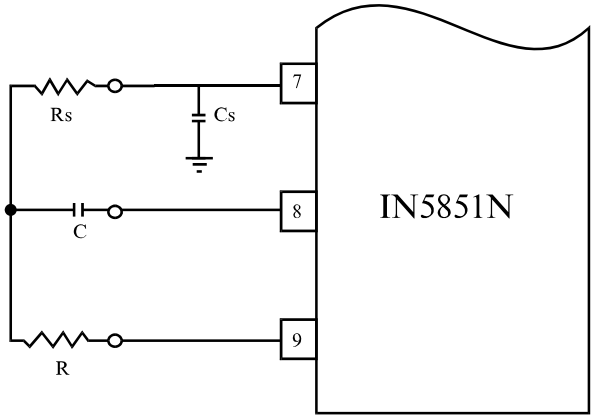
PIN 1 = V_{CC}
PIN 6 = GND

PIN ASSIGNMENT



PIN DESCRIPTION

NAME	PIN	DESCRIPTION
V_{CC}	1	Positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage should be regulated to less than 6.0 volts using on external form or regulation.
V_{REF}	2	The V_{REF} output provides reference voltage that tracks internal parameters of the KK5851N. V_{REF} provides a negative voltage reference to the V_{CC} supply. Its magnitude will be approximately 0.6 volt higher than the minimum operating voltage of each particular KK5851N. The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{CC} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). with this amount of supply current, operation of the KK851N is guaranteed. The internal circuit of the V_{REF} function is shown in Figure 1 with its associated I-V characteristic . 
Row1-Row4, Col1-Col4	3,4,5,13, 14,15,16	Keyboard inputs. The KK5851N incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used. A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are scanned alternately (pulled high, then low) to verify the varied input. The input must remain valid for 10msec of debounce time to be accepted. Form A type keyboard  2 of 7 keyboard (negative common)  2 of 7 keyboard  Electronic input 
GND	6	Negative supply

		pin is connected to the common part in general applications.
RC1-RC3	7,8,9	Oscillator The KK5851N contains on-chip inverters to provide oscillator which will operate with a minimum external components. Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ration $K=R_S/R$ equal to 10 The oscillator period is given by: $T=RC(1.386+(3.5KC_S)/C-(2K/(K+1))$ in $(K/(1.5K + 0.5))$ Where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with this capacitance minimized. 
PPS	10	10/20pps Select Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps. Connecting the pin V_{CC} (pin 1) will select an output pulse rate of 20pps.
M/B	11	Make/break Select The Make/Break pin controls the Make/Break ratio of the pulse output. The make/Break ratio is controlled by connection V_{CC} or GND to this pin as shown in the following table.

Input	Make	Break
V_{CC} (Pin1)	33.4%	66.6%
GND(PIn 6)	40%	60%

$\overline{\text{Mute}}$	12	Mute Output The mute output is an open-drain N-Channel transistor designed to drive external bipolar transistor. This circuitry is usually used to mute the receiver during outpulsing. As shown in Fig. 2 the KK5851N mute output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break. The delay from the end of the last break until the mute output turns off is mute overlap and is specified as t_{MO}.
OH	17	ON-HOOK/TEST This pin detects the state of the hook switch contact “OFF HOOK” corresponds to V_{SS} condition. ÖN HOOK”corresponds to V_{DD} condition. When outpulsing in this mode, which can be up to 300msec, is completed, the circuit is deactivated and will require current only necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications). Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the

		number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.
$\overline{\text{PULSE}}$	18	Pulse Output The Pulse output is an open drain N-channel transistor designed to drive external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KK5851N pulse output is an open circuit during make and pulls to the GND supply during break.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.3 to +6.2	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.3 to V_{CC} +0.3	V
P_D	Power Dissipation in Still Air **	500	mW
Tstg	Storage Temperature	-40 to +125	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
** Derating: -10 $^{mW}/_{°C}$ from 65°C to 70°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature	-20	+70	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND, V_{CC} = 2.0 V to 6.0V, T_A = -20 to +70°C, F_{OSC}=2.4KHz)

Symbol	Parameter	Test Conditions	Guaranteed Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		$0.8V_{CC}$		V_{CC}	V
V_{IL}	Input Low Voltage		0		$0.2V_{CC}$	V
V_{DR}	Minimum Memory Retention Voltage		1.0			V
I_{OL}	Output Leakage Current	V_{CC}=6.0V , MUTE,PULSE=6.0V			1	µA
I_{OL1}	Minimum Output current (MUTE,PULSE)	V_O=0.8V,V_{CC}=2.5V	0.5			mA
I_{OL2}	Minimum Output current (MUTE,PULSE)	V_O=0.8V,V_{CC}=3.5V	1.7			mA
I_{OD}	Operating Current	All output under no load, V_{CC}=2.0V			150	µA
I_{SD}	Maximum Standby Current	V_{CC}=2.5V V_{IH}=2.5V			1	µA
I_{REF}	Minimum Reference Current	V_{CC}=6.0V	1			µA

AC ELECTRICAL CHARACTERISTICS (F_{OSC}= 2.4 KHz, V_{CC}=2.0 to 6.0 V, T_A=-20 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min.	Typ.	Max	
T_{KD}	Minimum Valid Key Entry Time		20			mS
T_{OH}	On Hook Time Required to Clear Memory (Figure 2)		300			mS
T_{IDR}	Inter Digital Pause (Figure 2)			800		mS
Δf	Frequency Sability			±10		%
T_{MO}	Recovery Time, MUTE to PULSE (Figure 2)			800		mS
T_{PDP}	Maximum Pre-digital Pause (Figure 2)				30	mS
T_{DP}	Maximum Delay Time, Key Input to PULSE (Figure 2)				50	mS
M/B	Make/Break Ratio			1/2		M/B=V_{CC}
				2/3		M/B=GND

TIMING DIAGRAMM

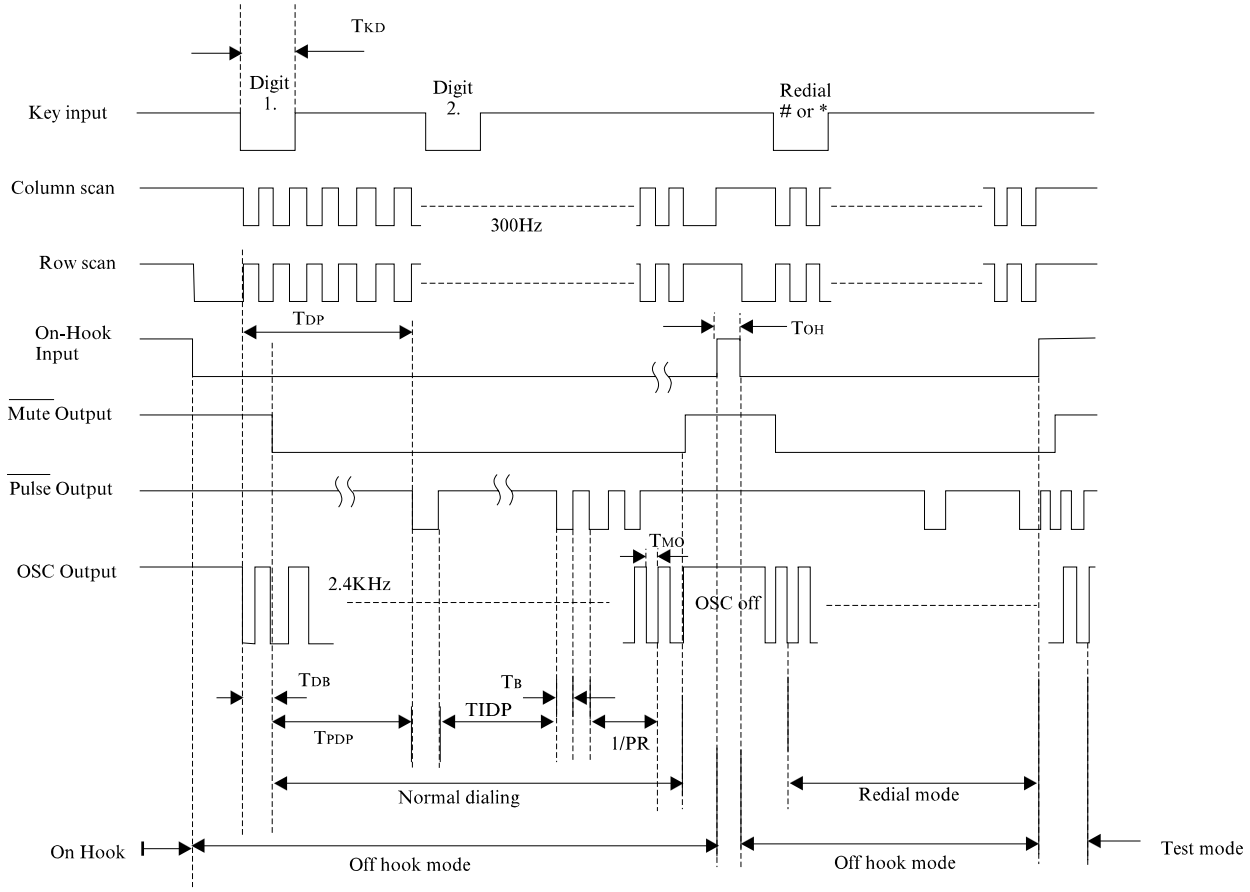
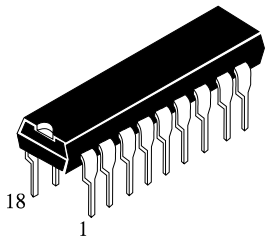
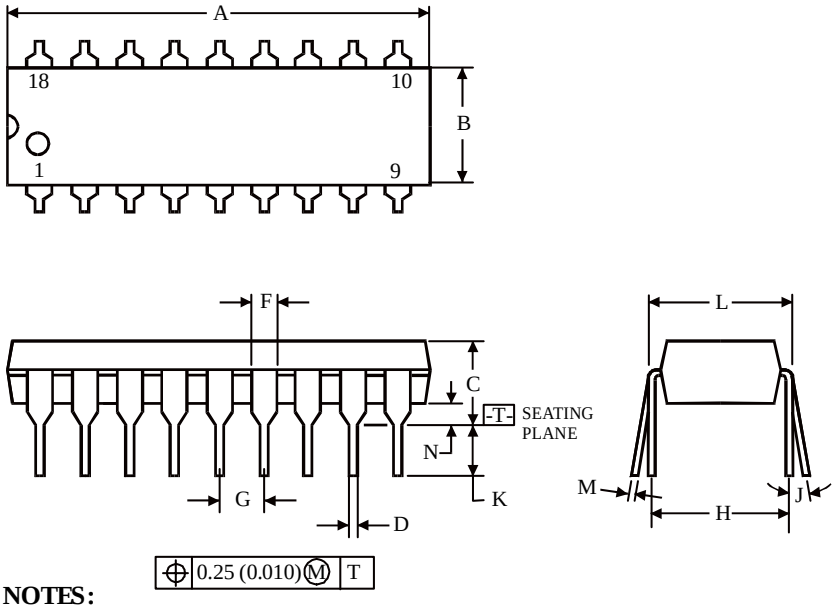


Figure 2

N SUFFIX PLASTIC DIP
(MS - 001AC)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	22.35	23.37
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.