MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet

TMOS IV N-Channel Enhancement-Mode

Power Field Effect Transistor
DPAK for Surface or Insertion Mount

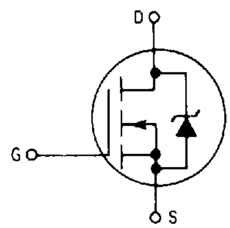
MTD3055E

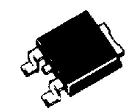
Motorola Preferred Device

TMOS POWER FET
8 AMPERES
$R_{DS(on)}$ = 0.15 OHM
60 VOLTS

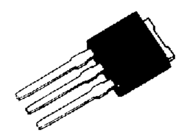
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.
- Available With Long Leads, Add -1 Suffix





CASE 369A-10
TO-252
MTD3055E



CASE 369-06
TO-251
MTD3055E1

Preferred device is a Motorola recommended choice for future use and best overall value.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MTD3055E	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W
Maximum Device Temperature for Soldering Purposes (for 5 seconds maximum)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 80	μA

(1) These ratings are applicable when surface mounted on the minimum pad size recommended

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)				
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$R_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 1.3 1	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)	g_{FS}	3.5	—	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY				
Unclamped Inductive Switching Energy See Figures 16 and 17 (I_D = 20 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 8 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 3.2 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)	W_{DSR}	 — — —	 3 10 4	mJ

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	100	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 18	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	65	
Fall Time		t_f	—	65	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 15	Q_g	12 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	6.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5.5 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_{FM} = 0.5 Rated I_D, dI_S/dt = 100 A/μs, V_{GS} = 0)	V_{SD}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	50 (Typ)	90	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

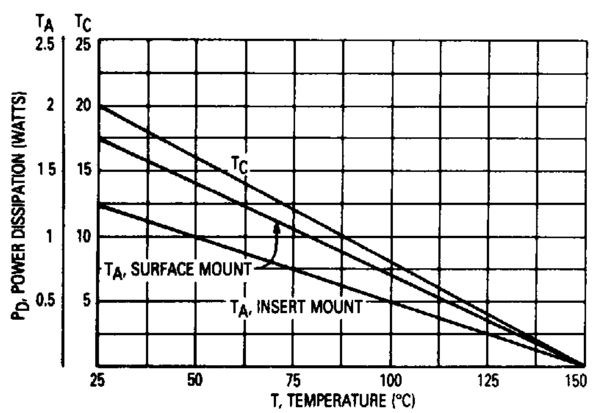


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

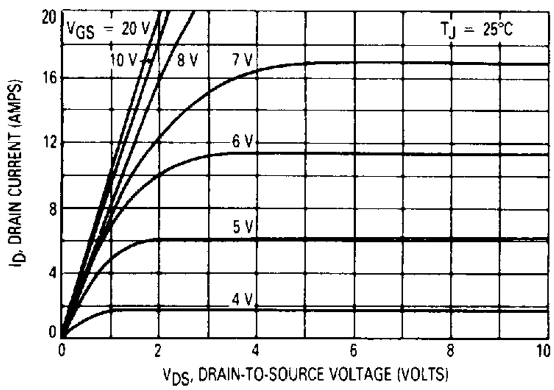


Figure 2. On-Region Characteristics

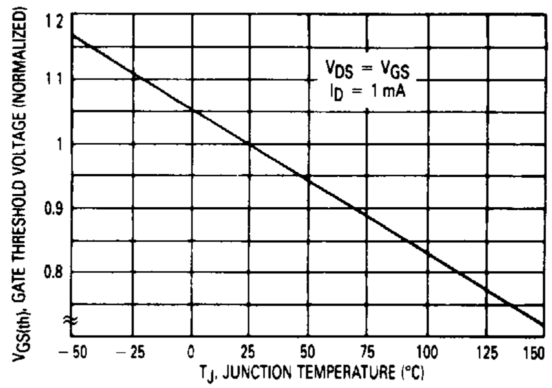


Figure 3. Gate-Threshold Voltage Variation With Temperature

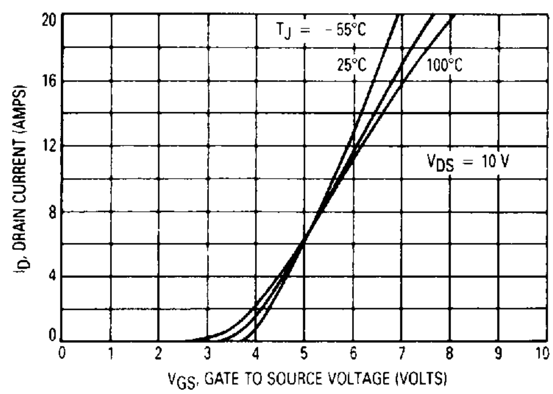


Figure 4. Transfer Characteristics

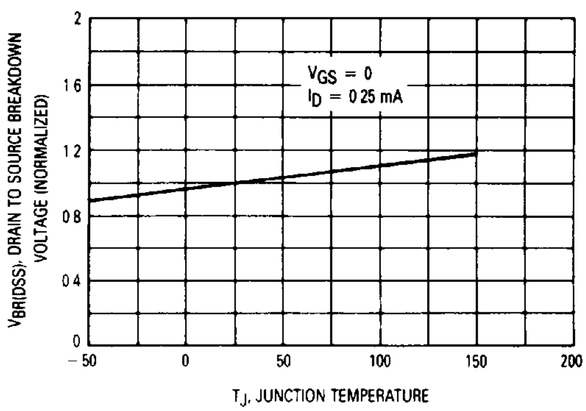


Figure 5. Breakdown Voltage Variation With Temperature

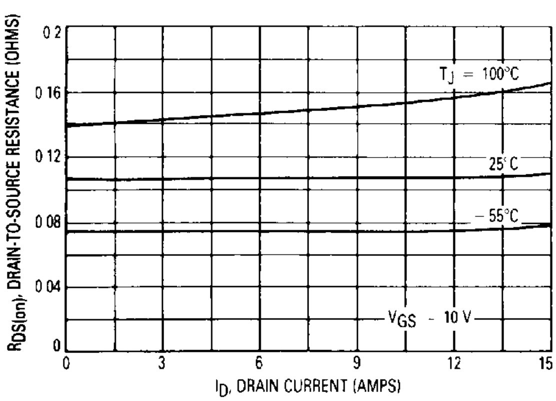


Figure 6. On-Resistance versus Drain Current

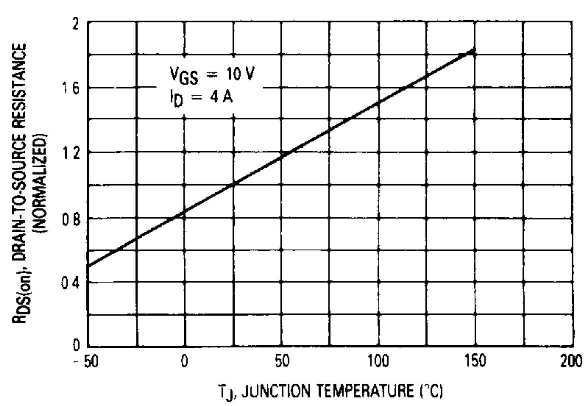


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

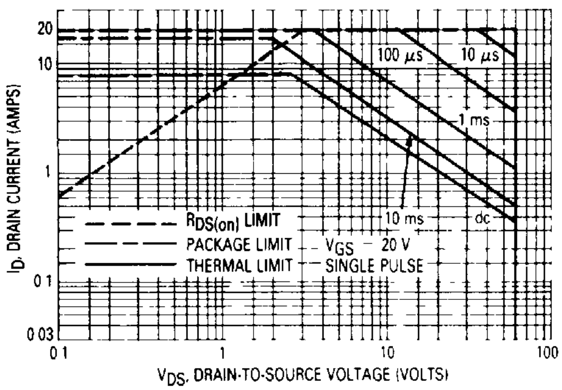


Figure 8. Maximum Rated Forward Biased Safe Operating Area

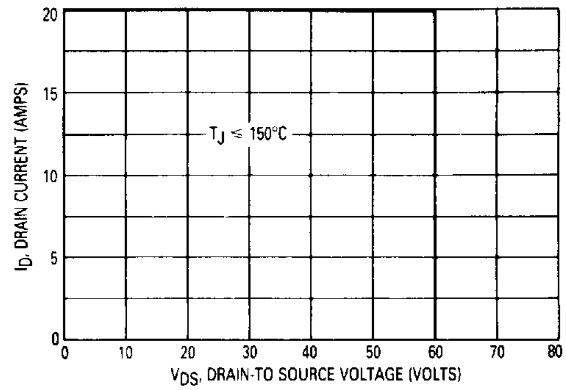


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

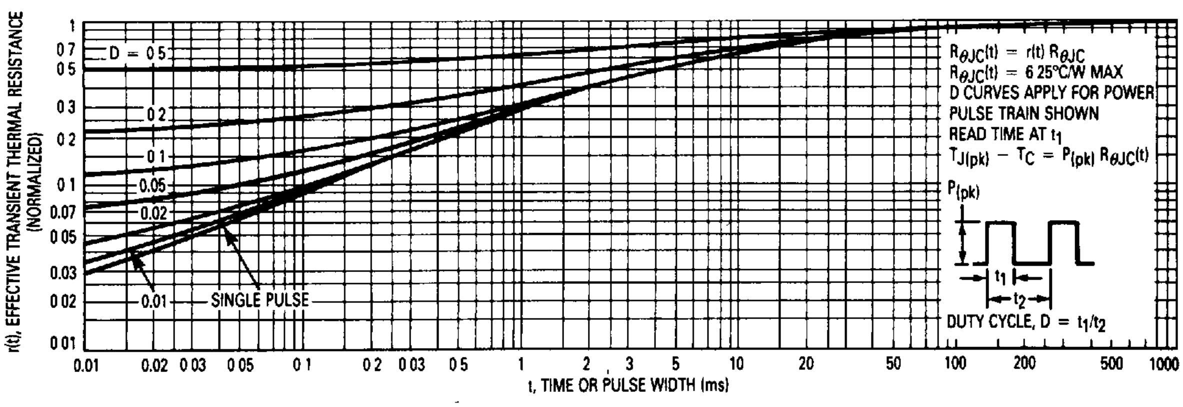


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

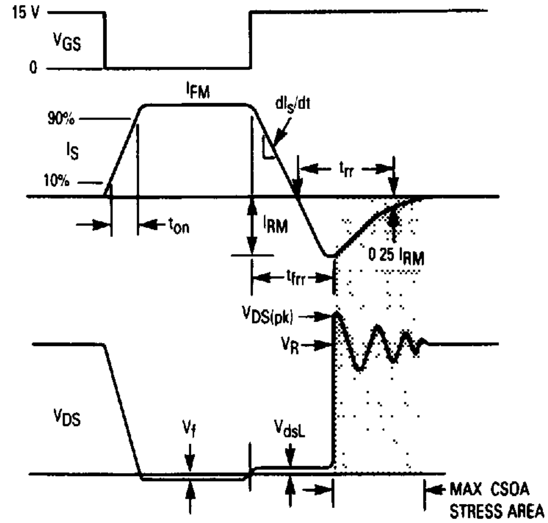


Figure 11. Commutating Waveforms

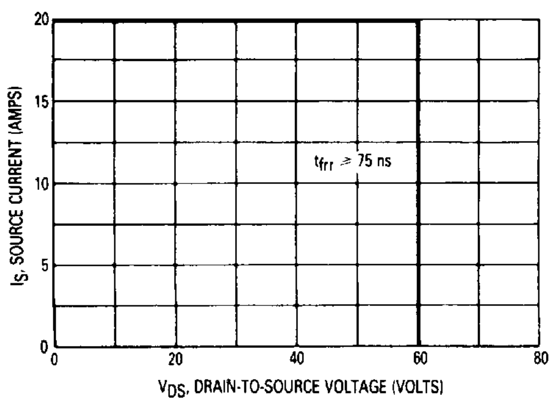


Figure 12. Commutating Safe Operating Area (CSOA)

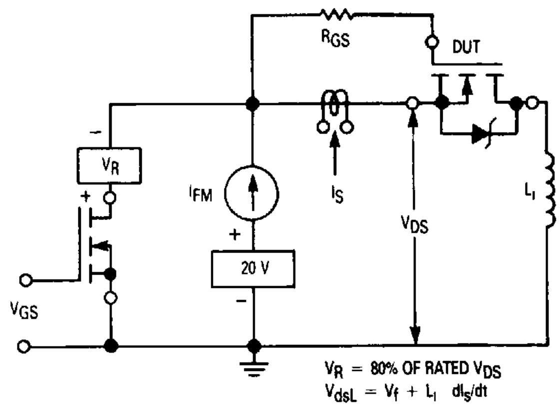


Figure 13. Commutating Safe Operating Area Test Circuit

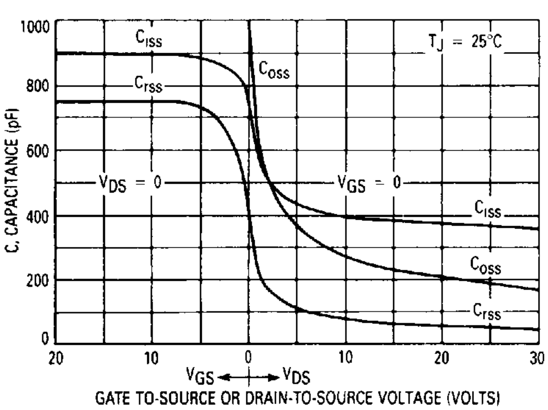


Figure 14. Capacitance Variation

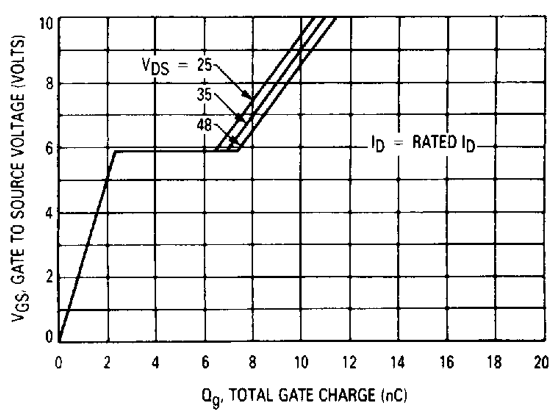


Figure 15. Gate-Charge versus Gate-to-Source Voltage

3

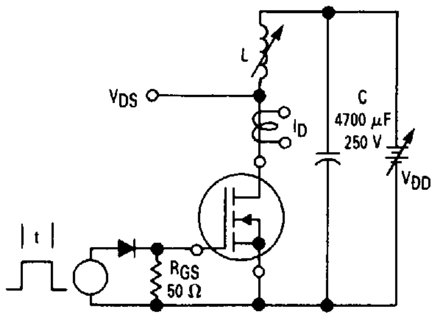
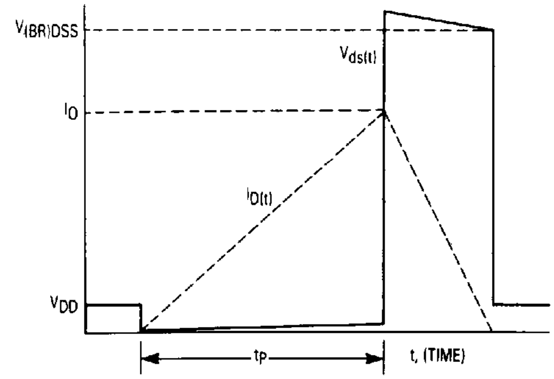


Figure 16. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING

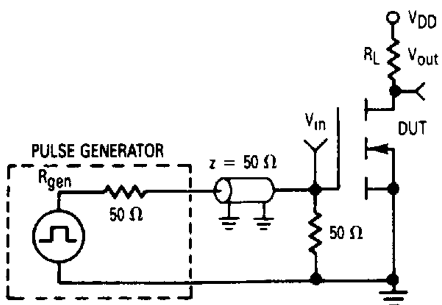


Figure 18. Switching Test Circuit

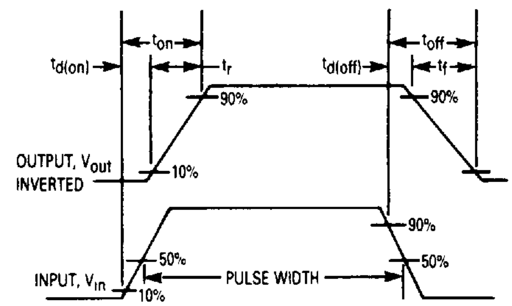


Figure 19. Switching Waveforms