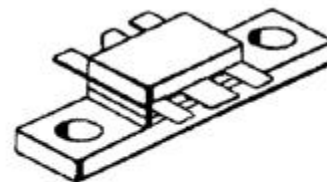


MS1454

RF AND MICROWAVE TRANSISTORS 806-960 MHZ CELLULAR BASE STATIONS

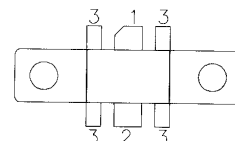
Features

- Gold Metallization
- Diffused Emitter Ballasting
- Internal Input Matching
- Designed for Linear Operation
- High Saturated Power Capability
- Common Emitter Configuration
- P_{OUT} 30 W MIN
- Gain 7.5 dB
- Efficiency 55% (Typ)
- 20:1 VSWR
- Overdrive Survivability 5 dB



.230 6LFL (M142)
epoxy sealed

PIN CONNECTION



1. Collector 3. Base
2. Emitter

DESCRIPTION:

The MS1454 gold/metallized epitaxial silicon NPN planar transistor uses diffused emitter ballast resistors for high linearity class AB operation in cellular base station applications.

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	48	V
V_{CEO}	Collector-Emitter Voltage	25	V
V_{EBO}	Emitter-Base Voltage	3.5	V
P_{DISS}	Total Power Dissipation	88	W
I_C	Collector Current	7.5	A
T_j	Junction Temperature	+200	$^{\circ}C$
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

THERMAL DATA

$R_{TH(j-c)}$	Junction-Case Thermal Resistance	2	$^{\circ}C/W$
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ELECTRICAL SPECIFICATIONS (T_{case} = 25°C)
STATIC

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CES}	I_C = 100 mA	48	55	---	V
BV_{EBO}	I_E = 10 mA	3.5	5	---	V
BV_{CEO}	I_C = 40 mA	25	28	---	V
BV_{CER}	I_E = 40 mA R_{BE} = 100 Ω	30	40	---	V
I_{CBO}	V_{CE} = 24 V	---	---	---	mA
h_{FE}	V_{CE} = 20 V I_C = 2 A	15	40	100	---

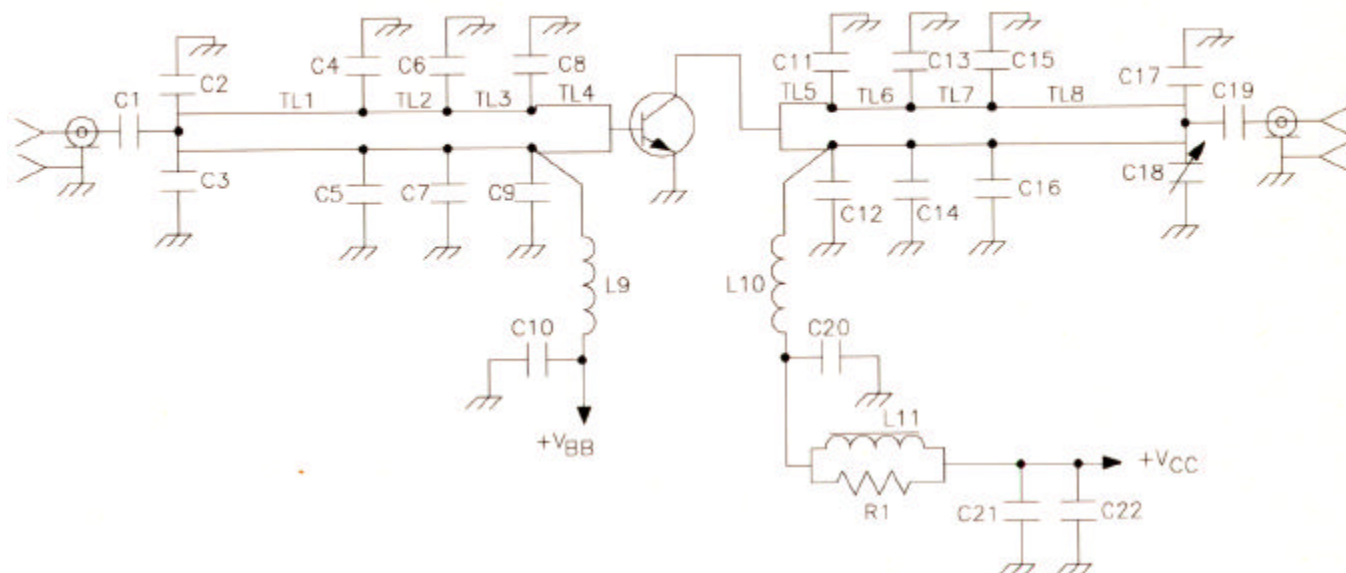
DYNAMIC

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	f = 860 MHz I_{CQ} = 60 mA V_{CE} = 25 V	30	---	---	W
η_C	f = 860 MHz I_{CQ} = 60 mA V_{CE} = 25 V	---	55	---	%
G_P	f = 860 MHz I_{CQ} = 60 mA V_{CE} = 25 V	7.5	9	---	DB
C_{OB}	V_{CB} = 25 V f₀ = 1 MHz	---	42	---	pF
IMD₃	P_{OUT} = 30 W PEP f₁ = 860.0 MHz f₂ = 860.1 MHz	---	-35	---	dBc
VSWR₁	VSWR = 20:1 V_{CE} = 25 V VSWR = 10:1 V_{CE} = 25 V ± 20%	NO DEGRADATION IN OUTPUT DEVICE			Typ.
VSWR₂	VSWR = 5:1 V_{CE} = 25 V ± 20% P_{IN} = P_{IN} (norm) + 3 dB	NO DEGRADATION IN OUTPUT DEVICE			Typ.
OVD	P_{IN}(norm) = +5dB V_{CE} = 25 V P_{IN}(norm) = +5dB V_{CE} = 25 V ± 20%	NO DEGRADATION IN OUTPUT DEVICE			Typ.

IMPEDANCE DATA

Freq.	$Z_{IN} (\Omega)$	$Z_{CL} (\Omega)$
800 MHz	$4.3 + j 5.8$	$3.5 + j 0.2$
830 MHz	$3.2 + j 6.1$	$3.5 + j 0.1$
860 MHz	$3.5 + j 7.1$	$2.9 - j 0.2$
900 MHz	$5.3 + j 6.4$	$2.0 - j 0.6$
915 MHz	$6.1 + j 6.3$	$3.2 - j 0.7$
930 MHz	$9.4 + j 6.3$	$3.2 - j 1.1$
945 MHz	$6.6 + j 3.0$	$3.3 - j 1.2$
960 MHz	$5.9 + j 1.0$	$3.4 - j 1.5$

TEST CIRCUIT

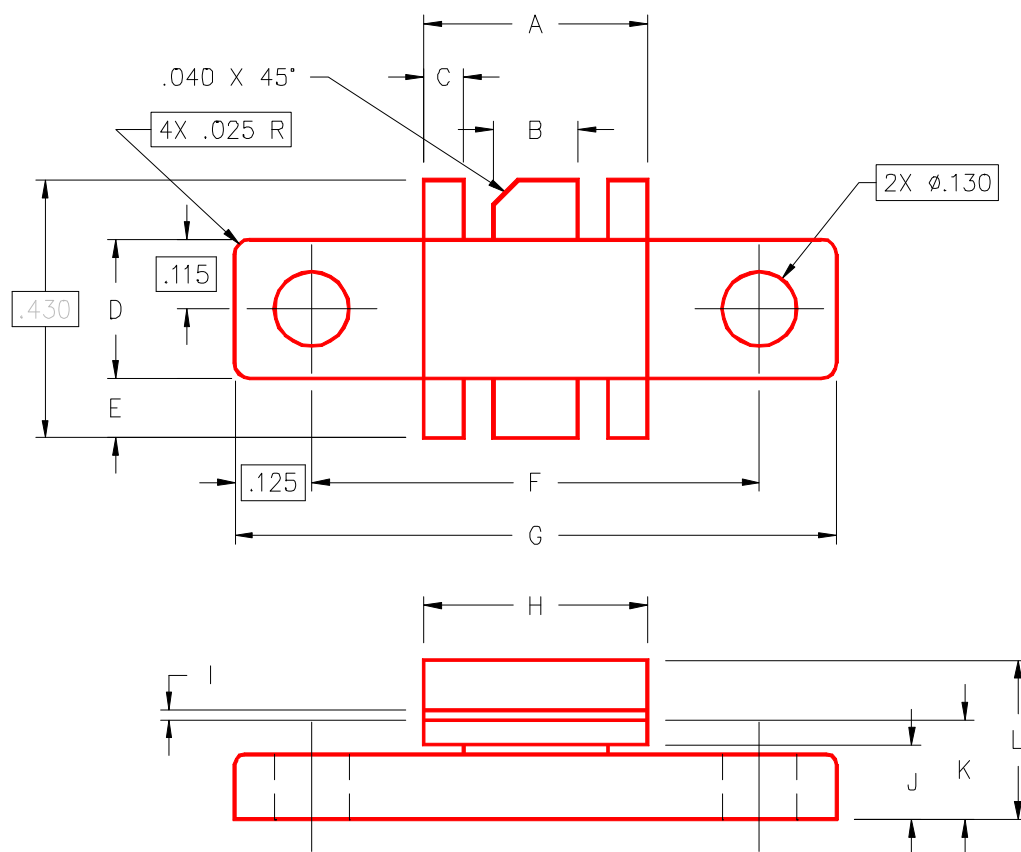


C1, C19 : 33pF ATC 100B Chip Capacitor
 C2, C15 : 3.6pF ATC 100B Chip Capacitor
 C3 : 4.5pF ATC 100B Chip Capacitor
 C4, C16 : 5.0pF ATC 100B Chip Capacitor
 C5 : 2.9pF ATC 100B Chip Capacitor
 C6, C7 : 1.8pF ATC 100B Chip Capacitor
 C8, C9 : 6.2pF ATC 100B Chip Capacitor
 C10, C22 : 300pF ATC 100B Chip Capacitor
 C11, C12

C18 : .5 - 6.0pF Gigatrim Adjustable Capacitor
 C20 : 10pF ATC 100B Chip Capacitor
 C21 : 10 μ F (50V) Electrolytic Capacitor
 L9 : 4 Turns (tight) I.D. 120mil ENAM Cu 20 AWG
 L10 : 4 Turns (tight) I.D. 158mil ENAM Cu 18 AWG
 L11 : 1.5 Turns VK-200 Ferrite H.F. Choke
 TL1, TL8 : 964 x 85.69 mils (50 Ω /36.84")
 TL2, TL3 : 352 x 85.69 mils (50 Ω /13.46")
 TL4 : 222 x 109.03 mils (42.6 Ω /8.56")
 TL5 : 149 x 109.03 mils (42.6 Ω /5.74")
 TL6 : 334 x 85.69 mils (50 Ω /12.75")

PACKAGE MECHANICAL DATA

PACKAGE STYLE M142



	MINIMUM INCHES/MM	MAXIMUM INCHES/MM		MINIMUM INCHES/MM	MAXIMUM INCHES/MM
A	.355/9,02	.365/9,27	I	.004/0,10	.006/0,15
B	.115/2,92	.125/3,18	J	.120/3,05	.130/3,30
C	.075/1,91	.085/2,16	K	.160/4,06	.180/4,57
D	.225/5,72	.235/5,97	L	.230/5,84	.260/6,60
E	.090/2,29	.110/2,79			
F	.720/18,29	.730/18,54			
G	.970/24,64	.980/24,89			
H	.355/9,02	.365/9,27			