



MP7651

8-Channel, Voltage Output
10 MHz Input Bandwidth 8-Bit Multiplying
DACs with Serial Digital Data Port
and Chip Select Decoder

FEATURES

- 8 Independent 2-Quadrant Multiplying 8-Bit DACs
- Serial Digital Input Data and Address Port (3-Wire Standard) plus Internal Chip Address Decoder©
- Dual Supplies (± 5 V typ.)
- High Speed:
 - 12.5 MHz Digital Clock Rate
 - V_{REF} to V_{OUT} Settling Time: 150ns to 8-bit (typ)
 - Voltage Reference Input Bandwidth: 10 MHz (typ)
- Low Power: 150mW (typ)
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ± 0.8 LSB, INL = ± 1 LSB (typ)
- DACs Matched to $\pm 0.5\%$ (typ)
- Low Harmonic Distortion: 0.25% typical with $V_{REF} = 1$ V p-p @ 1 MHz
- $V_{REF}/2$ Output Preset Level
- Latch-Up Proof
- Greater than 2000 V ESD Protection

APPLICATIONS

- ATE
- Process Control (Low Noise)
- Convergence Adjustment for High Resolution Monitors (Work Stations)
- Digital Gain/Attenuation/Offset Control
- Trimmer Replacement

GENERAL DESCRIPTION

The MP7651 is ideal for direct gain control of video, composite video, CCD and other high frequency analog signals. The device includes 8-channels of high speed, high bandwidth, two quadrant, multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving ± 1 mA (typ) to a load. DNL of better than ± 0.8 LSB is achieved with a channel-to-channel matching of better than 0.5%. Stability, matching, and precision of the DACs is achieved by using EXAR's thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 10 MHz (typ),

fast output settling time, and V_{REF} feedthrough isolation of -65 dB or better. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal.

A specified and constant input impedance of each V_{REF+} input gives flexibility for optimal system design. The serial data 3-wire standard μ -processor logic interface reduces pin count, package size (28 pin), and board wire (space). Additionally, the internal chip select decoder allows for easy daisy chaining without the addition of separate control logic.

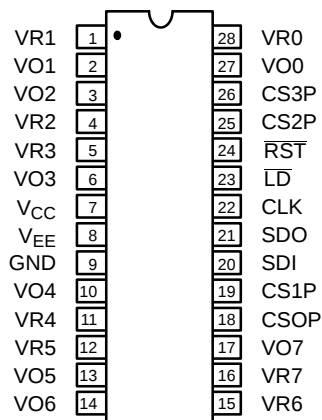
MP7651 is fabricated on a junction isolated, high speed, dual metal, linear compatible BiCMOS (BiCMOS IVTM) thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

The diagram illustrates the internal architecture of the CS3P DAC module. It features a 16-bit shift register that receives data from the SDI input through a 1-bit latch. The shift register's output is split into two paths: one leading to a 4-bit decoder (4-8 DEC) and another to a 4-bit counter (COMP). The decoder's output is used to address an 8-bit DAC, which is also controlled by an 8-bit latch. The DAC's output is then passed through a +1 incrementer to produce the final output voltage (e.g., VO0, VO1, ..., VO7). The module is controlled by a reset signal (RST) and a clock signal (CLK). The LD signal is used to enable the 3-state buffer (SDO) and to control the DAC's output. The module is powered by VCC and VFF, and grounded at GND.

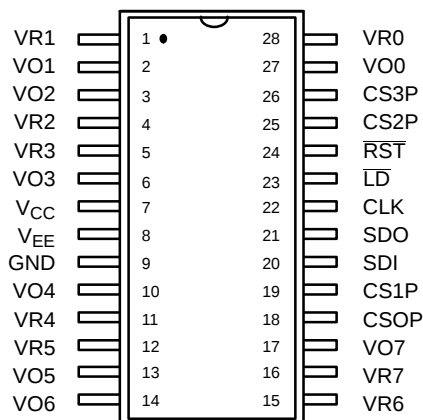
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	-40 to +85°C	MP7651AS	±1	±0.8	±1.5
Plastic Dip	-40 to +85°C	MP7651AN	±1	±0.8	±1.5

PIN CONFIGURATIONS

See Packaging Section for
Package Dimensions



**28 Pin PDIP (0.300")
NN28**



**28 Pin SOIC (EIAJ, 0.335")
R28**

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	VR1	DAC 1 Reference Input
2	VO1	DAC 1 Output
3	VO2	DAC 2 Output
4	VR2	DAC 2 Reference Input
5	VR3	DAC 3 Reference Input
6	VO3	DAC 3 Output
7	V _{CC}	Positive Supply
8	V _{EE}	Negative Supply
9	GND	Ground
10	VO4	DAC 4 Output
11	VR4	DAC 4 Reference Input
12	VR5	DAC 5 Reference Input
13	VO5	DAC 5 Output
14	VO6	DAC 6 Output
15	VR6	DAC 6 Reference Input

PIN NO.	NAME	DESCRIPTION
16	VR7	DAC 7 Reference Input
17	VO7	DAC 7 Output
18	CSOP	Chip Select Bit 0 (LSB)
19	CS1P	Chip Select Bit 1
20	SDI	Serial Data/Address Input
21	SDO	Serial Data Output
22	CLK	Shift Register Clock
23	$\overline{LD}$	Load Signal; Load Data to Selected DACs
24	$\overline{RST}$	Reset Signal; Reset all DACs to V _{REF/2}
25	CS2P	Chip Select Bit 2
26	CS3P	Chip Select Bit 3 (MSB)
27	VO0	DAC 0 Output
28	VR0	DAC 0 Reference Input

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Noted: $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ and -3 V , $V_{REF} = 3\text{ V}$ and -3 V , $T = 25^\circ\text{C}$,
Output Load = Open

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	FSR = Full Scale Range (1)
Differential Non-Linearity	DNL			+0.8		+1	LSB	
Integral Non-Linearity	INL			+1		+1	LSB	
Monotonicity		Guaranteed			Guaranteed			
Gain Error	GE			+1.5		+1.5	% FSR	
Zero Scale Offset	Z _{OFS}		+20	+75		+75	mV	
Output Drive Capability	I _O		+1				mA	
REFERENCE INPUTS								
Impedance of V _{REF}	REF	6	12	18	6	18	kΩ	Max Swing is AGND ±3 V
Voltage Range	V _R	V _{EE} +1.5		V _{CC} −1.8		V	V _{REF}	
DYNAMIC CHARACTERISTICS ²								
Input to Output Bandwidth			10				MHz	R _L = 5 k, C _L = 20 pF V _R = 1.6 V p–p, R _L = 5k to V _{EE} V _R = 1.6 V p–p, R _L = 5k to V _{EE} V _{OUT} =50mV p-p above code 16
Input to Output Settling Time ⁵			150				ns	
Small Signal Voltage Reference	f _{tr}		10				MHz	
Input to Output Bandwidth								V _{OUT} =50mV p-p for all codes
Small Signal Voltage Reference	f _{tr}	5	8				MHz	
Input to Output Bandwidth								V _R =0 to V _R = 3V Step (6) to 1 LSB ZS to FS to 1 LSB
Voltage Settling from V _{REF} to V _{DAC} Out	t _{sr}		275	300		325	ns	
Voltage Settling from Digital Code to V _{DAC} Out	t _{sd}		275	300		325	ns	
V _{REF} Feedthrough	F _{DT}		−65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T _{HD}		0.5				%	V _{REF} =1MHz Sine 3V p-p @ 1 MHz, single channel CLK to V _{OUT} Δ V = ±5%
Channel-to-Channel Crosstalk	C _T		−75				dB	
Digital Feedthrough	Q			1			nVs	
Power Supply Rejection Ratio	PSRR			0.02			%/%	
POWER CONSUMPTION								
Positive Supply Current	I _{CC}		15	25		30	mA	V _{REF} = 0 V
Negative Supply Current	I _{EE}		15	25		30	mA	V _{REF} = 0 V
Power Dissipation	P _{DISS}		150	250		300	mW	V _{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High ³	V _{IH}	2.4			2.4		V	
Logic Low ³	V _{IL}			0.8		0.8	V	
Input Current	I _L			±10		±10	μA	
Input Capacitance ²	C _L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C			Tmin to Tmax		Units	Conditions
		Min	Typ	Max	Min	Max		
DIGITAL TIMING SPECIFICATIONS ^{2, 4}								
Input Clock Pulse Width	t _{CH} , t _{CL}	40			50		ns	
Data Setup Time	t _{DS}	10			10		ns	
Data Hold Time	t _{DH}	15			15		ns	
CLK to SDO Propagation Delay	t _{PD}			40		50	ns	
DAC Register Load Pulse Width	t _{LD}	100			100		ns	
Reset Pulse Width	t _{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t _{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t _{CKLD2}	0			0		ns	
Load Falling Edge to SDO	t _{HZ1}	50			60		ns	
3-state Enable								
Load Rising Edge to SDO	t _{HZ2}	35			50		ns	
3-state Disable								
Load Falling Edge to CLK Disable	t _{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t _{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t _{LDSU}	15			20		ns	
CS0-CS3 Set-Up Time with Respect to $\overline{LD}$	t _{CSLD}	25			35		ns	

NOTES:

- 1 Full Scale Range (FSR) is 3V.
- 2 Guaranteed but not production tested.
- 3 Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- 4 See Figures 2 and 3.
- 5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

V_{CC} to GND	+6.5 V	Maximum Junction Temperature	150°C
V_{EE} to GND	−6.5 V	Storage Temperature	−65°C to +150°C
V_{Ri} to GND	V_{CC} to V_{EE}	Lead Temperature (Soldering, 10 sec)	+300°C
V_{Oi} to GND	V_{CC} to V_{EE}	Package Power Dissipation Rating @ 75°C	
Digital Input & Output Voltage to GND	GND −0.5 to V_{CC} +0.5 V	PDIP, SOIC	1000mW
Operating Temperature Range		Derates above 75°C	6mW/°C
Extended Industrial	−40°C to +85°C		

NOTES:

- 1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.

APPLICATIONS INFORMATION

Refer to Section 8 for Applications Information

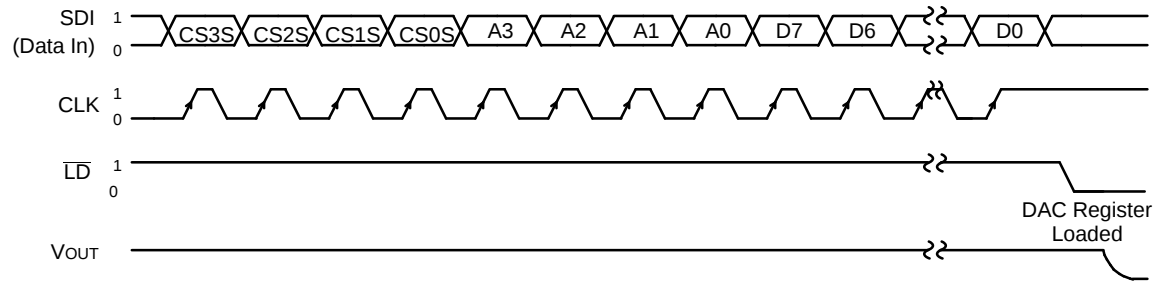


Figure 1. Serial Data Timing and Loading

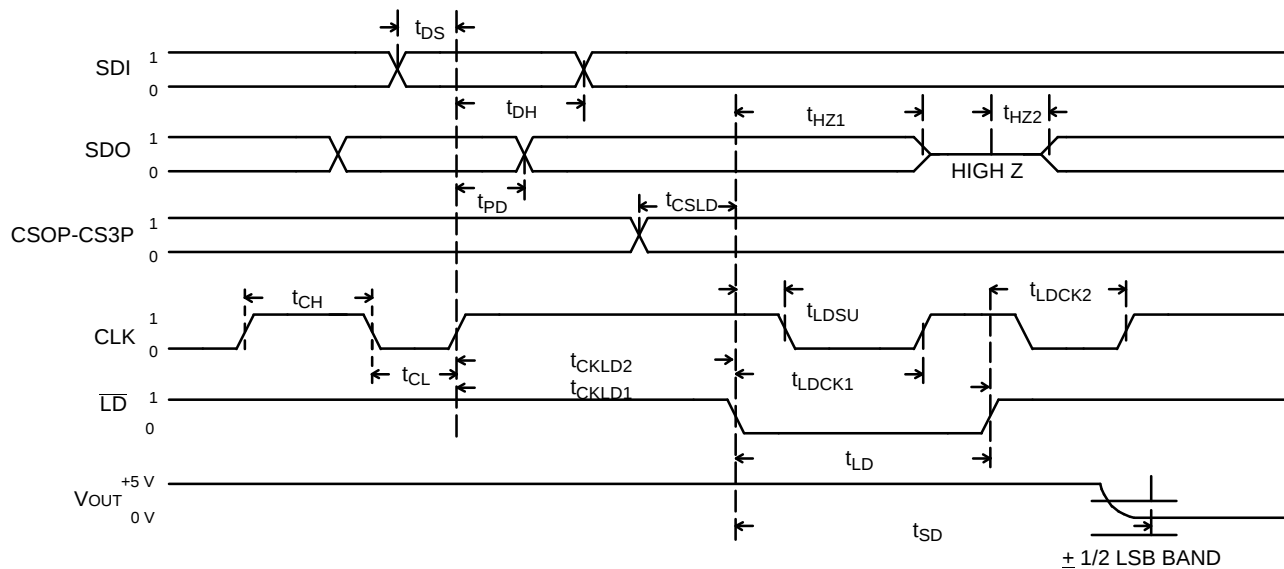


Figure 2. Detail Serial Data Input Timing ($\overline{\text{RST}} = "1"$)

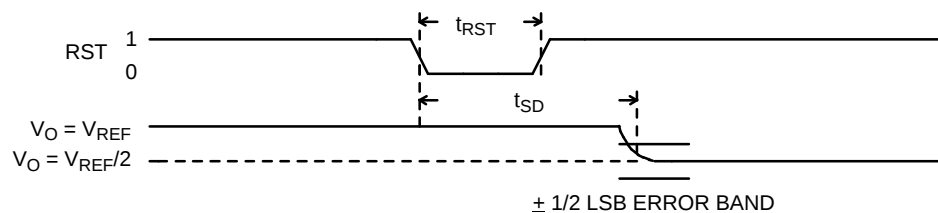


Figure 3. RESET Operation

THEORY OF OPERATION

MP7651 is equipped with a serial data 3-wire standard μ -processor logic interface to reduce pin count, package size (28 pin), and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 16-bit shift register (8 bits data D7 to D0, plus 4 bits address A3 to A0, and 4 bits of Chip Select data CS0S to CS3S). If the CS0S to CS3S in the shift register match the parallel chip-select address (CS0P to CS3P) for the selected chip, then the $\overline{LD}$ signal going low loads the data

into the selected DAC of that chip. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, 3-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. Note also that the reset signal ($\overline{RST}$) resets all analog outputs to $1/2$ of V_{REF} , regardless of any digital inputs. Also note that the input V_{Ri} is referenced to GND.

Function	A3	A2	A1	A0	$\overline{LD}$	CS0S CS1S CS2S CS3S	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	X X X X	0→1 Repeat	1	Data Input	Data Output
Stop Shifting Data In and Out	X	X	X	X	0	X X X X	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation	Matched with 4 parallel chip select data CS0P to CS3P	X	1	X	Hi-Z
DAC 0	0	0	0	1	1→0		X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0		X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0		X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0		X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0		X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0		X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0		X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0		X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation		X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮		X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation		X	1	X	Hi-Z
⋮	1	1	1	1	No Operation		X	1	X	Hi-Z
Reset all DACs to $V_{REF}/2$	X	X	X	X	X	X X X X	X	0	X	X

**Table 1. Digital Function Truth Table
Serial In/Serial Out**

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{Oi} = AGND + (V_{Ri} - AGND) \left(\frac{D}{256} \right)$
0	0	0	0	0	0	0	0	AGND
0	0	0	0	0	0	0	1	$(V_{Ri} - AGND) \left(\frac{1}{256} \right) + AGND$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{Ri} - AGND) \left(\frac{254}{256} \right) + AGND$
1	1	1	1	1	1	1	1	$(V_{Ri} - AGND) \left(\frac{255}{256} \right) + AGND$

**Table 2. DAC Transfer Function
Analog Output vs. Digital Code**



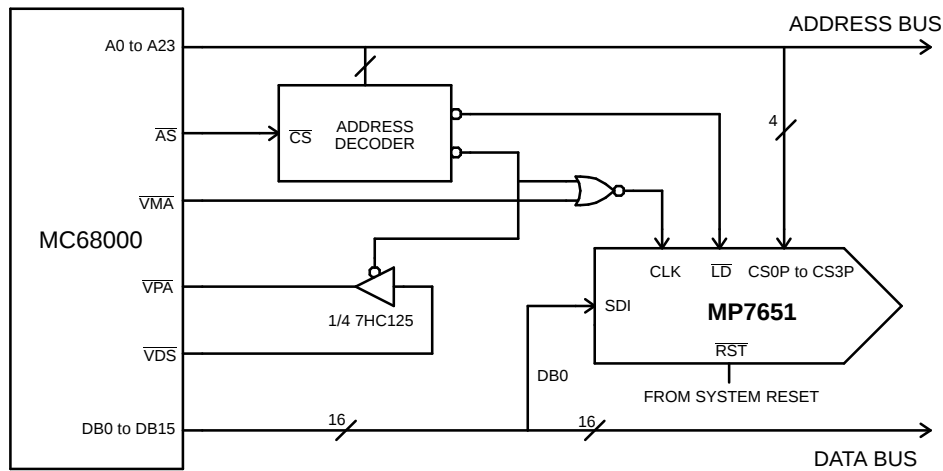
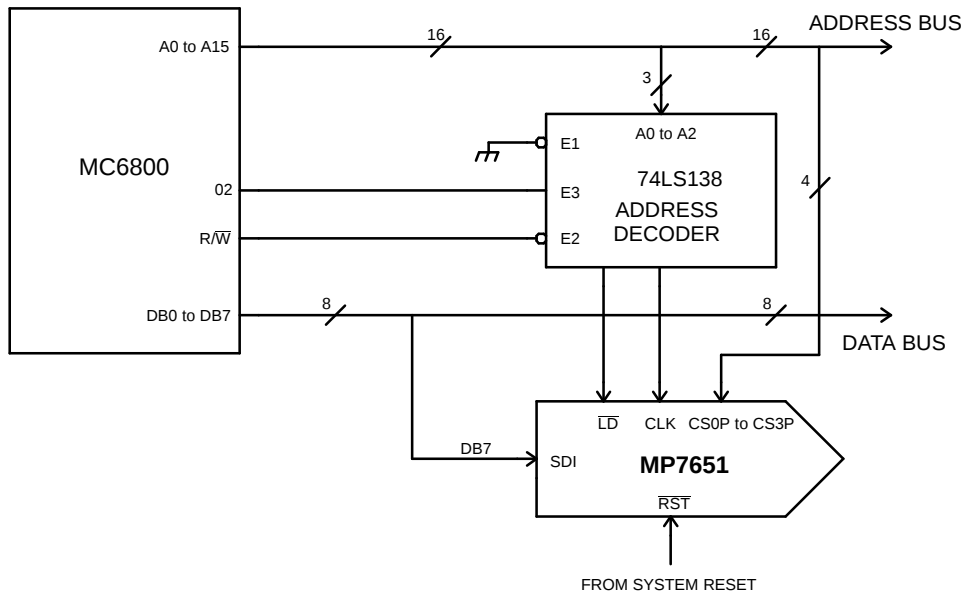


Figure 5. MC68000 Interface (Simplified Diagram)



NOTES:

1. Execute consecutive memory write instructions while manipulating the data between WRITES so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/W, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 6. MC6800 Interface (Simplified Diagram)

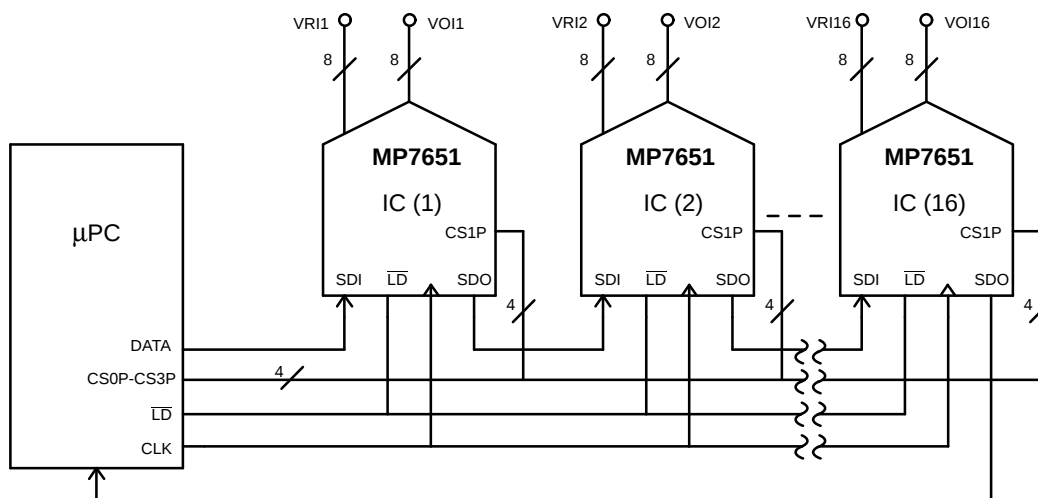


Figure 7. Simplified Diagram Configuration A

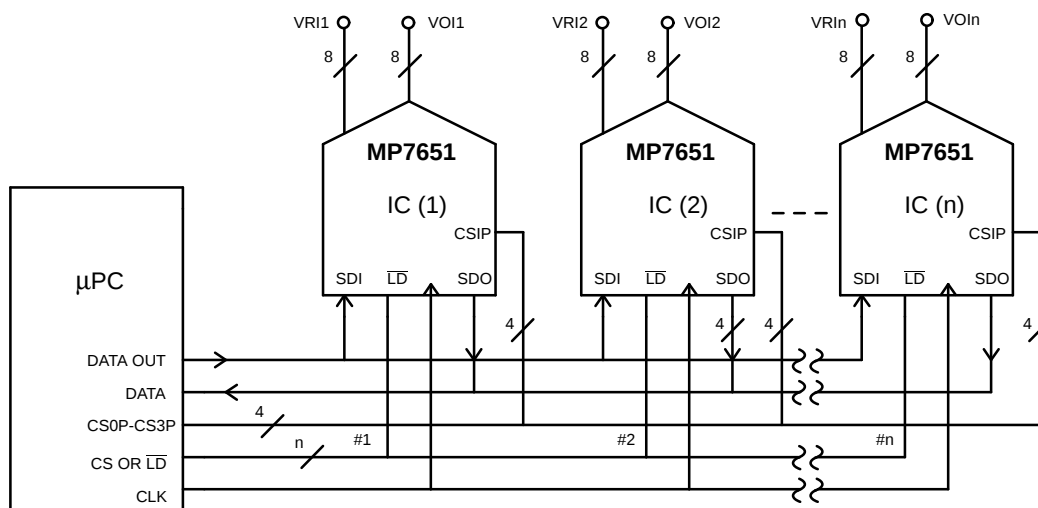
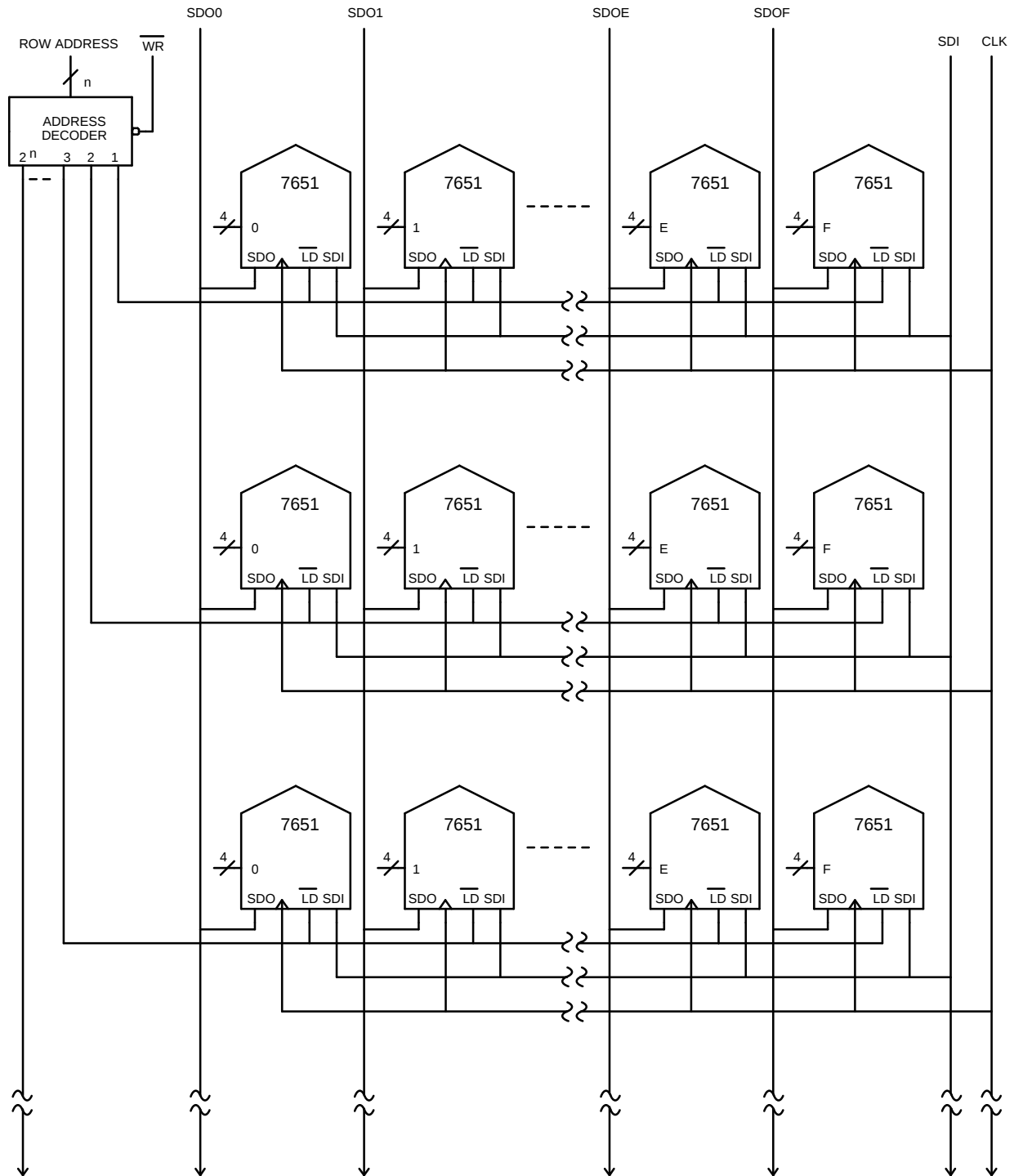
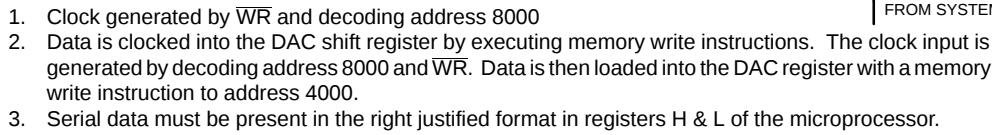


Figure 8. Simplified Diagram Configuration B



**Figure 9. Simplified Diagram
Configuration C**

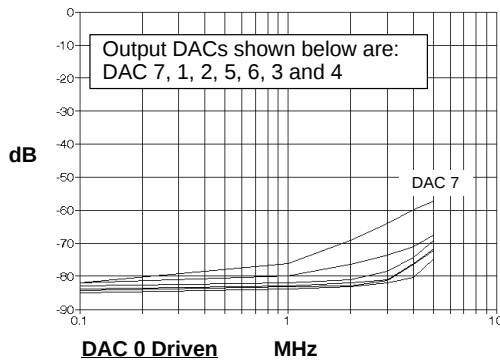


All resistors = 50 Ω unless otherwise specified
Gain of all DACs set to 1 (no attenuation)

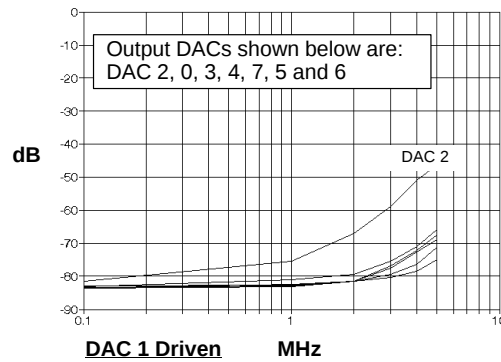


PERFORMANCE CHARACTERISTICS

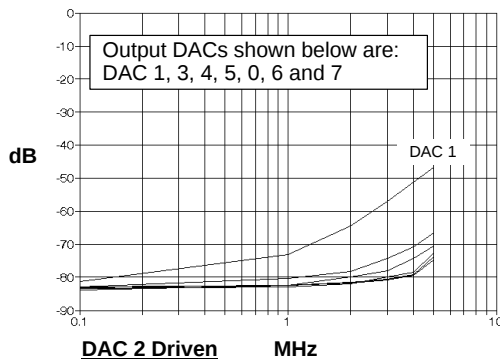
Channel-to-Channel Crosstalk (Gain vs. Frequency; All DACs set to full scale; $V_{REF}=1.6$ Vp-p)



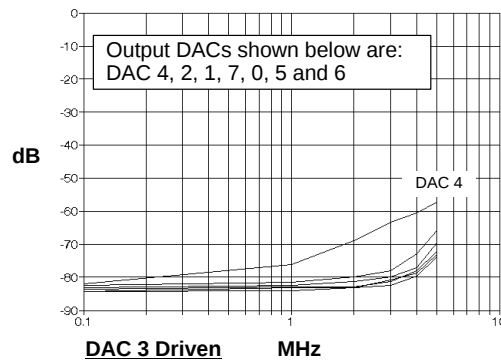
Graph 1.



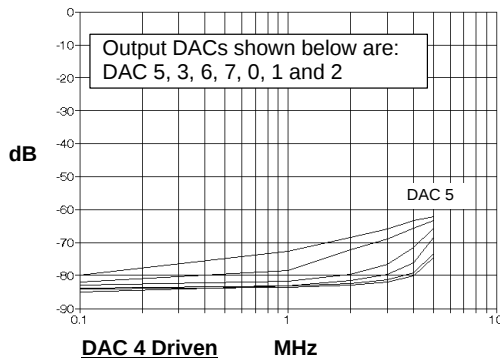
Graph 2.



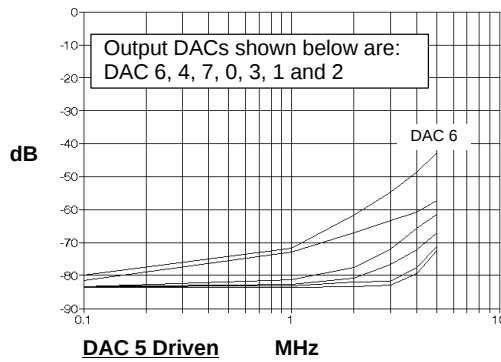
Graph 3.



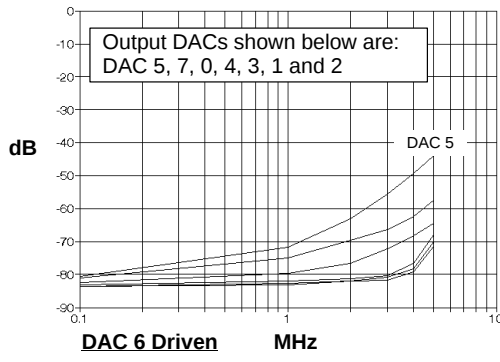
Graph 4.



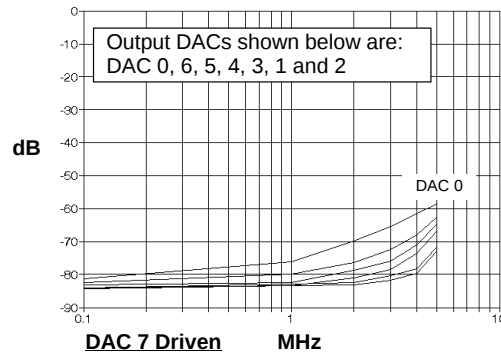
Graph 5.



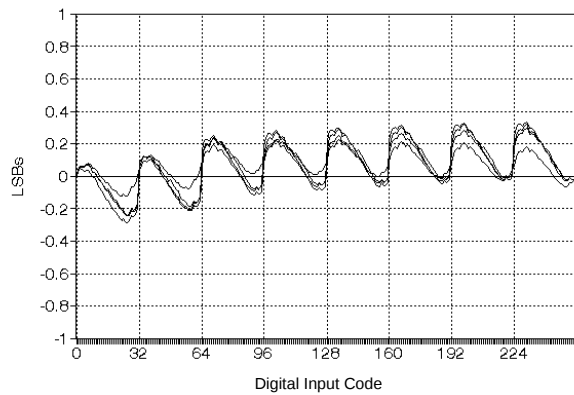
Graph 6.



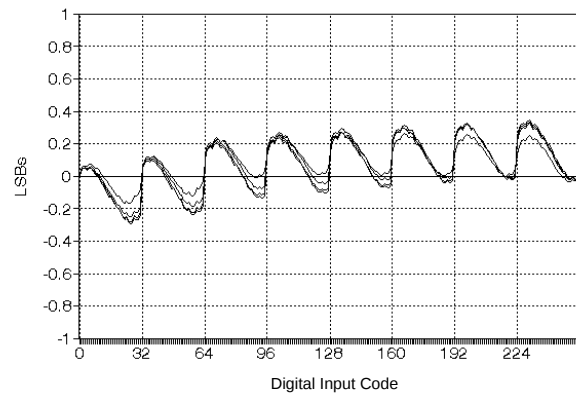
Graph 7.



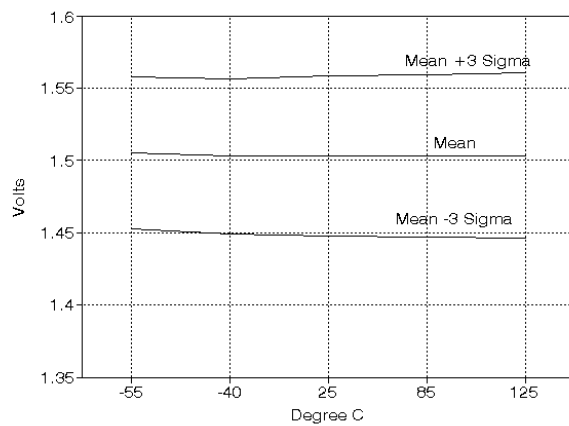
Graph 8.



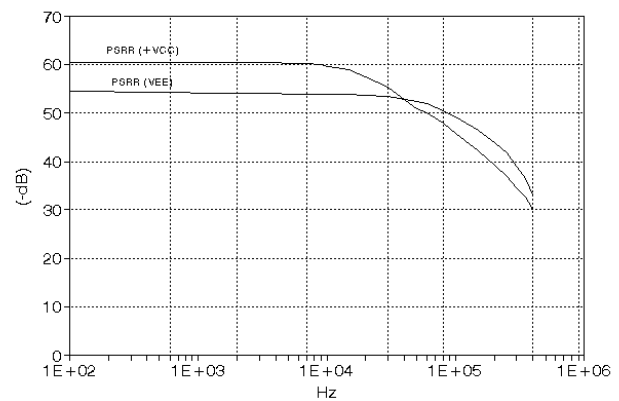
**Graph 9. Linearity Error vs. Digital Input Code
DACs 0 to 3**



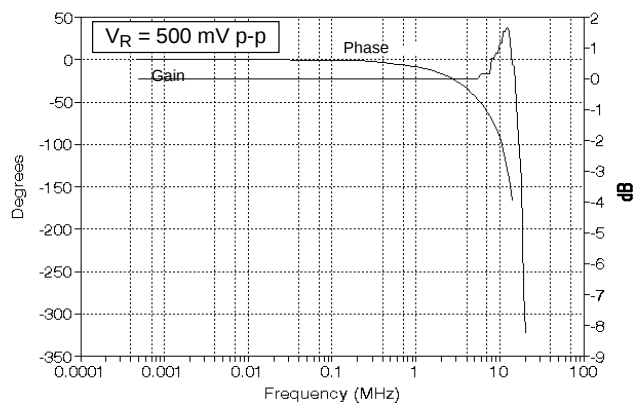
**Graph 10. Linearity Error vs. Digital Input Code
DACs 4 to 7**



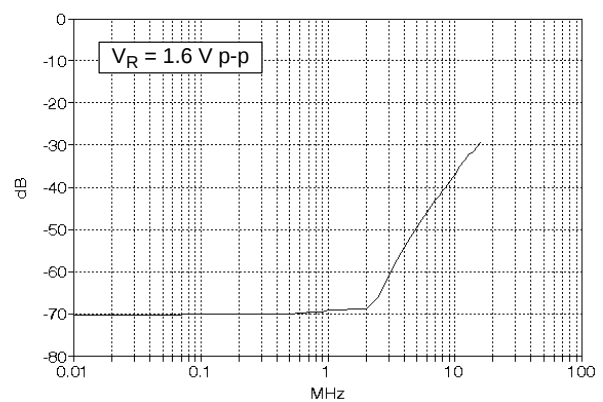
Graph 11. Preset Voltage vs. Temperature



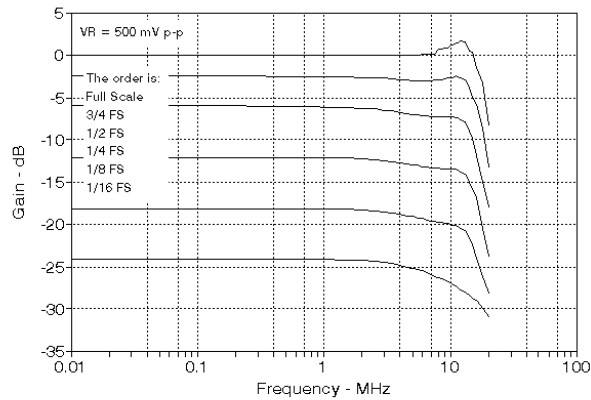
Graph 12. PSRR vs. Frequency



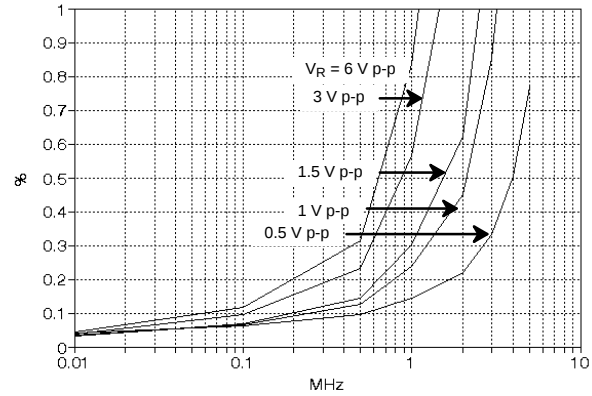
Graph 13. Gain & Phase vs. Frequency



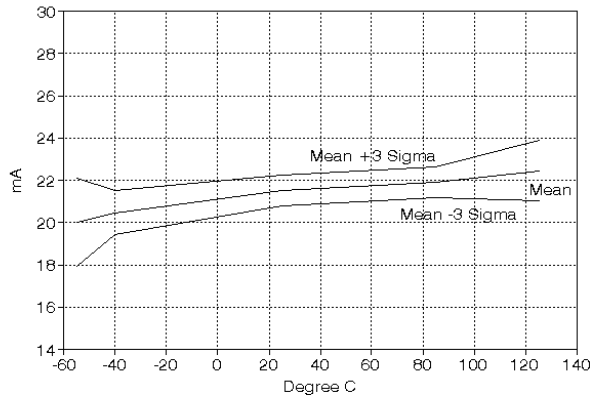
Graph 14. Feedthrough vs. Frequency



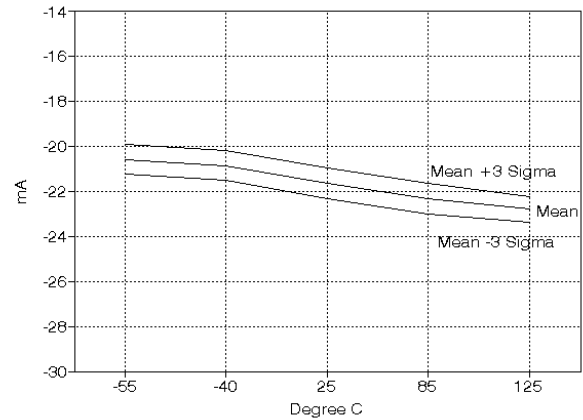
**Graph 15. Gain (V_O/V_R) vs. Frequency
Open Loop/Unloaded Output***



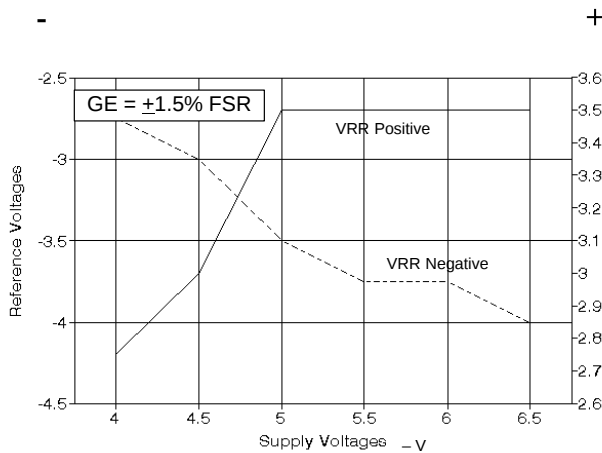
Graph 16. THD vs. Frequency



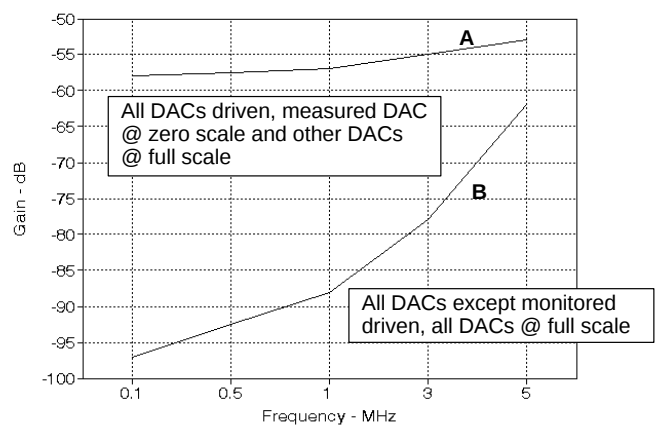
Graph 17. I_{CC} vs. Temperature



Graph 18. I_{EE} vs. Temperature



**Graph 19. Reference Input Voltage
Range vs. Supply Voltages**



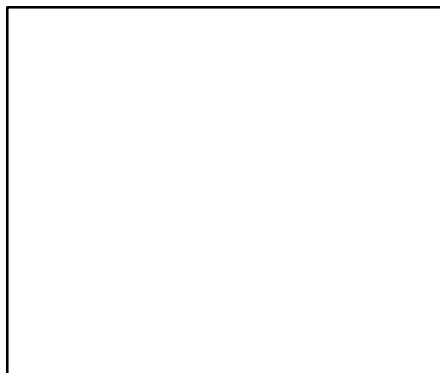
**Graph 20. All Channel
Crosstalk vs. Frequency**

* A 2K or 5K resistor across output and V_{EE} will remove peaking (See graph 26).

$\overline{\text{LD}}$
(5 V/DIV)

$V_R = 3 \text{ V}$
Digital Code =
255 $\rightarrow$ 0 $\rightarrow$ 255

V_O
(2 V/DIV)

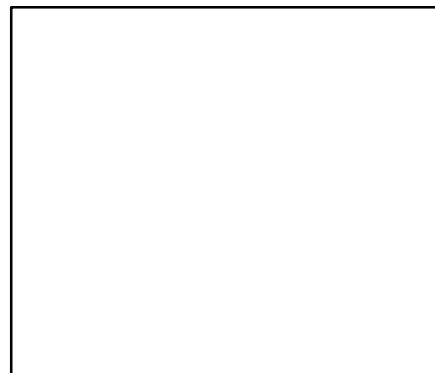
2 μs /DIV

Graph 21. Digital Settling

V_R
(2 V/DIV)

Digital Code =
All Ones

V_O
(2 V/DIV)

2 μs /DIVGraph 22. Pulse Response
($t_R = t_F = 100 \text{ ns}$ for V_R)

V_R
(2 V/DIV)

V_O
(2 V/DIV)

2 μs /DIVGraph 23. 128 kHz
Sawtooth Waveform Response

$\overline{\text{LD}}$
(5 V/DIV)

V_O
(10 mV/DIV)

2 μs /DIVGraph 24. Clock and SDI
Feedthrough

$\overline{\text{LD}}$
(5 V/DIV)

V_O
(10 mV/DIV)

2 μs /DIVGraph 25. Clock/SDI
Feedthrough

Gain
(5 dB/DIV)

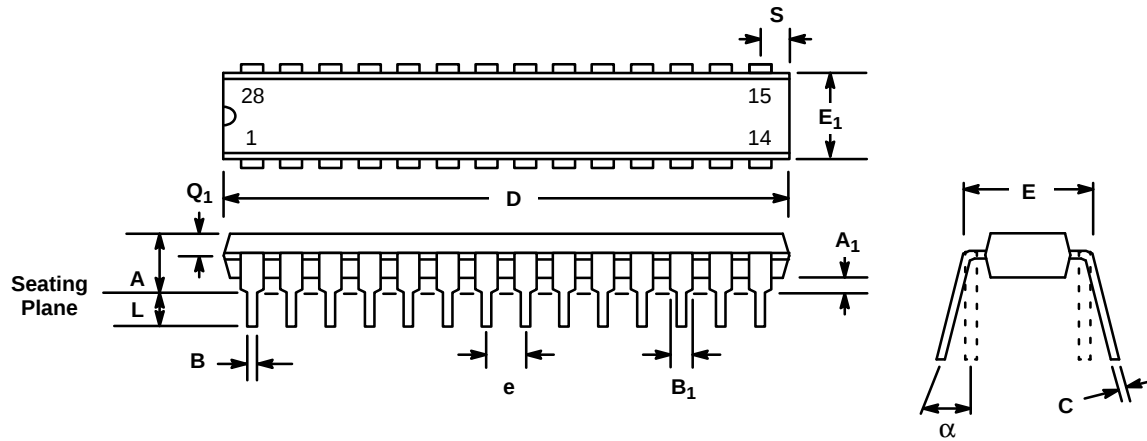
Group Delay
(20 ns/DIV)



MHz

Graph 26. Typical Gain and Group
Delay vs. Frequency (with 5K resistor
across output to V_{EE})

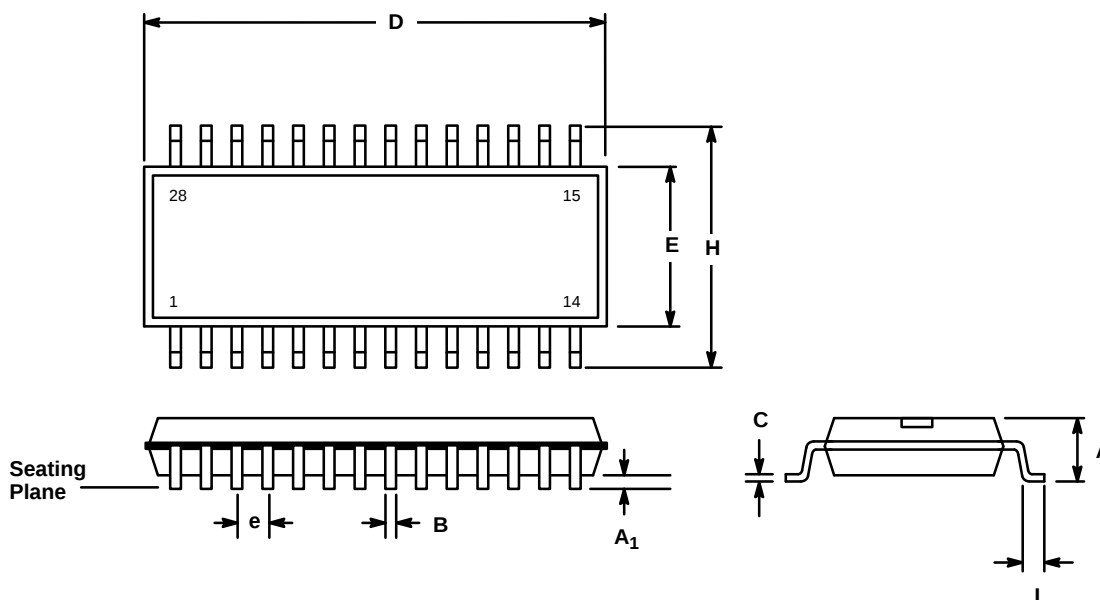
**28 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN28**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
A ₁	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B ₁ (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.340	1.485	34.04	37.72
E	0.290	0.325	7.37	8.26
E ₁	0.240	0.310	6.10	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q ₁	0.055	0.070	1.40	1.78
S	0.020	0.100	0.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE (335 MIL EIAJ SOIC) R28



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A ₁	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

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