National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC449A-X REV 1A0

Original Creation Date: 08/07/98
Last Update Date: 10/25/02
Last Major Revision Date: 10/24/02

1.2GHz ULTRA-WIDEBAND MONOLITHIC OP AMP

General Description

The Comlinear CLC449 is an ultra-high-speed monolithic op amp, with a typical -3dB bandwidth of 1.2GHz at a gain of +2. This wideband op amp supports rise and fall times less than 1ns, settling time of 6ns (to 0.2%) and slew rate of 2500V/us. The CLC449 achieves 2nd harmonic distortion of -68dBc at 5MHz at a low supply current of only 12mA. These performance advantages have been achieved through improvements in Comlinear's proven current feedback topology combined with a high-speed complementary bipolar process.

The DC to 1.2GHz bandwidth of the CLC449 is suitable for many IF and RF applications as a versatile op amp building block for replacement of AC coupled discrete designs. Operational amplifier functions such as active filters, gain blocks, differentiation, addition, subtraction and other signal conditioning functions take full advantage of the CLC449's unity-gain stable closed-loop performance.

The CLC449 performance provides greater headroom for lower frequency applications such as component video, high-resolution workstation graphics, and LCD displays. The amplifier's 0.1dB gain flatness to beyond 200MHz, plus 0.8ns 2V rise and fall times are ideal for improved time domain performance. In addition, the 0.03%/0.02 differential gain/phase performance allows system flexibility for handling standard NTSC and PAL signals.

In applications using high-speed flash A/D and D/A converters, the CLC449 provides the necessary wide bandwidth (1.2GHz), settling (6ns to 0.2%) and low distortion into 50 Ohms loads to improve SFDR.

Industry Part Number

CLC449A

NS Part Numbers

CLC449AJ-MLS
CLC449AJ-QML

Prime Die

VB1851A

Controlling Document

5962-9752001MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 1.2GHz small-signal bandwidth (Av = +2)
- 2500V/us slew rate
- 0.03%, 0.02 Dg
- 6ns settling time to 0.2%
- 3rd order intercept, 30dBm @ 70MHz
- Dual ±5V or single 10V supply
- High output current: 90mA
- 2.5dB noise figure

Applications

- High performance RGB video
- RF/IF amplifier
- Instrumentation
- Medical electronics
- Active filters
- High-speed A/D driver
- High-speed D/A buffer

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vcc)	±6V dc
Output Current (Iout)	±96mA
Common Mode Input Voltage	Vcc
Differential Input Voltage	±4V
Maximum Power Dissipation (Pd) (Note 2)	1.2W
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150C
Lead Temperature (soldering, 10 seconds)	+300 C
Thermal Resistance	
Junction -to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	TBD
(500 LFPM)	TBD
Junction -to-case (ThetaJC)	
Ceramic DIP	TBD
Package Weight (Typical)	
Ceramic DIP	TBD

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.
Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vcc)	±5V dc
Gain Range	±2 to ±10
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±5.0V, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 249 Ohms, gain resistance (Rg) = 249 Ohms, and gain (Av) = 2. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIO	Input Offset Voltage				-7	7	mV	1
					-12	12	mV	2, 3
IBN	Input Bias Current, non-inverting				-30	30	uA	1
					-60	60	uA	2, 3
IBI	Input Bias Current, inverting				-20	20	uA	1
					-40	40	uA	2, 3
PSRR	Power Supply Rejection Ratio	+V = 4.5V to 5.0V, -V = -4.5V to -5.0V			43		dB	1
					41		dB	2, 3
Icc	Supply Current	No Load				13.5	mA	1
						14.0	mA	2, 3
LSBW	Large Signal Bandwidth	Vout < 2.0Vpp			380		MHz	4
					360		MHz	5, 6
GFLAT	Gain Flatness	Vout < 2.0Vpp, 0.3MHz to 200MHz			-0.5	0.5	dB	4
					-0.7	0.7	dB	5, 6
HD2	2nd Harmonic Distortion	20MHz, 2.0Vpp			48		dBc	4
					48		dBc	5, 6
HD3	3rd Harmonic Distortion	20MHz, 2.0Vpp			66		dBc	4
					64		dBc	5, 6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI), (Note 3).

Vio	Input Offset Voltage				-0.7	+0.7	mV	1
Ibn	Input Bias Current, non-inverting				-3	+3	uA	1
Ibi	Input Bias Current, inverting				-2	+2	uA	1

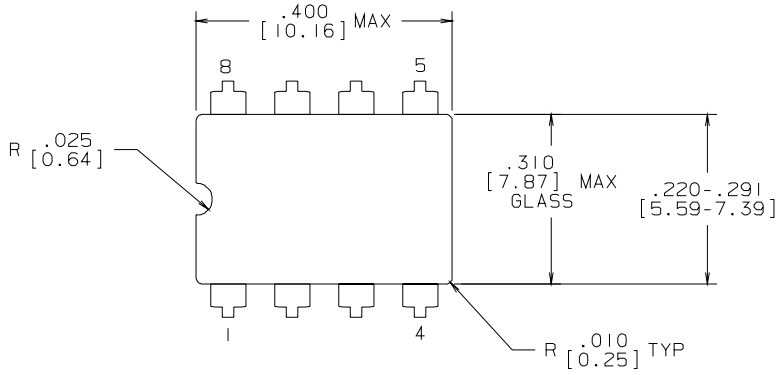
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

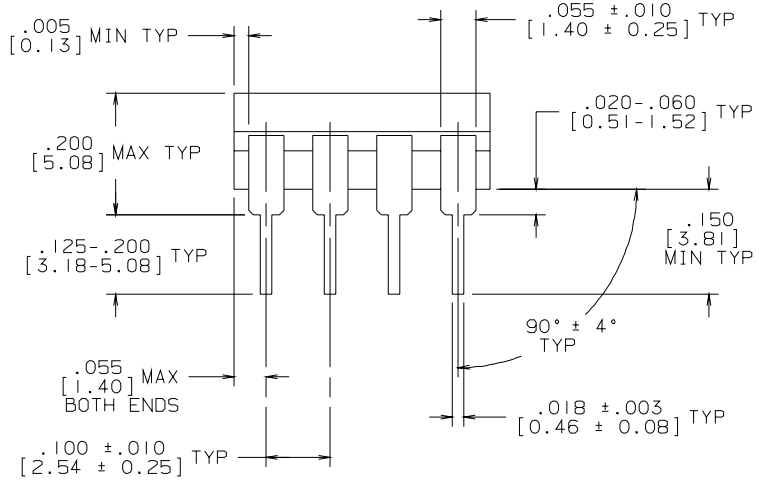
Graphics and Diagrams

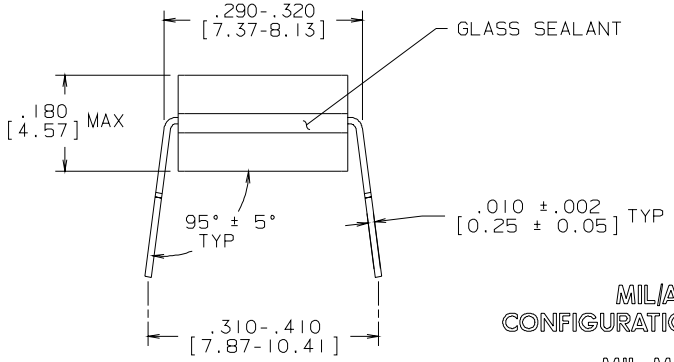
GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000410A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

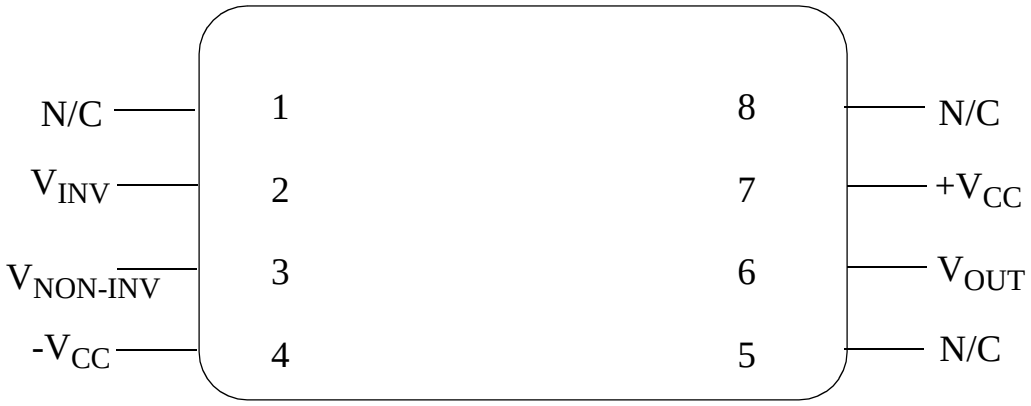
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC449J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000410A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002997	10/25/02	Shaw Mead	Initial MDS Release
1A0	M0004075	10/25/02	Rose Malone	Updated MDS: MNCLC449A-X, Rev. 0A0 to MNCLC449A-X, Rev. 1A0. Added MLS NSID to Main Table and Drift Table to Electrical Section.