
SDRAM SODIMM MODULE

512 MByte (64M x 64) SDRAM

Unbuffered 144 Pin SODIMM

LOW PROFILE (1.03 inch height)

General Description:

This memory module is a high performance 512 Megabyte Unbuffered synchronous dynamic RAM module organized as 64M x 64 in a 144 pin Small Outline Dual In-Line Memory Module (SODIMM) package. The module utilizes eight (8) 8Mx4X16 512MbitSDRAM¹ devices in a TSOP II 400 mil package. A 256 Byte Serial EEPROM contains the module configuration information. The EEPROM can be configured to a customer's specifications.

These modules offer substantial advances in SDRAM operating performance, including the ability to synchronously burst data at a high rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during burst.

Features:

- ◆ High density: 512 MB (64M x 64)
- ◆ Cycle time: 10 ns (100 MHz)
7.5 ns (133 MHz)
- ◆ JEDEC Standard 144 Pin Unbuffered SDRAM SODIMM Pinout
- ◆ PC133 and PC100 Compliant
- ◆ Single power supply of 3.3V ± 10%
- ◆ Serial Presence Detect
- ◆ LVTTL Compatible I/O and Clock
- ◆ Unbuffered Control and Address Lines
- ◆ Auto Precharge handled by SDRAM Devices
- ◆ Refresh 8K rows every 64ms
- ◆ Programmable Burst Type, Burst Length and CAS Latency of SDRAM Devices
- ◆ Internal Pipeline Operation
- ◆ Fully Synchronous – all signals registered on positive edge of system clock
- ◆ Package Height: 1.03 inches (+/- 10mils)

¹ Based on ELPIDA 512Mbit HM5257165B-75A

Operating Features:

The SDRAM SODIMM utilizes a clock input for the synchronization. Each operation of the SDRAM is determined by commands and all operations are referenced to a positive clock edge. CAS Latency defines the delay from when a Read Command is registered on a rising clock edge to when the data from the Read Command becomes available at the outputs. The CAS latency is expressed in terms of clock cycles. This specific DIMM supports 3 and 2 clock cycles.

The burst mode is a very high-speed access mode utilizing an internal column address generator. Once a column address for the first access is set, following addresses are automatically generated by the internal column address counter.

All control and address signals are supplied from the chipset through an unbuffered path to the SDRAMs. There are two clock signals supplied by the motherboard to synchronize the SODIMM.

Absolute Maximum Ratings*:

Item	Symbol	Rating	Unit
Supply voltage (V_{CC} Relative to V_{SS})	V_{CC}	-1.0 to +4.6	V
Input/Output Voltage	$V_{I/O}$	-1.0 to +4.6	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Short circuit output current	I_{out}	±50	MA

* Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

(Voltage referenced to V_{CC} . $T_A = 0$ to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.1	3.3	3.5	V
Input high voltage	V_{IH}	2.0	-	$V_{DD}+0.3$	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	+25	+70	°C

Capacitance:

($T_A=25^{\circ}\text{C}$, $V_{cc}=3.3\text{V}\pm 0.3\text{V}$)

Parameter	Symbol	Max.	Unit
Input capacitance (Address, /WE, CKE0,1 , /CAS)	C_{IN}	45	pF
Input capacitance (/CS0~/CS1)	C_{IN}	28	pF
Input capacitance (/DQMBs)	C_{IN}	14	pF
Input capacitance (CK0, CK1)	C_{IN}	28	pF
Input capacitance (/RAS)	C_{IN}	56	pF
Input/Output capacitance (DQ0~DQ63, CB0~CB7)	$C_{I/O}$	16	pF

Pin Names:

CK0-CK3	Clock Inputs	DQ0-DQ63	Data Inputs/Outputs
CKE0	Clock Enables	CB0-CB7	ECC Data Input/Output
/RAS	Row Address Strobe	/DQMB0-/DQMB7	Data Mask Enables
/CAS	Column Address Strobe	V _{DD}	Power supply
/WE	Write Enable	V _{SS}	Ground
/CS0-/CS3	Chip Select	SCL	Serial Clock
A0-A11	Address Inputs	SDA	Serial Data Input/Output
BA0, BA1	SDRAM Bank Select	SA0-SA2	Decode Input
NC or DU	No Connect	WP	Write Protect for SPD

SDRAM Pinout:

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	V _{SS}	37	DQ8	73	NU	109	A9
2	V _{SS}	38	DQ40	74	CK1	110	BA1
3	DQ0	39	DQ9	75	V _{SS}	111	A10/AP
4	DQ32	40	DQ41	76	V _{SS}	112	A11
5	DQ1	41	DQ10	77	NC	113	V _{DD}
6	DQ33	42	DQ42	78	NC	114	V _{DD}
7	DQ2	43	DQ11	79	NC	115	DQMB2
8	DQ34	44	DQ43	80	NC	116	DQMB6
9	DQ3	45	V _{DD}	81	V _{DD}	117	DQMB3
10	DQ35	46	V _{DD}	82	V _{DD}	118	DQMB7
11	V _{DD}	47	DQ12	83	DQ16	119	V _{SS}
12	V _{DD}	48	DQ44	84	DQ48	120	V _{SS}
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	V _{SS}	91	V _{SS}	127	DQ27
20	DQ39	56	V _{SS}	92	V _{SS}	128	DQ59
21	V _{SS}	57	NC	93	DQ20	129	V _{DD}
22	V _{SS}	58	NC	94	DQ52	130	V _{DD}
23	DQMB0	59	NC	95	DQ21	131	DQ28
24	DQMB4	60	NC	96	DQ53	132	DQ60
25	DQMB1	61	CK0	97	DQ22	133	DQ29
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
27	V _{DD}	63	V _{DD}	99	DQ23	135	DQ30
28	V _{DD}	64	V _{DD}	100	DQ55	136	DQ62
29	A0	65	RAS	101	V _{DD}	137	DQ31
30	A3	66	CAS	102	V _{DD}	138	DQ63
31	A1	67	WE	103	A6	139	V _{SS}
32	A4	68	CKE1	104	A7	140	V _{SS}
33	A2	69	S0	105	A8	141	SDA
34	A5	70	A12	106	BA0	142	SCL
35	V _{SS}	71	S1	107	V _{SS}	143	V _{DD}
36	V _{SS}	72	A13	108	V _{SS}	144	V _{DD}

DC Characteristics:
 $(V_{DD} = 3.3V \pm 0.3V, V_{SS} = 0V, T_A = 0 \text{ to } +70^\circ\text{C})$

Parameter ²	Symbol	133MHz Max.	100MHz Max.	Unit
Operating current (No Burst, $T_{CK} = \text{min.}$, $T_{RC} = \text{min.}$, Single Bank)	I_{CC1}	880	880	mA
Precharge Standby Current ($CKE = V_{IL}$, $T_{CK} = \text{min.}$, All banks idle) ($CKE = V_{IH}$, $T_{CK} = \text{min.}$, All banks idle)	I_{CC2}	48 320	48 320	mA
Active Standby Current ($CKE = V_{IL}$, $T_{CK} = \text{min.}$, One bank active) ($CKE = V_{IH}$, $T_{CK} = \text{min.}$, One bank active)	I_{CC3}	32 240	32 240	mA
Burst Mode Current ($t_{CK} = \text{min.}$)	I_{CC4}	760	760	mA
Refresh Current (per DIMM bank) ($t_{CK} = \text{min.}$, $t_{RC} = \text{min.}$, $t_{RRD} = \text{min.}$, Auto Refresh)	I_{CC5}	1320	1320	mA
Self Refresh Current (all DIMM banks, $CKE = V_{IL}$)	I_{CC6}	48	48	mA

AC Electrical Characteristics:
 $(T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{DD} = 3.3V \pm 0.3V, V_{DD} = 0V)$

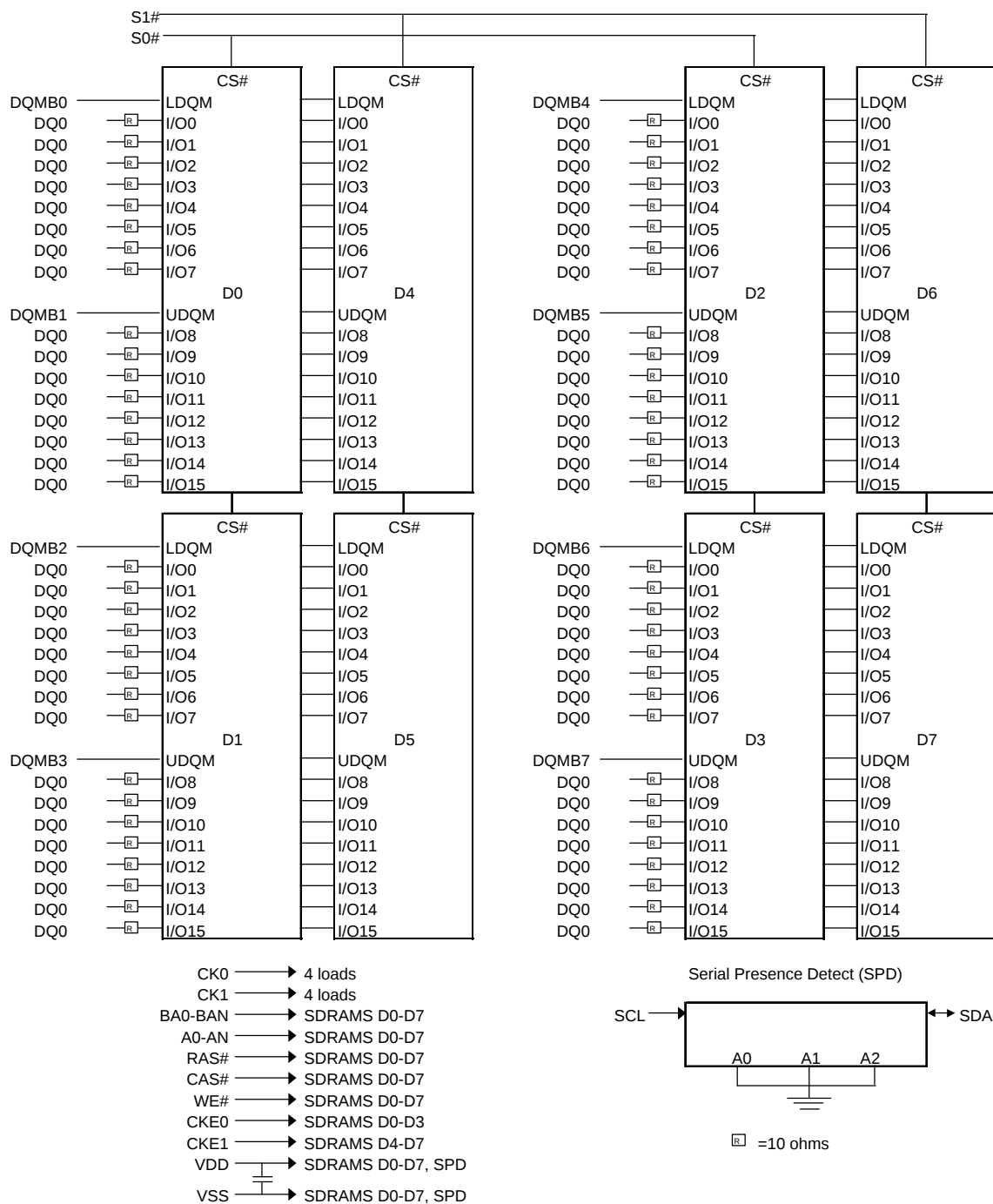
Parameter	Symbol	133MHz Min.	133MHz Max.	100MHz Min.	100MHz Max.	Unit
Row to row active delay	t_{RRD}	15		20		ns
RAS to CAS delay	t_{RCD}	20		20		ns
Row precharge time	t_{RP}	20		20		ns
Row active time	t_{RAS}	45	120K	50	120K	ns
Row cycle time	t_{RC}	67.5		70		ns
Last data in to row precharge	t_{RDL}	8		10		ns
Last data in to new Col. Address delay	t_{CDL}	1		1		clk
Last data in to burst stop	T_{BDL}	1		1		clk
Column address to column address delay	T_{CCD}	1		1		clk
Number of valid output data (CL=3) (CL=2)			2 -		2 1	Ea
Clock Cycle Time (CL=3) (CL=2)	t_{CC}	7.5 -		10 10^3		ns
Clock to Valid Output Delay (CL=3) (CL=2)	T_{AC}		5.4 5.4		6 6	ns
Output Data Hold Time (CL=3) (CL=2)	t_{OH}	2.7 -		3 3		ns
Clock High Pulse Width	t_{CH}	2.5		3		ns
Clock Low Pulse Width	t_{CL}	2.5		3		ns
Input Setup Time	t_{SS}	1.5		2		ns
Input Hold Time	t_{SH}	0.8		1		ns
Clock to Output in Low-Z	T_{SLZ}	1		1		ns

² Typical Actual values run lower than Max Spec'ed Values.

³ Available for select SDRAM devices/part numbers.

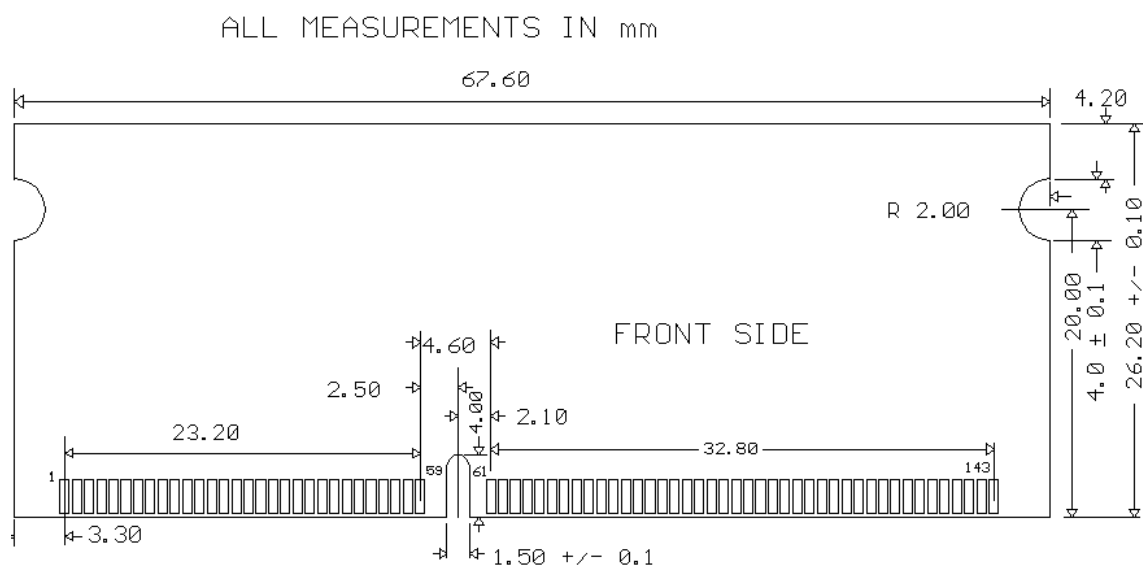
Clock to Output in High-Z	t _{SHZ}	5.4	6	ns
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Functional Block Diagram:



Part number*	Configuration	Height	Clock Speed
KT6464SSN0UBL-XX	64M x 64	1.03 in.	10ns (100 MHz)
KT6464SSN3UBL-XX	64M x 64	1.03 in.	7.5ns (133 MHz)

Package Description:



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