ML2264*

4-Channel High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2264 is a high-speed, µP compatible, 4-channel 8-bit A/D converter with a conversion time of 680ns over the operating temperature range and supply voltage tolerance. The ML2264 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2264 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz.

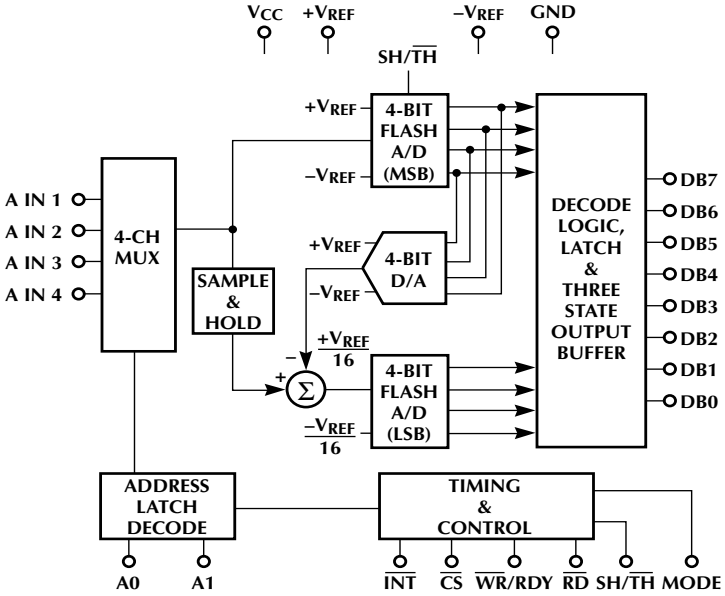
The ML2264 digital interface has been designed so that the device appears as a memory location or I/O port to a µP. Analog input channels are selected by the latched and decoded multiplexer address inputs.

The ML2264 is an enhanced, pin compatible second source for the industry standard AD7824. The ML2264 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

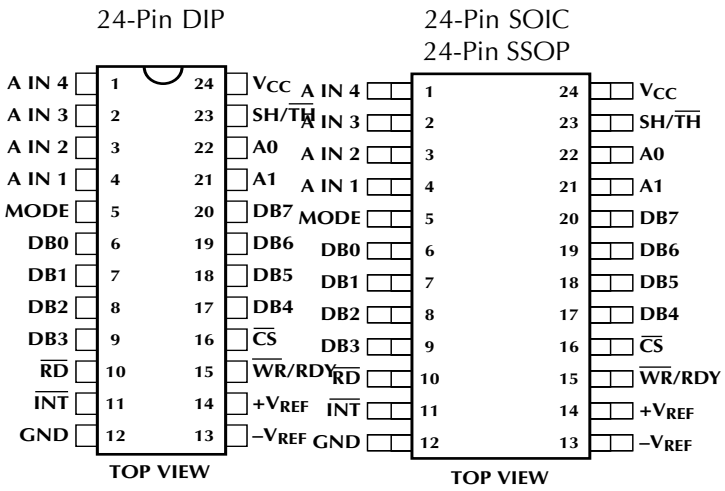
FEATURES

- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 830ns max
  - Sample & Hold Mode ..... 700ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Capable of digitizing a 5V, 250kHz sine wave
- 4-analog input channels
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Power-on reset circuitry
- Low power 100mW
- Narrow 24-pin DIP, SOIC, or SSOP
- Superior pin compatible replacement for AD7824

BLOCK DIAGRAM



PIN CONNECTIONS



*This Part Is End Of Life As Of August 1, 2000

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	A IN 4	Analog input 4.
2	A IN 3	Analog input 3.
3	A IN 2	Analog input 2.
4	A IN 1	Analog input 1.
5	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
6	DB0	Data output — bit 0 (LSB).
7	DB1	Data output — bit 1.
8	DB2	Data output — bit 2.
8	DB3	Data output — bit 3.
10	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
11	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
12	GND	Ground.
13	$-V_{REF}$	Negative reference voltage for A/D converter.
14	$+V_{REF}$	Positive reference voltage for A/D converter.
15	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is $\overline{WR}$ input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
16	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
17	DB4	Data output — bit 4.
18	DB5	Data output — bit 5.
19	DB6	Data output — bit 6.
20	DB7	Data output — bit 7 (MSB).
21	A1	Digital address input 1 that selects analog input channel. See multiplexer addressing section.
22	A0	Digital address input 0 that selects analog input channel. See multiplexer addressing section.
23	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
24	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} + 0.3V
  Analog Inputs ..... –0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Plastic) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C
  SOIC
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... T_{MIN} - T_A - T_{MAX}
  ML2264CCS
  ML2264CCP
  ML2264CCR ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$ (Note 1)

PARAMETER	NOTES	CONDITIONS		ML2264XCX MIN	ML2264XCX TYP (NOTE 3)	ML2264XCX MAX	UNITS
Converter							
Total Unadjusted Error ML2264CXX	4, 6					±1	LSB
Integral Linearity Error ML2264CXX	4, 6					±1	LSB
Differential Linearity Error ML2264CXX	4					±1	LSB
Full Scale Error ML2264CXX	4					±1	LSB
Zero Scale Error ML2264CXX	4					±1	LSB
Channel to Channel Mismatch	4					±1/4	LSB
$+V_{REF}$ Voltage Range	5			$-V_{REF}$		V_{CC}+0.1	V
$-V_{REF}$ Voltage Range	5			GND–0.1		$+V_{REF}$	V
Reference Input Resistance	4			1	2.5	4	k ý
Analog Input Range	4, 7			GND–0.1		V_{CC}+0.1	V
Power Supply Sensitivity	4	DC V_{CC} =5V ± 5%, V_{REF} = 4.50V			±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC}, V_{IN} = 0			±1/16		LSB
Analog Input Leakage Current, OFF Channel	4	ON Channel = V_{CC} OFF Channel = 0V		–1			µA
		ON Channel = 0V OFF Channel = V_{CC}				1	µA
Analog Input Leakage Current, ON Channel	4	ON Channel = 0V OFF Channel = V_{CC}		–1			µA
		ON Channel = V_{CC} OFF Channel = 0V				1	µA
Analog Input Capacitance		During Acquisition Period			45		pF
Digital and DC							
$V_{IN(1)}$, Logical "1" Input Voltage	4	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1		2.0			V
		MODE, SH/$\overline{TH}$		V_{CC}–0.5			V
$V_{IN(0)}$, Logical "0" Input Voltage	4	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1				0.8	V
		MODE, SH/$\overline{TH}$				0.5	V
$I_{IN(1)}$, Logical "1" Input Current	4	$V_{IH} = V_{CC}$	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, A1			1	µA
			MODE, SH/$\overline{TH}$	15	50	150	µA
$I_{IN(0)}$, Logical "0" Input Current	4	V_{IL} = GND	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	–1			µA
			MODE, SH/$\overline{TH}$	–20			µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$, and timing measured at 1.4V, $C_L = 100pF$. (Note 1)

PARAMETER	NOTES	CONDITIONS	ML2264XCX MIN	ML2264XCX TYP (NOTE 3)	ML2264XCX MAX	UNITS
Digital and DC (Continued)						
$V_{OUT(1)}$, Logical "1" Output Voltage	4	$I_{OUT} = -2mA$	4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	4	$I_{OUT} = 2mA$			0.4	V
I_{OUT}, Three-State Output Current	4	$V_{OUT} = 0V$	–1			µA
		$V_{OUT} = V_{CC}$				1µA
C_{OUT}, Logic Output Capacitance				5		pF
C_{IN}, Logic Input Capacitance				5		pF
I_{CC}, Supply Current	4	$\overline{CS} = \overline{WR} = \overline{RD}$ = "1", No Output Load			18	mA
AC and Dynamic Performance (Note 9)						
t_{CRD}, Conversion Time, Read Mode	4	$\overline{RD}$ to $\overline{INT}$, MODE = 0V			1020	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	4, 8	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; $SH/\overline{TH} = V_{CC}$			700	ns
		$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; $SH/\overline{TH} = GND$			830	ns
SNR, Signal to Noise Ratio		$V_{IN} = 5V$, 250kHz Noise is sum of all nonfundamental components from 0–500kHz. $SH/\overline{TH} = V_{CC}$, MODE = V_{CC} $f_{SAMPLING} = 1.0$ MHz		48		dB
HD, Harmonic Distortion		$V_{IN} = 5V$, 250kHz THD is sum of 2–5th harmonics relative to fundamental. $SH/\overline{TH} = V_{CC}$, MODE = V_{CC} $f_{SAMPLING} = 1.0$ MHz		–63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. $SH/\overline{TH} = V_{CC}$, MODE = V_{CC} $f_{SAMPLING} = 1.0$ MHz		–60		dB
FR, Frequency Response		$V_{IN} = 5V$, 0–250kHz Relative to 1kHz $SH/\overline{TH} = V_{CC}$, MODE = V_{CC} $f_{SAMPLING} = 1.0$ MHz		±0.1		dB
SR, Slew Rate Tracking	5	$SH/\overline{TH} = V_{CC}$			4.0	V/µs
		$SH/\overline{TH} = GND$			0.25	V/µs
t_{AS}, Multiplexer Address Setup Time	4	$SH/\overline{TH} = GND$, Figure 1 (Track & Hold Operation)	0			ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF. (Note 1)

PARAMETER	NOTES	CONDITIONS	ML2264XCX			UNITS
			MIN	TYP (NOTE 3)	MAX	
AC and Dynamic Performance (Note 9) (Continued)						
t_{AH}, Multiplexer Address Hold Time	4	SH/$\overline{TH}$ = GND, Figure 1 (Track & Hold Operation)	60			ns
t_{AS}, Multiplexer Address Setup Time	4	SH/$\overline{TH}$ = V_{CC}, Figure 2 (Sample & Hold Operation)	225			ns
t_{AH}, Multiplexer Address Hold Time	4	SH/$\overline{TH}$ = V_{CC}, Figure 2 (Sample & Hold Operation)	60			ns
AC Performance Read Mode (Pin 5 = 0V), Figure 4						
t_{RDY}, $\overline{CS}$ to RDY Delay	4		0		60	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	4, 9	Figure 3			1020	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	4		0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	4		0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ low	4, 9				1020	ns
t_{ACC0}, Data Access Time $\overline{RD}$ to Data Valid	4		t_{CRD}–10		t_{CRD}+20	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	4		t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	4, 9		0		65	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	5, 9	Figure 3	0		50	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	4, 9	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			ns
AC Performance Write-Read Mode (Pin 5 = 5V), Figures 5 and 6						
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	4		0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	4		0			ns
t_{WR}, $\overline{WR}$ Pulse Width	4	SH/$\overline{TH}$ = V_{CC}	190		50K	ns
	5	SH/$\overline{TH}$ = GND	320		50K	ns
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	4	$t_{RD} < t_{INTL}$	275			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	4, 9	$t_{RD} < t_{INTL}$	0		235	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	4	$t_{RD} < t_{INTL}$	0		240	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	4, 8, 9	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}			700	ns
	5, 8, 9	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			830	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF. (Note 1)

PARAMETER	NOTES	CONDITIONS	ML2264XCX			UNITS
			MIN	TYP (NOTE 3)	MAX	
AC Performance Write-Read Mode (Pin 5 = 5V) Figures 5 and 6 (Continued)						
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	4, 9	$t_{RD} > t_{INTL}$			620	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	4	$t_{RD} > t_{INTL}$	0		50	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	5, 9	Figure 3	0		50	ns
t_{INTH}, $\overline{RD}$□ to $\overline{INT}$□ Delay	4, 9		0		65	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	4, 9	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			ns
t_{IHWR}, $\overline{WR}$□ to $\overline{INT}$□ Delay	4, 9	Standalone Mode	0		90	ns
t_{ID}, $\overline{INT}$¬ to Data Valid Delay	4, 9	Standalone Mode	0		20	ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

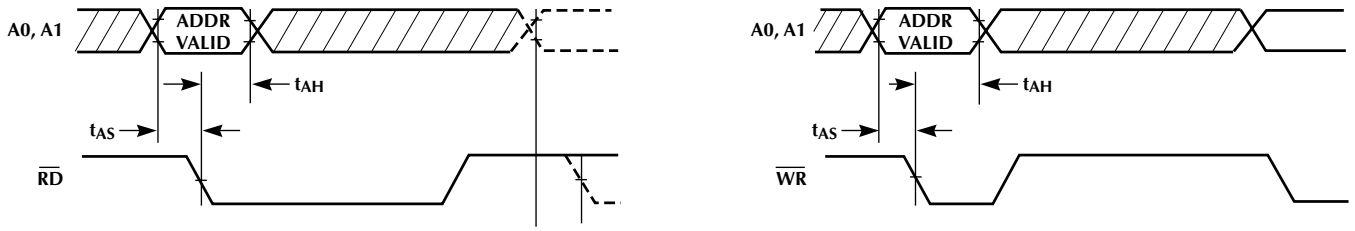
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Total unadjusted error includes offset, full scale, linearity, sample and hold, and multiplexer errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{R1}, and t_P. For example, for the ML2264XCX in the sample and hold mode, $\overline{WR}$/$\overline{RD}$ mode: t_{WR} = 190ns, t_{RD} = 275ns with a frequency of 1.000MHz (cycle time of 1000ns).

Note 7: For $-V_{REF} \bullet V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 8: Conversion time, write-read mode = $t_{WR} + t_{RD} + t_{RI}$.

Note 9: Defined from the time an output crosses 0.8V or 2.4V.



a) RD Mode (Pin 5 = GND)

b) WR-RD Mode (Pin 5 = V_{CC})

Figure 1. Analog Multiplexer Address Timing for Track & Hold Mode (Pin 23 = GND)

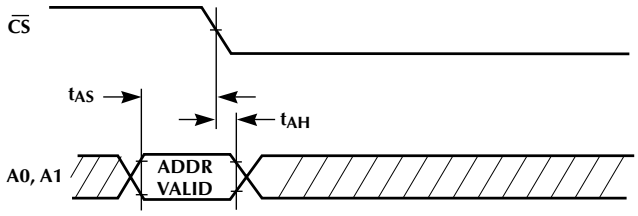


Figure 2. Analog Multiplexer Address Timing for Sample & Hold Mode (Pin 23 = V_{CC})

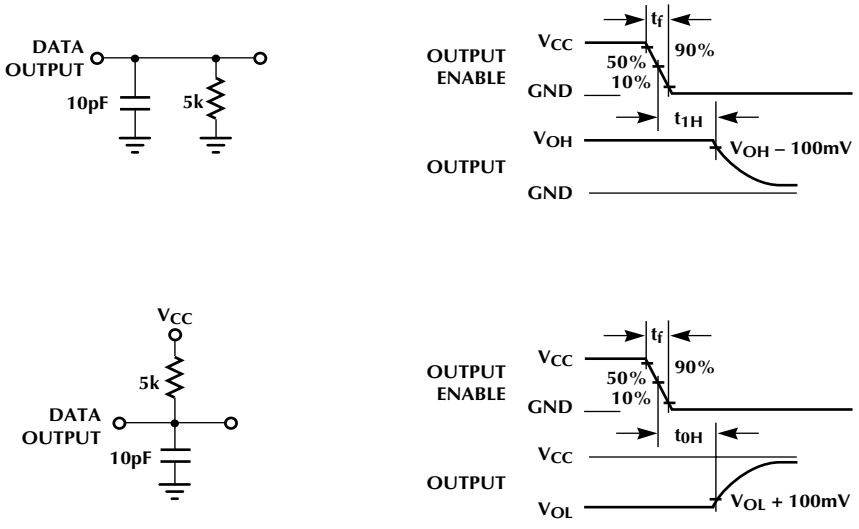
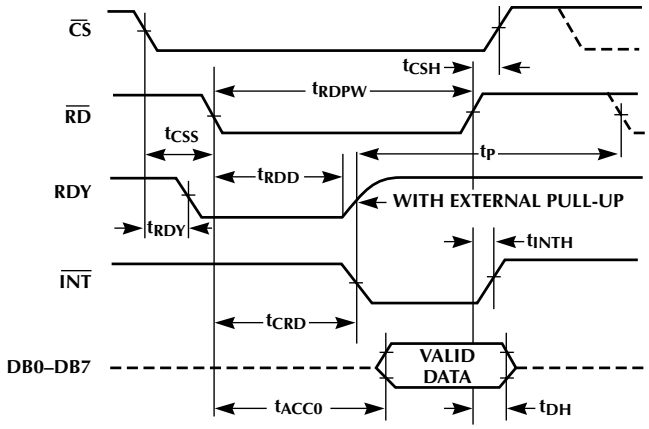


Figure 3. High Impedance Test Circuits and Waveforms



*In SAMPLE & HOLD mode a pull up resistor on RDY should not be used unless CS¬ is • 20ns before RD¬.

Figure 4. RD Mode Timing

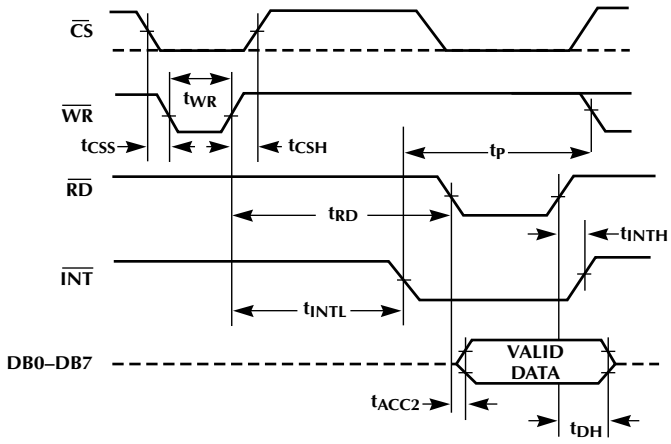


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

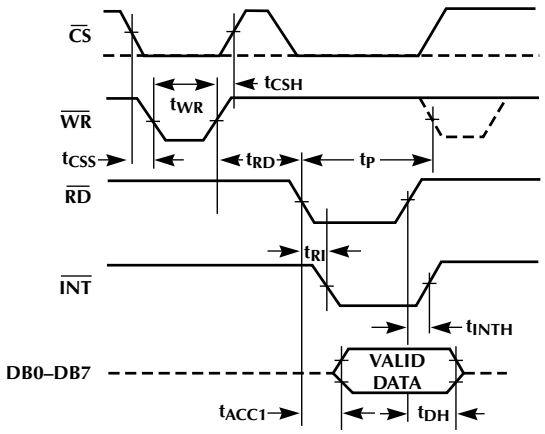


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

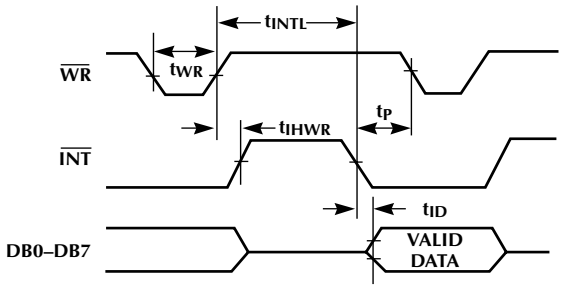


Figure 7. WR-RD Mode Stand-Alone Timing $\overline{CS} = \overline{RD} = 0$

1.0 FUNCTIONAL DESCRIPTION

The ML2264 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word.

1.1 MULTIPLEXER ADDRESSING

The ML2264 contains a 4-channel single ended analog multiplexer. A particular input channel is selected by using the address inputs A0 and A1. The relationship between the address inputs, A0 and A1, and the analog input selected is shown in Table 1.

Selected Analog Channel	Address Input	
	A0	A1
A IN 1	0	0
A IN 2	1	0
A IN 3	0	1
A IN 4	1	1

Table 1. Multiplexer Address Decoding

The address inputs are latched into the ML2264 on the falling edge of the $\overline{RD}$, $\overline{WR}$, or $\overline{CS}$ depending on the state of pins SH/$\overline{TH}$ and mode as shown in Table 2.

Address Latching Signal	Mode	Operation Mode
$\overline{RD}$¬	GND	GND
$\overline{WR}$¬	V_{CC}	GND
$\overline{CS}$¬	GND	V_{CC}
$\overline{CS}$¬	V_{CC}	V_{CC}

Table 2.

In the Sample & Hold mode of operation $\overline{CS}$ is used as the address latch enable, allowing for continuous conversions without addressing a given analog input for each conversion.

The Track & Hold mode of operation requires an analog input to be addressed and latched for each conversion that the ML2264 performs.

1.2 ANALOG INPUTS

The analog input on the ML2264 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 8. When the conversion starts in the T/H mode ($\overline{WR}$¬ in the WR-RD mode or $\overline{RD}$¬ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when $\overline{WR}$□ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2264 operates in the S/H mode (pin 23 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of $\overline{INT}$ and ends with the falling edge of $\overline{WR}$ in the WR-RD mode or the falling edge of $\overline{RD}$ in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46pF of input capacitance must be charged up in addition to the 11pF of stray capacitance.

1.3 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2264 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and

the MSB comparators will be tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2264 can track and hold signals with slew rates as high as 0.25V/µs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2264 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2264 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/µs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.3.1 Converter — T/H Mode

The operating sequence for the WR-RD mode is illustrated in Figure 9a. Initially, the internal comparators are auto-zeroed while $\overline{WR}$ is high. A conversion is initiated by the falling edge of $\overline{WR}$. While $\overline{WR}$ is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of $\overline{WR}$, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While $\overline{WR}$ is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while $\overline{WR}$ is high before another conversion can start.

The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

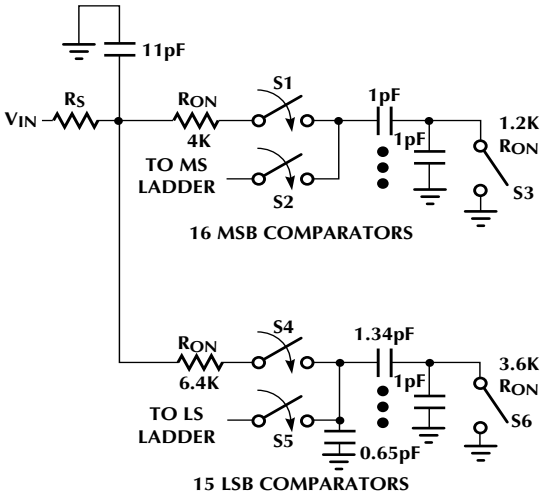


Figure 8. Converter Equivalent Input Circuit

1.3.2 Converter — S/H Mode

The operating sequence for S/H mode is illustrated in Figure 9b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of $\overline{INT}$ closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of $\overline{WR}$ opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while $\overline{WR}$ is low. On the rising edge of $\overline{WR}$, the MSB comparator results are latched. The LSB comparators make their decision when $\overline{WR}$ is high. When the LSB comparison or conversion is complete, $\overline{INT}$ goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of $\overline{RD}$, and the MSB and LSB conversions are generated by internal clock edges that are generated while $\overline{RD}$ is low.

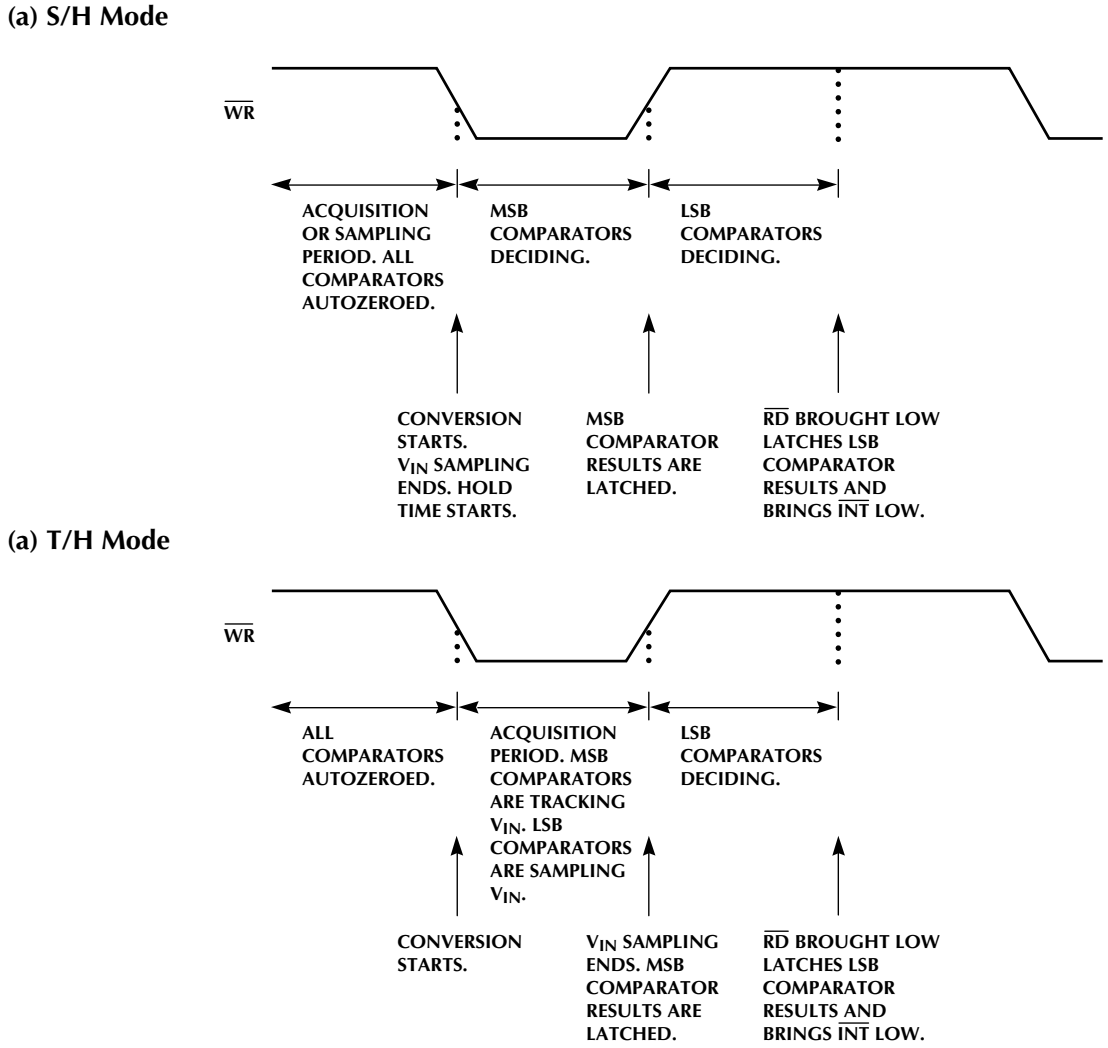


Figure 9. Operating Sequence (WR-RD Mode)

1.4 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 10.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}+$ and $-V_{REF}-$ can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

1.5 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1µF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1µF ceramic disc capacitors at the reference input pins.

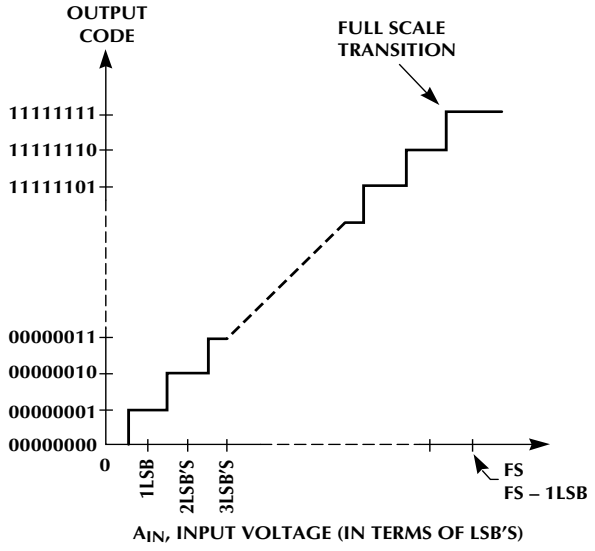


Figure 10. A/D Transfer Characteristic

1.6 DYNAMIC PERFORMANCE

1.6.1 Sinusoidal Inputs

Since the ML2264 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{MAX} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2264 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{190ns + 275ns + 235ns + 300ns}$$

f_{max} = 1.000 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2264. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2264 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_S.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

The Figure 11 plots are 4096 point FFT's of the ML2264 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2264 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measure-ments of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.6.2 Signal-To-Noise Ratio

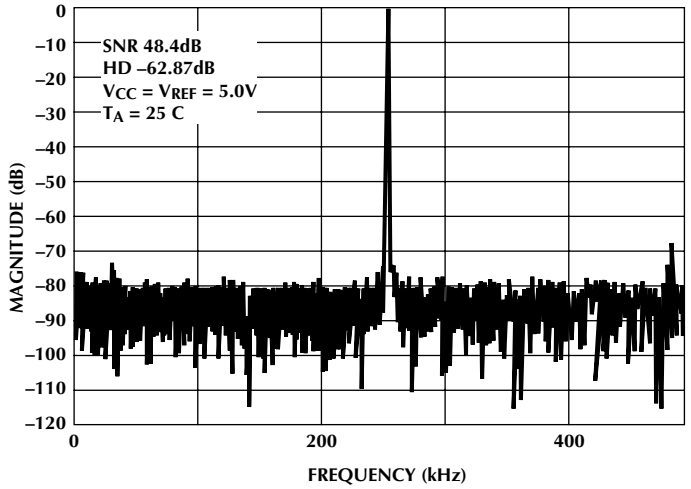
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

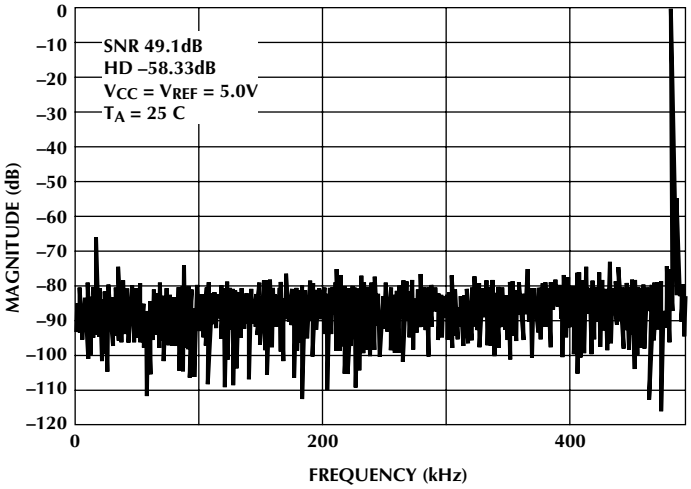
where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.

1.6.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2264 is defined as



a) Output Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 11. Dynamic Performance, Sample and Hold Mode

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.6.2 Signal-To-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

SNR = (6.02N + 1.76) dB

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.

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$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.6.4 Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 … Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and $f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), ($f_A + 2f_B$), and ($f_A - 2f_B$) only.

1.7 DIGITAL INTERFACE

The ML2264 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.7.1 RD Mode

In the RD mode, $\overline{WR}$/RDY pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the µP to start a conversion, wait, and then read data with a single read instruction.

The timing for the RD mode is shown in Figure 4. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high.

1.7.2 WR-RD Mode

In the WR-RD mode, the $\overline{WR}$/RDY pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.7.3 WR-RD Mode — Using Internal Delay ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 5. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when $\overline{RD}$ is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.7.4 WR-RD Mode — Reading Before Delay ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 6. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after WR rising edge and before $\overline{INT}$. $\overline{INT}$ goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before $\overline{INT}$ goes low the data bus always remains in the high-impedance state until $\overline{INT}$¬.

1.7.5 WR-RD Mode — Stand Alone Operation

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 7. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When, $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, $\overline{INT}$ is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.7.6 Power-On Reset

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2264 from starting in an unknown state. During this period of approximately 3µs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS

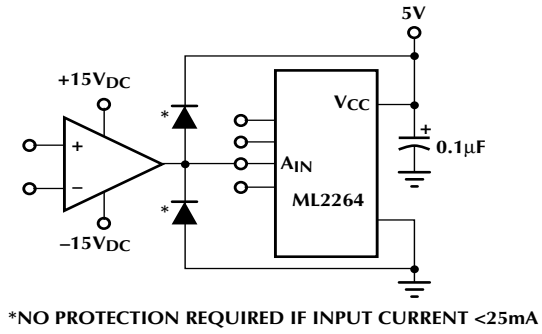


Figure 12. Protecting the Input

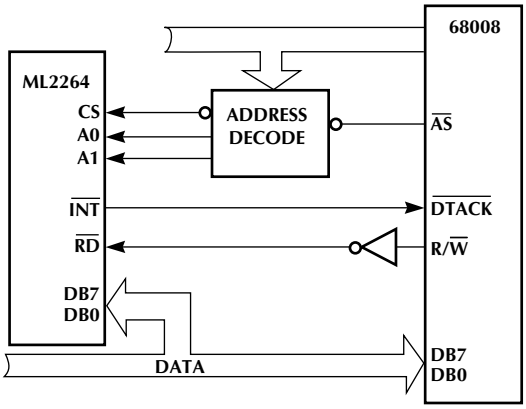


Figure 15. 68000 Type Interface to ML2264

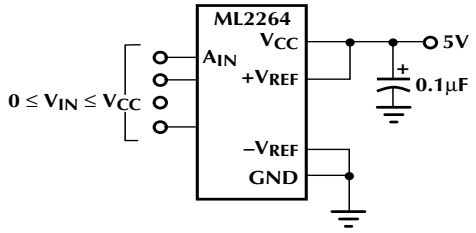


Figure 13. Using V_{CC} as Reference for Ratiometric Operation

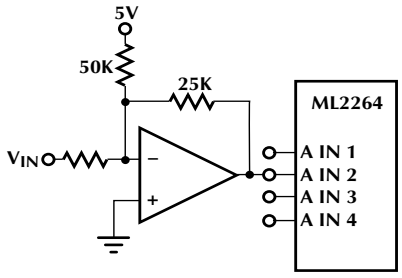


Figure 16. ±2.5V Analog Input Range

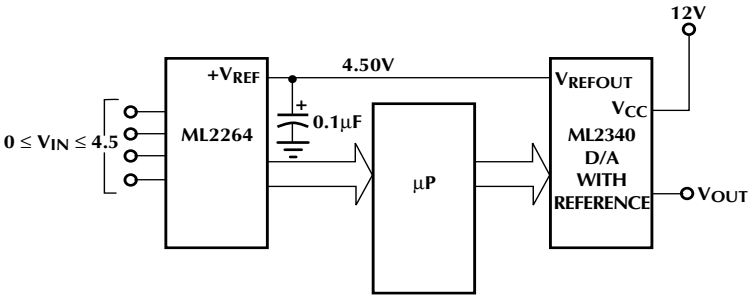


Figure 14. Using External Reference of D/A

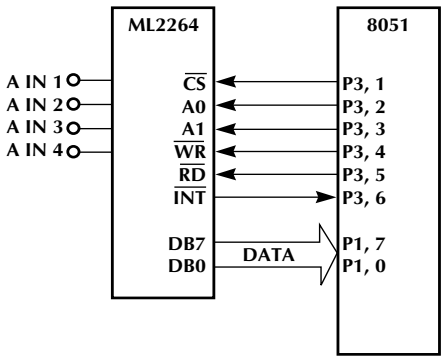


Figure 17. 8051 Interface to ML2264

2.0 TYPICAL APPLICATIONS (Continued)

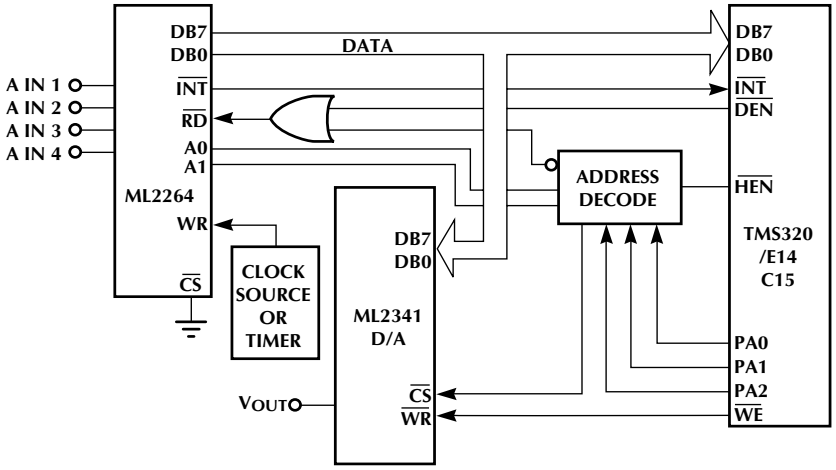


Figure 18. TMS320 Interface with D/A Output

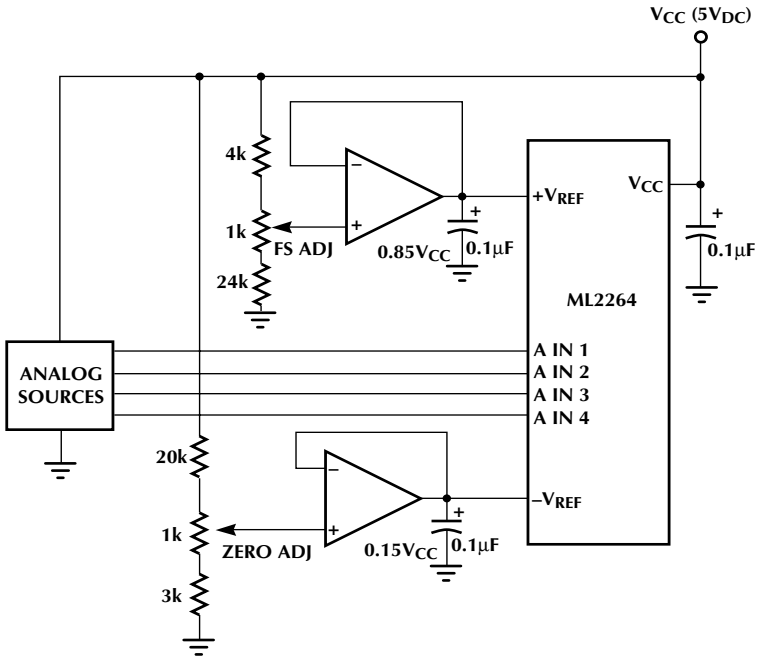
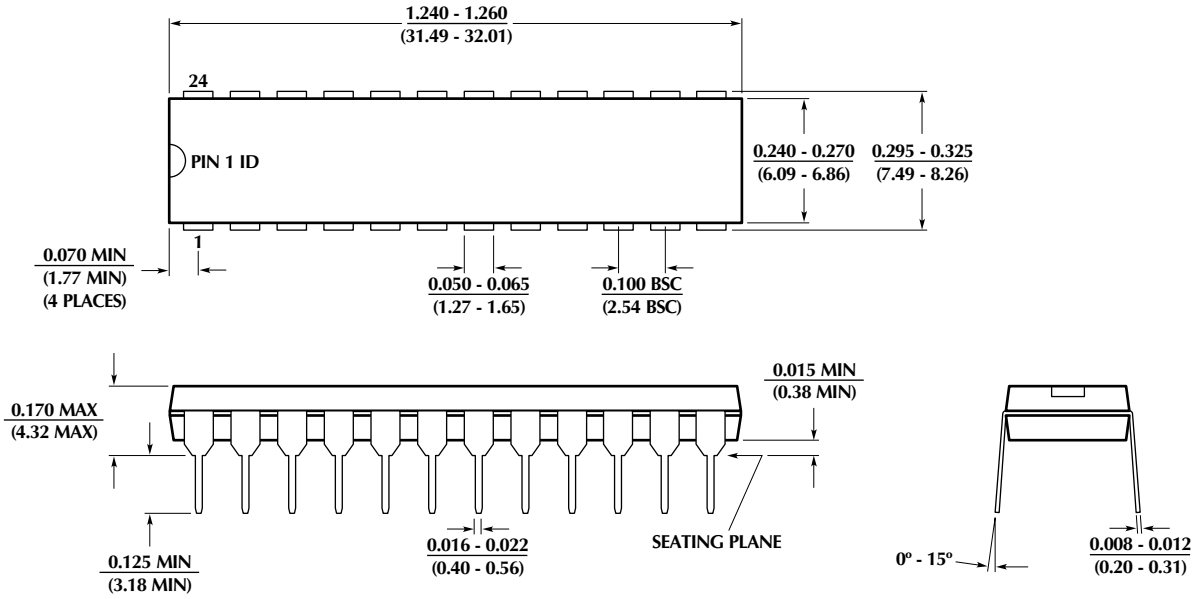


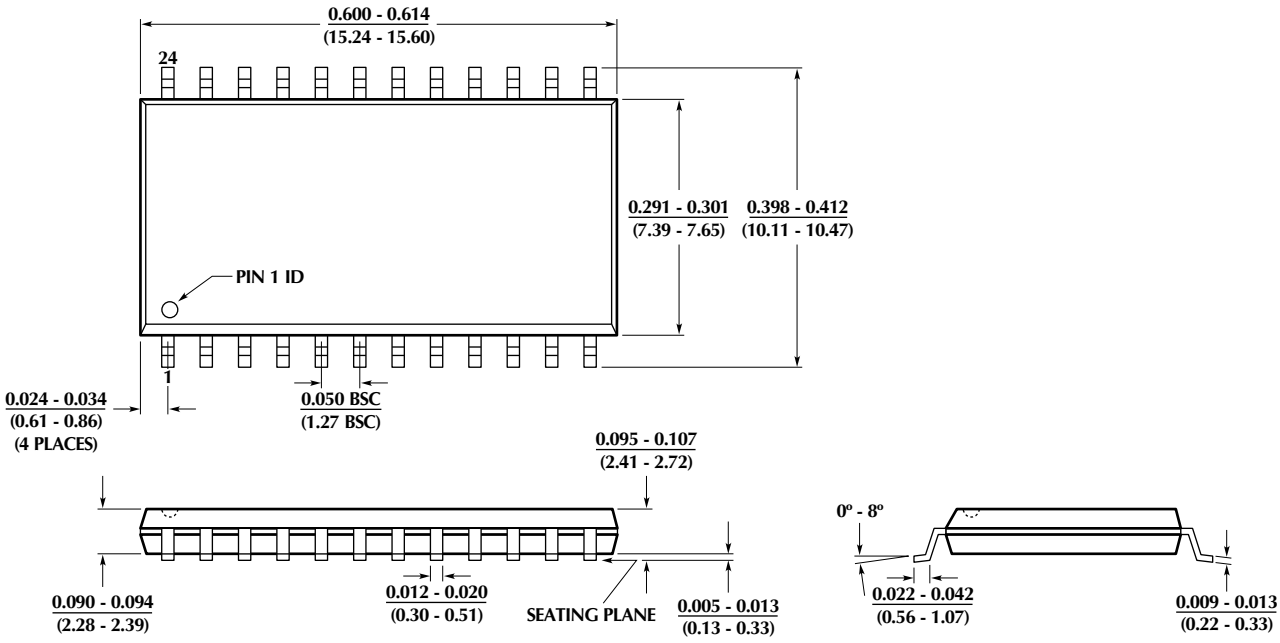
Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

PHYSICAL DIMENSIONS inches (millimeters)

Package: P24N
24-Pin Narrow PDIP

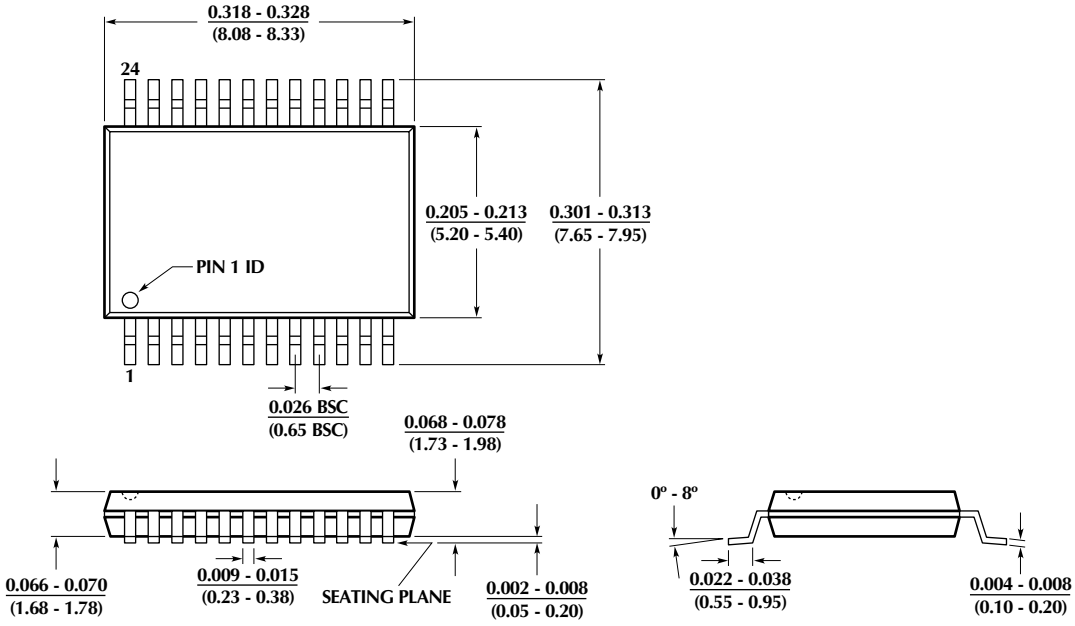


Package: S24
24-Pin SOIC



PHYSICAL DIMENSIONS inches (millimeters) (Continued)

Package: R24
24-Pin SSOP



ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2264CCP (Obsolete)	±1 LSB	0°C to +70°C	Molded DIP (P24)
ML2264CCS (End Of Life)		0°C to +70°C	Molded SOIC (S24)
ML2264CCR (Obsolete)		0°C to +70°C	Molded SSOP (R24)

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