OKI Semiconductor

FEDL2500BFULL-02
Issue Date: Aug.9, 2004

ML2500BTA

Analog-Storage Single-chip Record/Playback LSI with 1M Bit-Cell Flash Memory

GENERAL DESCRIPTION

Thanks to newly developed Analog Multi-Level Storage technology, ML2500B stores non-compressed analog source signal directly into on-chip 1M Bit-Cell Flash memory. The result is superb sound quality without noise and distortions introduced through coding/decoding, and impressive long-time record/playback capability up to 256 sec. ML2500B is fully controllable by an external MCU via the industry's standard Serial Peripheral Interface.
In addition, no backup requirement and low operating voltage (2.7 to 3.3 V) make the LSI an ideal choice for compact, handy and portable terminals. ML2500B is a true single-chip solution to record/playback subsystem for use with today's size-critical electronic products.

DIFFERENCES BETWEEN THE ML2500BTA AND THE ML2500TA

	ML2500BTA	ML2500TA
Operating Temperature	Ta = –40 to +70°C	Ta = –10 to +70°C
Pin Symbol	Pin 10: TEST2	Pin 10: NC
AC Characteristic	DI hold time t_{DIH} = 30 ns	DI hold time t_{DIH} = 20 ns

FEATURES

- On-chip non-volatile 1M bit-cell Flash memory
  - Program/Erase Cycles: 10,000 cycles
  - Data Retention : 10 years
- MCU Interface
  - Serial Peripheral Interface (SPI; Mode 0)
- Record/Playback Time Length (With the int. Osc. or ext. clock at 8.192 MHz)
  - Approx. 160 sec (At fsam = 6.4 kHz)
  - Approx. 190 sec (At fsam = 5.3 kHz)
  - Approx. 256 sec (At fsam = 4.0 kHz)
- Selectable Sampling Frequencies
  - 4.0 kHz, 5.3 kHz, 6.4 kHz
- Maximum number of recording phrases: 320 phrases
- Phrase Control
  - Fully controllable with user-definable Start, Stop addresses
- Built-in LPF/Smoothing Filter (LPF attenuation –40 dB/oct)
- Built-in Oscillation Circuit (8.192 MHz), No oscillator required
  - Optional external clock input (Clock Frequency 4.0 to 8.192 MHz)
- Power Supply : 2.7 to 3.3 V
- Operating Temperature:
  - –40 to +70°C (guaranteed for both function and voice quality)
  - –40 to +85°C (guaranteed for function only) *Notice

*Notice
- The voice quality can deteriorate at temperatures beyond the range of –40 to +70°C.
- DC and AC characteristics in this data sheet are specified for –40 to +70°C operating temperature range.

- Package:
  - 32-pin Plastic TSOP (TSOP(1)32-P-814-0.50-1K) (Product name: ML2500BTA)
  - Note: Please contact the Oki Sales office/Distributors for bare chips.

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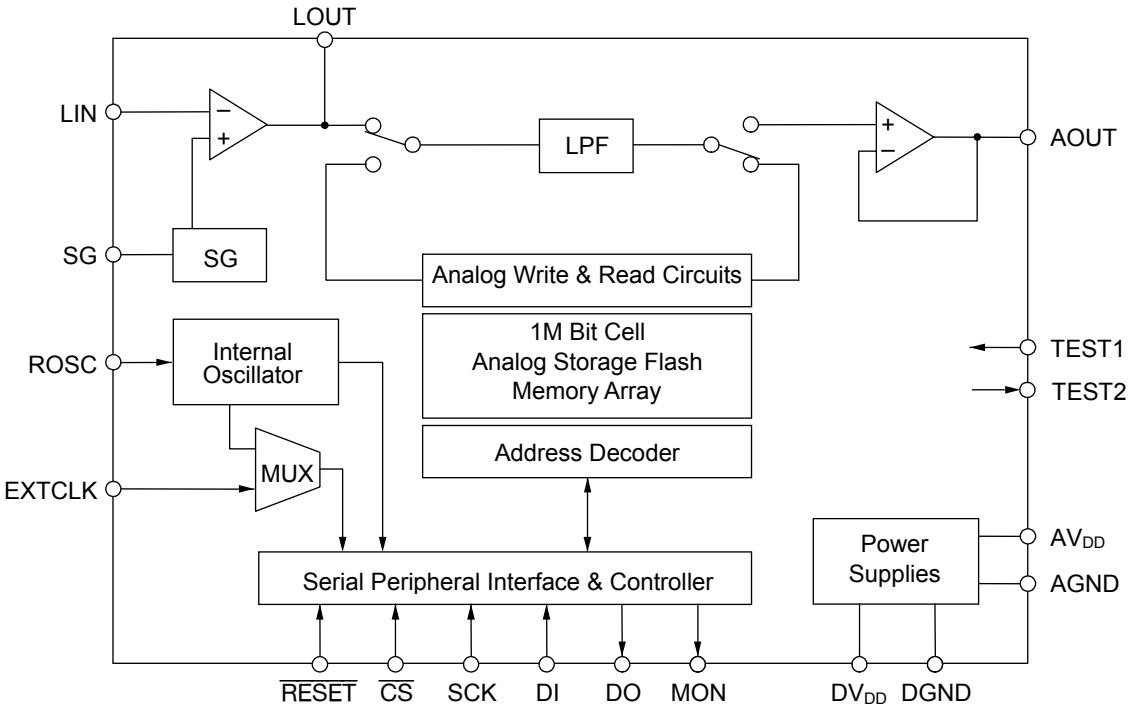
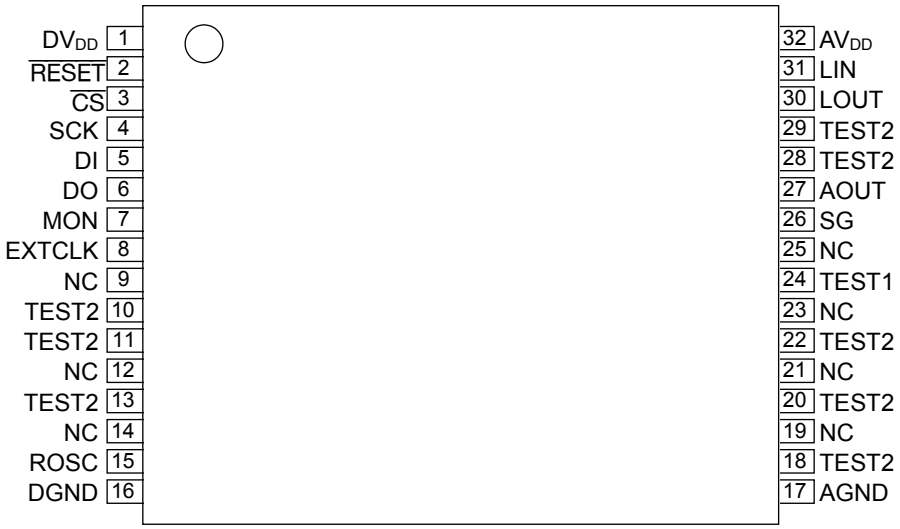
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No connection. Keep NC pins open.

32-Pin Plastic TSOP (Type 1)

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
5	DI	I	Serial input pin for command data.
6	DO	O	Serial output pin for status data.
4	SCK	I	Shift clock input pin for the DI and the DO pins.
3	$\overline{CS}$	I	Chip select pin. “L” level input enables data input/output through the serial interface.
2	$\overline{RESET}$	I	RESET input pin, resetting the serial interface circuit only. “L” level input to this pin initializes the serial interface. Must input “L” pulse after each power-on.
15	ROSC	I	Insert a 30 kΩ resistor (Precision within ±1%) between this pin and the DGND pin. The same resistor should also be inserted if an external clock is used. The resistor value determines the frequency of the clock for control in this device.
8	EXTCLK	I	External clock input pin. Allowable clock frequency range is 4.0 to 8.192 MHz. When external clock is unused and internal oscillation clock is used, connect this pin to the DGND.
7	MON	O	Output “H” level during recording/playback operation.
26	SG	O	Analog reference voltage (Signal Ground Voltage) output pin. It is recommendable to insert a capacitor of 3300 pF or less between this pin and the AGND pin. Loads except for capacitors should not be connected to this pin.
31	LIN	I	Inverting input pin for the internal OP amplifier. Non-inverting input pin is internally connected to SG voltage.
30	LOUT	O	Output pin from the internal OP amplifier.
27	AOUT	O	Analog waveform output. Connect to an amplifier to drive a SP.
10, 11, 13, 18, 20, 22, 28, 29	TEST2	O	Pins for testing the LSI. Must be held “OPEN”.
24	TEST1	I	LSI’s testing pin. Must be connected to DGND.
1	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger by-pass capacitor between this pin and the DGND pin.
16	DGND	—	Digital Ground pin
32	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger by-pass capacitor between this pin and the AGND pin.
17	AGND	—	Analog Ground pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +5.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 3.3			V
Operating Temperature	T_{op}	—	–40 to +70			°C
			Min.	Typ.	Max.	
External Clock Frequency 1 *1	$f_{EXTCLK1}$	—	3.85	4.096	4.34	MHz
External Clock Frequency 2 *1	$f_{EXTCLK2}$	—	7.70	8.192	8.68	MHz

*1: Applicable only with external clock

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = –40 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1	V_{IH}	DGND = AGND = 0 V	0.8 × V_{DD}	—	—	V
"L" Input Voltage *1	V_{IL}	—	—	—	0.2 × V_{DD}	V
"H" Output Voltage *2	V_{OH}	I_{OH} = –40 μA	V_{DD}–0.3	—	—	V
"L" Output Voltage *2	V_{OL}	I_{OL} = 2 mA	—	—	0.45	V
"H" Input Current *1	I_{IH}	V_{IH} = V_{DD}	—	—	10	μA
"L" Input Current *1	I_{IL}	V_{IL} = 0 V	–10	—	—	μA
Operating Current Consumption 1	I_{DD1}	In Recording Operation	—	30	45	mA
Operating Current Consumption 2	I_{DD2}	In Playback Operation	—	20	30	mA
Operating Current Consumption 3	I_{DD3}	In Command-Wait State	—	5	10	mA
Powerdown Current Consumption	I_{DDS}	—	—	—	10	μA

*1: Applied to logic input pins (DI, SCK, $\overline{CS}$, $\overline{RESET}$ and EXTCLK) except ROSC and TEST1 pins.
*2: Applied to logic output pins (DO and MON) except TEST2 pin.

Analog Characteristics

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = –40 to +70°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
LIN Input Impedance *1		R_{LIN}	—	1	—	—	MΩ
Input OP. Amplifier Open Loop Gain*2		G_{OP}	f_{IN} = 0 to 4 kHz	40	—	—	dB
LOUT Load Resistance *3		R_{LOUT}	—	200	—	—	kΩ
AOUT Load Resistance *4		R_{AOUT}	—	50	—	—	kΩ
LOUT Output Voltage Allowance *5	Voice voltage	V_{LOUT}	—	0.5	—	2.2	V
	Beep voltage		With respect to SG voltage	–0.5	—	+0.5	V

*1: Applied to LIN pin.
*2: Applied to LIN and LOUT pins.
*3: Applied to LOUT pin.
*4: Applied to AOUT pin.
*5: Refer to “LOUT Output Voltage Range Allowance” section.

AC Characteristics 1

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = –40 to +70°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
External Clock Duty Cycle		f_{duty}	—	40	50	60	%
$\overline{RESET}$ Pulse Width		t_{RST}	—	1	—	—	µs
Powering up time		t_{PWUP}	—	—	—	1	ms
Power-down Shift Time after PDWN Command Input		t_{PDWN}	—	—	—	100	µs
Power-down Shift Time after "L" Input to $\overline{RESET}$ pin		t_{PDWNR}	—	—	—	100	µs
$\overline{CS}$ "L" Level Pulse Width for Power-down Reset		t_{CSWL}	—	1	—	—	µs
MON Rising Time after REC Command Input *1		t_{RECM}	At fsam = 6.4 kHz	—	—	165	µs
RPM Rising Time after REC Command Input		t_{RECR}	—	—	—	220	ms
MON Rising Time after PLAY Command Input		t_{PLYM}	—	—	—	11	ms
RPM Rising Time after PLAY Command Input		t_{PLYR}	—	—	—	11	ms
MON Falling Time after STOP Command Input	At REC	t_{SPCM}	At fsam = 4.0 kHz	—	—	305	ms
			At fsam = 5.3 kHz	—	—	280	
			At fsam = 6.4 kHz	—	—	266	
	At PLAY *1	t_{SPCM}	At fsam = 6.4 kHz	—	—	165	µs
RPM Falling Time after STOP Command Input	At REC	t_{SPCR}	At fsam = 4.0 kHz	—	—	305	ms
			At fsam = 5.3 kHz	—	—	280	
			At fsam = 6.4 kHz	—	—	266	
	At PLAY *1	t_{SPCR}	At fsam = 6.4 kHz	—	—	165	µs
VPM Bit Rising Time after PAUSE Command Input *1		t_{PSCP}	At fsam = 6.4 kHz	—	—	165	µs
VPM Bit Reset Time after PAUSE Command Input, while Pausing *1		t_{SPCP1}	At fsam = 6.4 kHz	—	—	165	µs
VPM Bit Reset Time after STOP Command Input, while Pausing *1		t_{SPCP2}	At fsam = 6.4 kHz	—	—	165	µs
Sampling Frequency Error When internal oscillation clock is used *2	Absolute Error	Δf_{sam1}	Ta = 25°C, DV_{DD} = AV_{DD} = 3.0 V	–3.0	Defined Frequency	+3.0	%
	V_{DD} Variation Error	Δf_{sam2}	Ta = 25°C, DV_{DD} = AV_{DD} = 2.7 to 3.0 V	–6.0	Defined Frequency	+6.0	
	Temperature Variation Error	Δf_{sam3}	Ta = –40 to +70°C	–3.0	Defined Frequency +Δf_{sam2}	+3.0	

*1: The value changes in proportion to the sampling frequency selected.
*2: When a 30 kΩ resistor is used between ROSC and DGND pins.

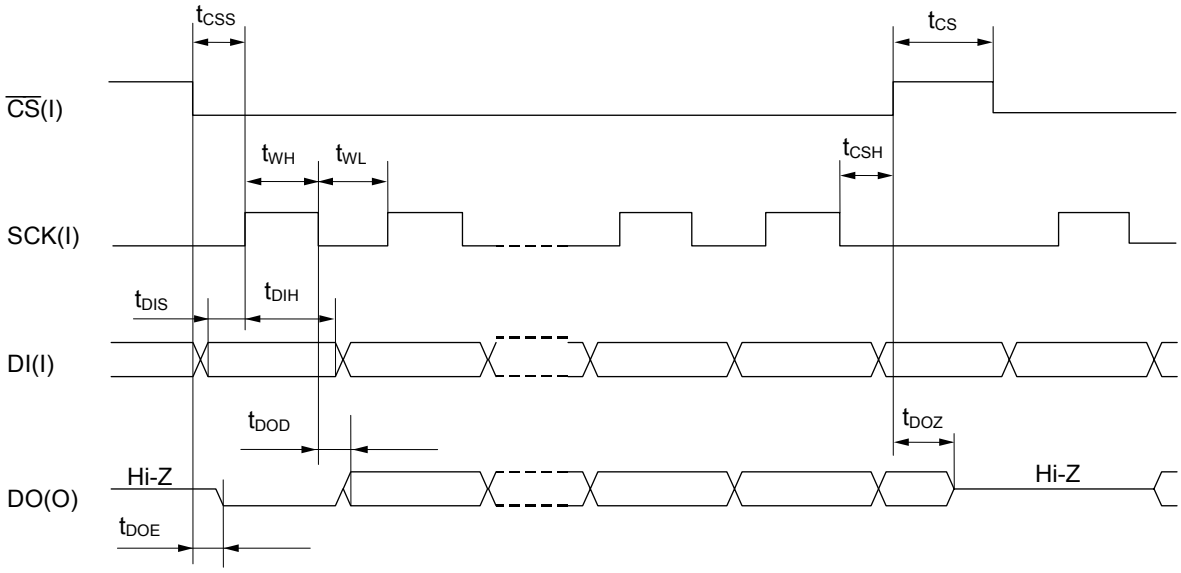
AC Characteristics 2

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = –40 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
$\overline{CS}\downarrow$ – SCK↑ Setup Time	t_{CSS}	—	100	—	—	ns
SCK↓ – $\overline{CS}\uparrow$ Hold Time	t_{CSH}	—	100	—	—	ns
SCK “H” Level Pulse Width	t_{WH}	—	100	—	—	ns
SCK “L” Level Pulse Width	t_{WL}	—	100	—	—	ns
DI Setup Time	t_{DIS}	—	20	—	—	ns
DI Hold Time	t_{DIH}	—	30	—	—	ns
DO Output Delay Time	t_{DOD}	—	—	—	200	ns
DO Output Enable Shift Time	t_{DOE}	—	—	—	150	ns
DO Output Hi-Z Shift Time	t_{DOZ}	—	—	—	150	ns
Command Interval Time	t_{CS}	—	5	—	—	µs

TIMING DIAGRAM

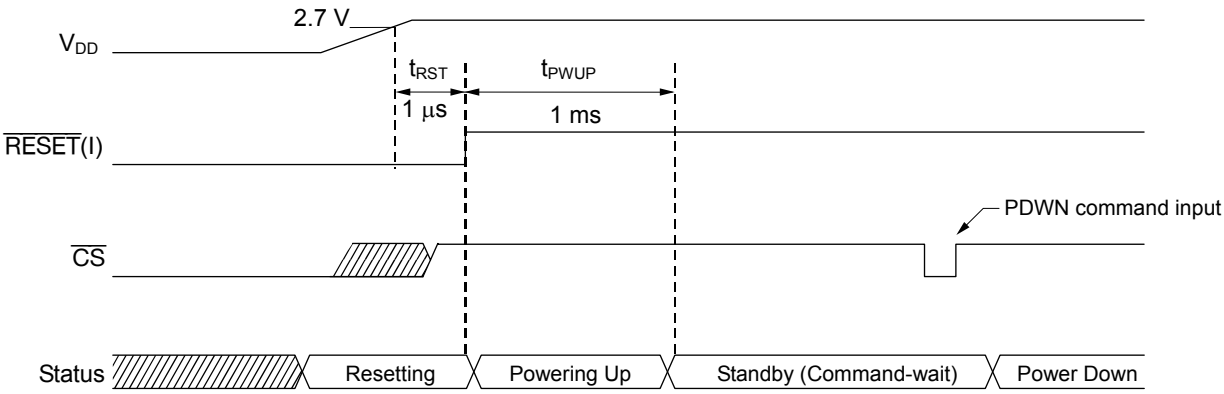
Serial Peripheral Interface (SPI) AC Characteristics Timing Chart



Operational Timing at Power-On

To initialize the internal serial interface circuit of ML2500B after power-on, you must input "L" pulse to the $\overline{\text{RESET}}$ pin at the timing shown below. After this "L" pulse input, the ML2500B enters into standby state (Command-wait state).

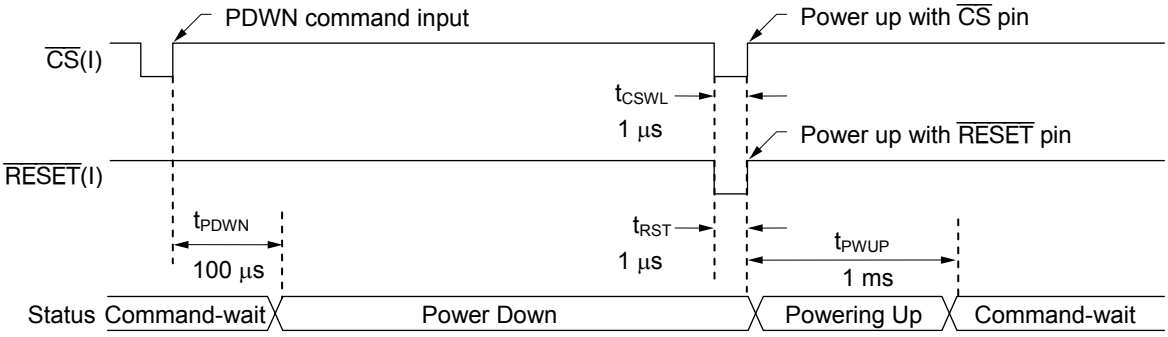
Timing for inputting $\overline{\text{RESET}}$ pulse at Power-on



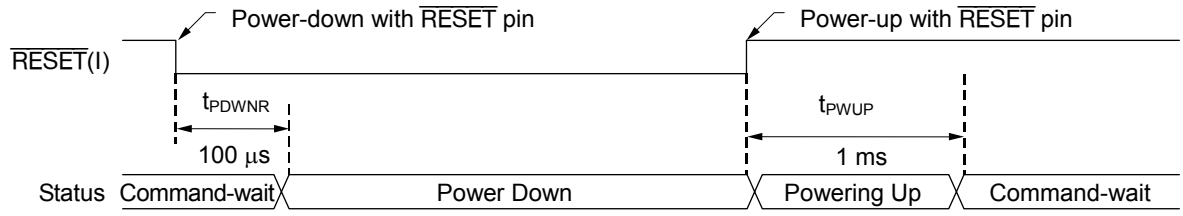
Timing for Power Up and Power Down Operations

ML2500B stops its oscillation circuit to shift to power-down state either by using the PDWN command or by inputting Low level to the $\overline{\text{RESET}}$ pin. In power-down state, the ML2500B turns into low power consumption mode.
Two options are available to power up the LSI again after power down by the PDWN command:
1. Input "L" pulse to the $\overline{\text{RESET}}$ pin, or
2. Input Low level to the $\overline{\text{CS}}$ pin.
The following charts show timings for power up and power down operations.

Timing for power-down operation by using the PDWN command



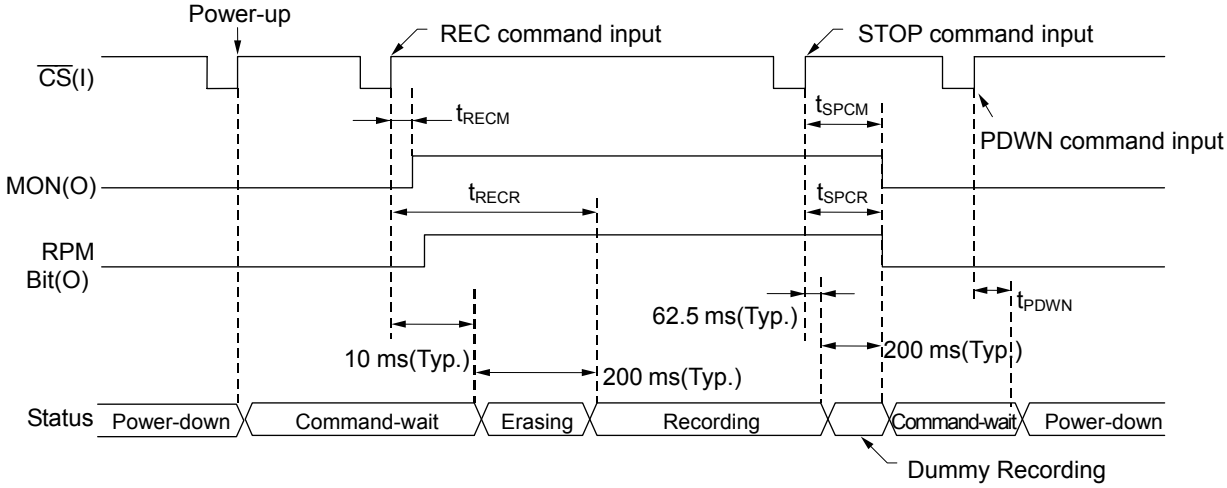
Timing for Power-down operation with $\overline{\text{RESET}}$ pin



Timing for Record/Playback Operation

1. Timing for Recording Operation

The following chart shows timing for recording operation at 6.4 kHz sampling frequency. It is assumed that the Start and Stop Addresses are set by the STADR and SPADR commands prior to the REC command input.



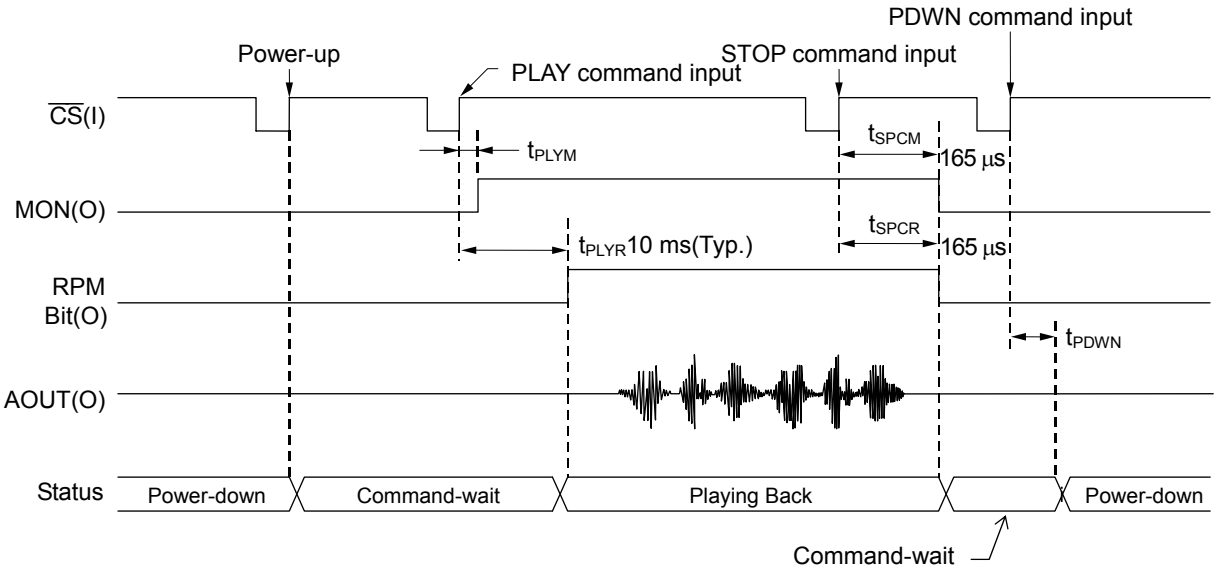
(Note 1) It takes about 210 ms (Typ.) for the LSI to start actual recording after the REC command input, as the LSI first erase 1 sector before it can start recording.

(Note 2) When recording is stopped by the STOP command, the LSI continues to record until the last address of the current page is reached. This "lag" recording time is the STOP command of about 62.5 ms (Typ.). Afterwards, dummy recording is taken place up to the end of the following sector (max. 2 sectors). This dummy recording takes about 200 ms (Typ.). The dummy recording is given in the device specification and the recording contents are undefined.

(Note 3) It is recommended to use the power-down mode in order to reduce power consumption when record or playback are not performed.

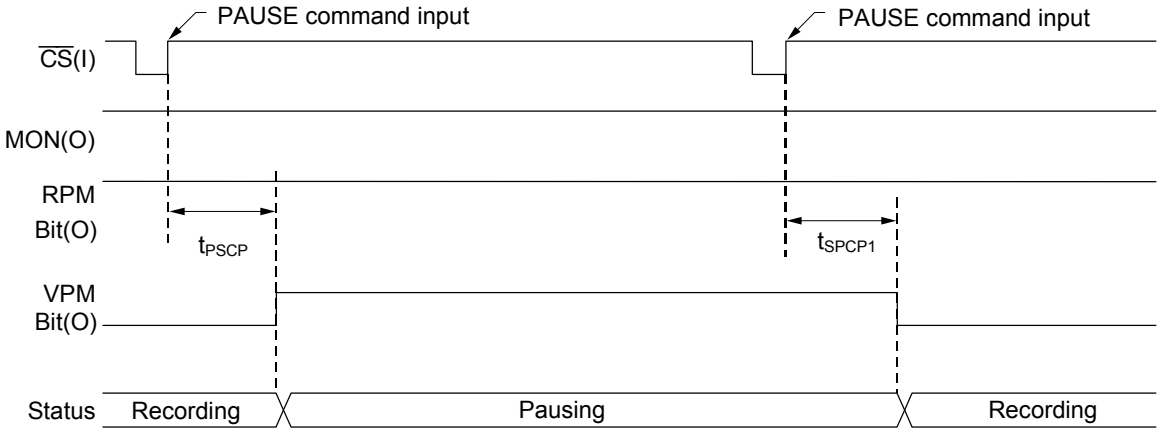
2. Timing for Playback Operation

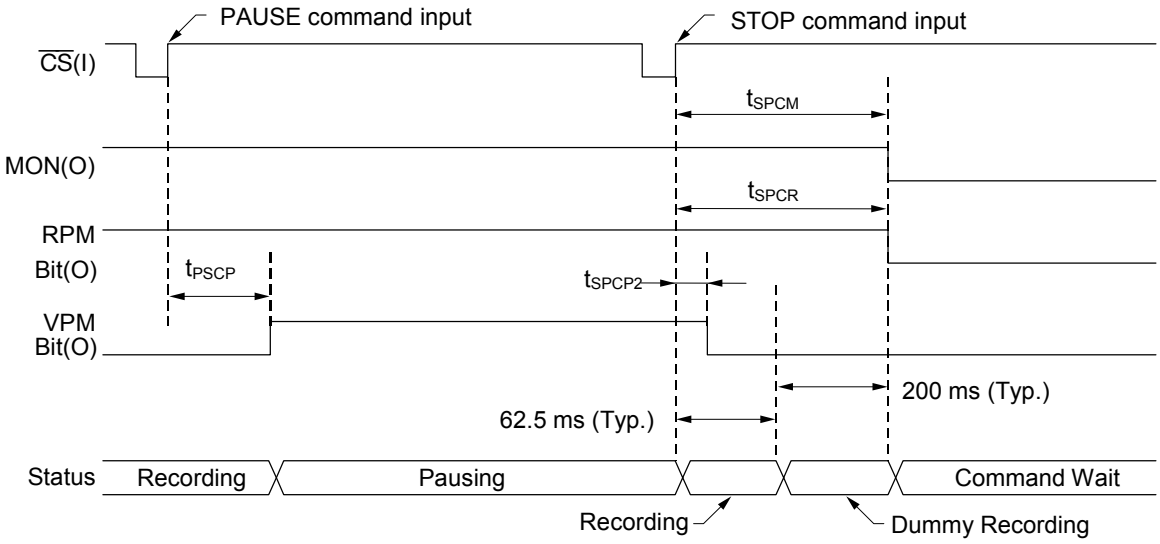
The following chart shows timing for playback operation at 6.4 kHz sampling frequency. It is assumed that the Start and Stop Addresses are set by the STADR and SPADR commands prior to the PLAY command input.



3. Timing for Pausing Operation by the PAUSE Command

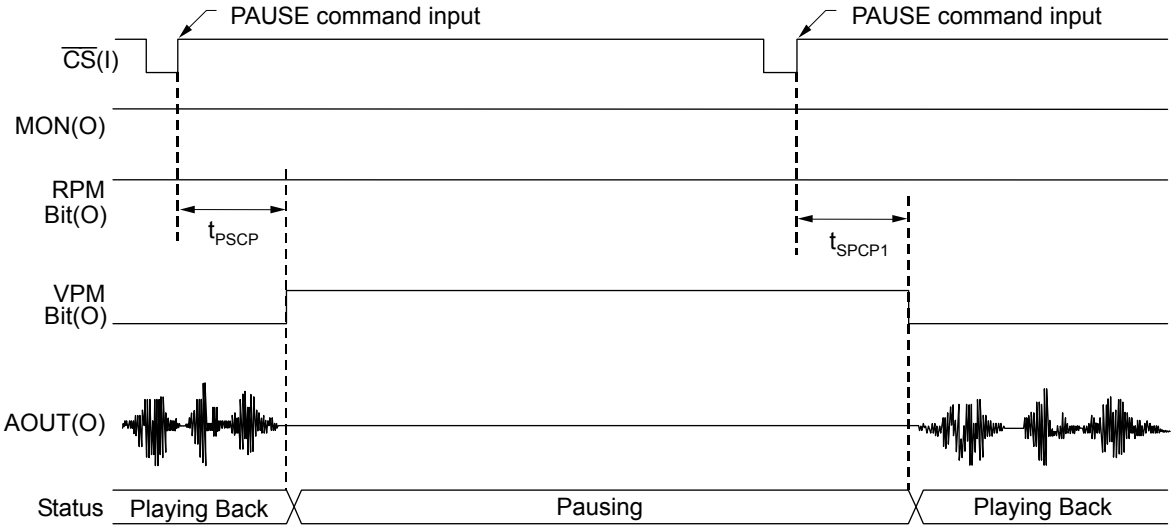
The following charts show timings for pausing recording operation by using the PAUSE command at 6.4 kHz sampling frequency.

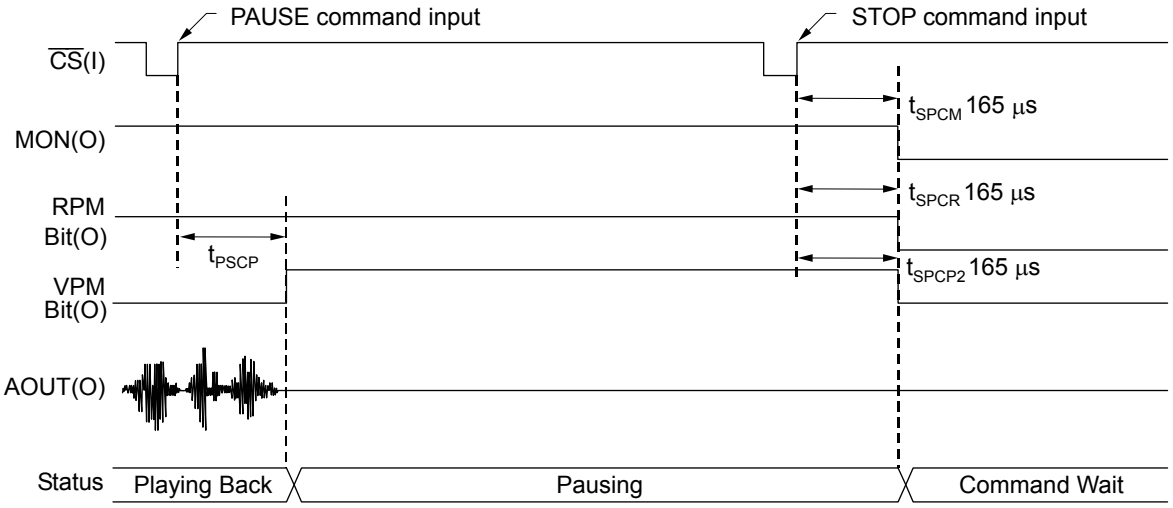




(NOTE) If the STOP command is input while recording is suspended by the PAUSE command, the LSI resumes recording and keeps on recording until the last address of the current page is reached. This “lag” recording time is about 62.5 ms (Typ.).
Afterwards, dummy recording is taken place up to the end of the following sector (max. 2 sectors). This dummy recording takes about 200 ms (Typ.).
The dummy recording is given in the device specification and the recording contents are undefined.

The following charts show timings for pausing playback by using the PAUSE command at 6.4 kHz sampling frequency.





FUNCTIONAL DESCRIPTION

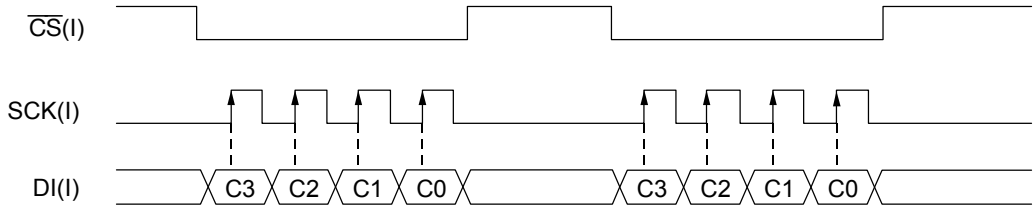
Serial Peripheral Interface (SPI)

ML2500B communicates with the external Micro-Controller Unit through the industry's standard Serial Peripheral Interface (SPI).

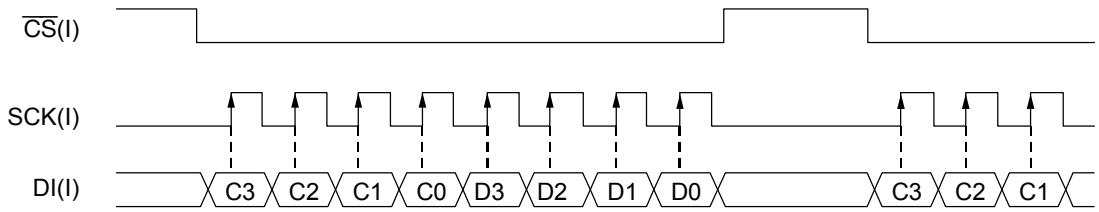
1. Timing for Writing Command Data

The following charts show timings for writing command data. After "L" input to $\overline{CS}$ pin, input command data, starting with the MSB in serial order, to the DI pin in sync with the SCK signal.
The command input to the DI pin is fetched to the LSI's internal shift resister at the rising edge of the SCK signal, and then the command is executed at the rising edge of the $\overline{CS}$ pin. The DI input is either of 4, 8, or 24th bit.
When the $\overline{CS}$ pin is brought to "H" level except at 4/8/24th bit for the command, the command input then is disregarded. It is a recommendable practice to input command data at the falling edge of the $\overline{CS}$ pin while having the SCK pin at "L".

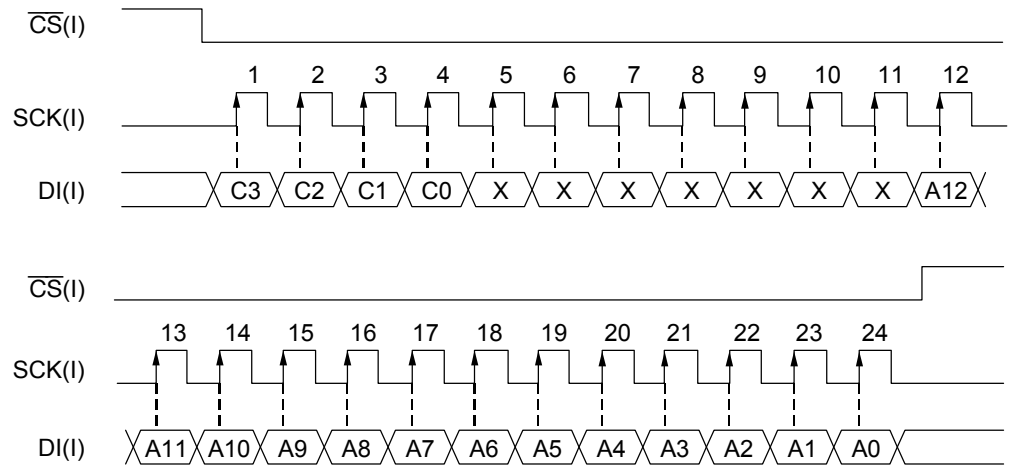
4-bit Command Format



8-bit Command Format



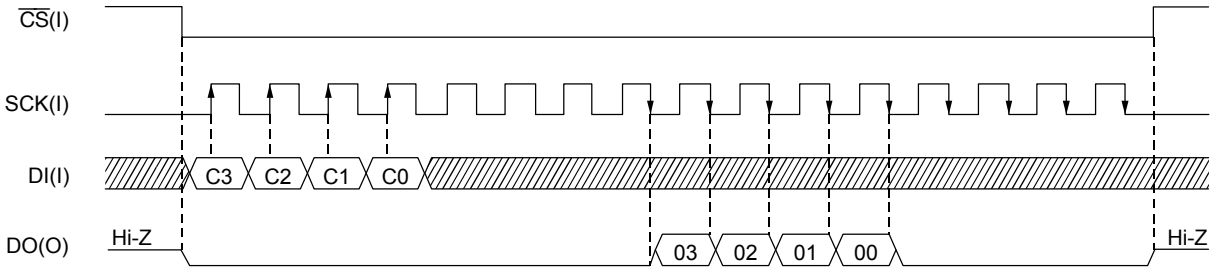
24-bit Command Format



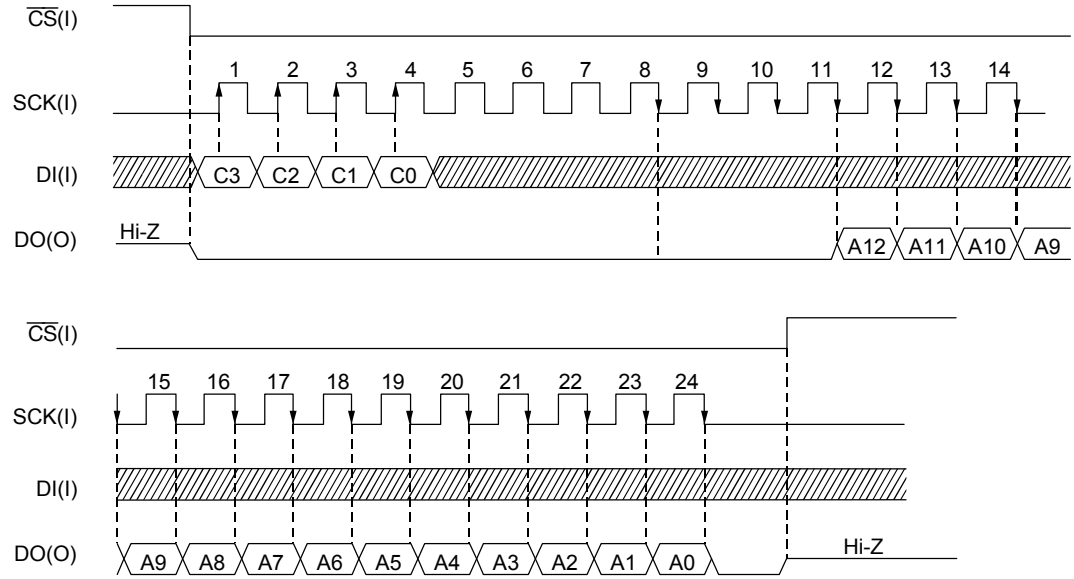
2. Timings for Reading out Status Data

Status data that can be read includes two types, the status register (refer to the section 1.7, RDSTAT Command) and the memory address counter (refer to the section 1.6, RDADR Command).
Timings for reading status data are shown in the charts below. After "L" input to the $\overline{CS}$ pin, input the RDSTAT command to read status data. While the $\overline{CS}$ pin being held "L", status data is output to the DO pin in serial sequence starting with the MSB, in synchronization with the 4th pulse SCK's falling edge following the command input. After reading status data, the DO pin returns to "Hi-Z" status regardless the number of SCK pulse, when the $\overline{CS}$ pin is brought to "H" level.

Status Data Read-Out Timing



Memory Address Counter Read-Out Timing



Control Commands

You can control Record/Playback operations by using 4-bit commands through the serial interface.

1. Control Commands-Recording

The following section describes commands used to control recording:

1.1. REC Command (1XH)

By using the first 4 bits of this command, you can initiate recording, starting at the specified Start Address and recording lasts up to the specified Stop Address. When the specified Stop Address is reached, recording automatically ends up.
4-bit data preceded is to define a sampling frequency, as shown in the table below. When the sampling frequency is not defined with this command, recording is made at the last defined sampling frequency.
When reset and powered up, recording is made at 6.4 kHz (default) sampling frequency.

(With the internal oscillator or the external clock at 8.192 MHz)

Data	Sampling Frequency
0H	4.0 kHz
1H	5.3 kHz
2H	6.4 kHz (Default)

You can specify the Start and Stop Addresses for a recording session by using the STADR and SPADR commands. See 1.4 and 1.5 of this Data Sheet for further details on the STADR and SPADR commands.

1.2. STOP Command (3H)

You can stop recording by using this command. The data following to this command is disregarded.

1.3. PAUSE Command (4H)

You can suspend recording temporarily by using this command. The data following to this command is disregarded.
To re-input the command resumes the suspended operation. If the STOP command is input while recording is suspended by the PAUSE command, the LSI shifts to Record Ending operation and then terminates recording.

1.4. STADR Command (5H)

You can specify the Start Address for recording with 13-bit data preceded by this command.
You need to run the STADR command before you can use the REC command.
Due to the design of memory array configuration, lower 4-bit of 13-bit Start Address defined is automatically set to "0H". For further details, refer to "Addressable Memory Space for Recording" section. When this command is not executed prior to the REC command input, recording starts at the last defined Start Address. After resetting or power-on, the Start Address is set to the memory's starting address as default.

1.5. SPADR command (6H)

You can specify the Stop Address for recording with 13-bit data preceded by this command.
You need to run the SPADR command before you can use the REC command.
When this command is not executed prior to the REC command input, recording ends at the last defined Stop Address. After resetting or power-on, the Stop Address is set to the memory's last address as default.

1.6. RDADR Command (7H)

By using this command you can read the address pointed by the current Memory Address Counter via serial interface. In sync with SCK signal following to the RDADR command, 13-bit Memory Address Counter's value, starting with the MSB, is output to the DO pin. The DO pin's output falls down to "L" level after 13th bit.
Right after recording stops, use this command to read the Stop Address of the phrase that has just been recorded. This allows the external MCU to control addresses for recorded phrases. This command can be input during recording and record pausing. However, running the RDADR command after the STADR (SPADR) command input, lets the LSI output the address defined by the STADR (SPADR) command.

1.7. RDSTAT Command (8H)

By using this command you can read out the values of the internal Status Register via serial interface. Reading the Status Register's values lets you know ML2500B's internal status as shown in the table below.
In sync with SCK signal following to the RDSTAT command bits, 4-bit Status Register's data is output to the DO pin, starting with the MSB. The DO pin's output after 4th bit falls down to the GND level.

Read Bit	Name	Status Description
03	MON	Output "H" level while in record/playback operation, physical recording/playback time plus memory control time. This output is identical value to that of the MON pin.
02	VPM	Output "H" level while recording/playback being suspended by the PAUSE command.
01	RPM	Output "H" level while in record/playback operation, physical recording/playback time only without memory control time.
00	FULL	Output "H" level simultaneously when the MON pin turns "L" level as recording/playback ends by reaching the last address of memory.

2. Control Commands-Playback

The following section describes commands used to control playback:

2.1. PLAY Command (2XH)

By using the first 4 bits of this command, you can initiate playback, starting at the specified Start Address and playback lasts up to the specified Stop Address. When the specified Stop Address is reached, playback automatically stops.
4-bit data preceded is to define a sampling frequency, same as with the REC command. When the sampling frequency is not defined with this command, playback is made last defined sampling frequency.
When reset and powered up, playback is made at 6.4 kHz (default) sampling frequency.
You can specify the Start and Stop Addresses for a playback session by using the STADR and SPADR commands. See 2.4 and 2.5 for further details on the STADR and SPADR commands. When the Start Address and the Stop Address are not defined by STADR and SPADR commands, playback is taken place by using the Start and Stop Addresses defined for the last playback session.

2.2. STOP Command (3H)

You can stop playback by using this command. The data following to this command is disregarded.

2.3. PAUSE Command (4H)

You can temporarily suspend playback by using this command. The data following to this command is disregarded.
Re-inputting this command resumes the suspended operation. If the STOP command is input while playback is suspended by the PAUSE command, the LSI stops playback.

2.4. STADR Command (5H)

You can specify the Start Address for playback with 13-bit data preceded by this command.
You need to run STADR command before you can use the PLAY command.
When this command is not executed prior to the PLAY command input, playback starts at the last defined Start Address. After resetting or power-on, the Start Address is set to the memory's starting address as default.

2.5. SPADR Command (6H)

You can specify the Stop Address for playback with 13-bit data preceded by this command.
You need to run the SPADR command before you can use the PLAY command.
When this command is not executed prior to the PLAY command input, playback ends at the last defined Stop Address. After resetting or power-on, the Stop Address is set to the memory's last address as default.

2.6. RDADR Command (7H)

By using this command you can read the address pointed by the current Memory Address Counter via serial interface. In synchronization with SCK signal following to the RDADR command, 13-bit Memory Address Counter's value, starting with the MSB, is output to the DO pin. The DO pin's output falls down to "L" level after 13th bit. This command can be input during playback and playback pausing.

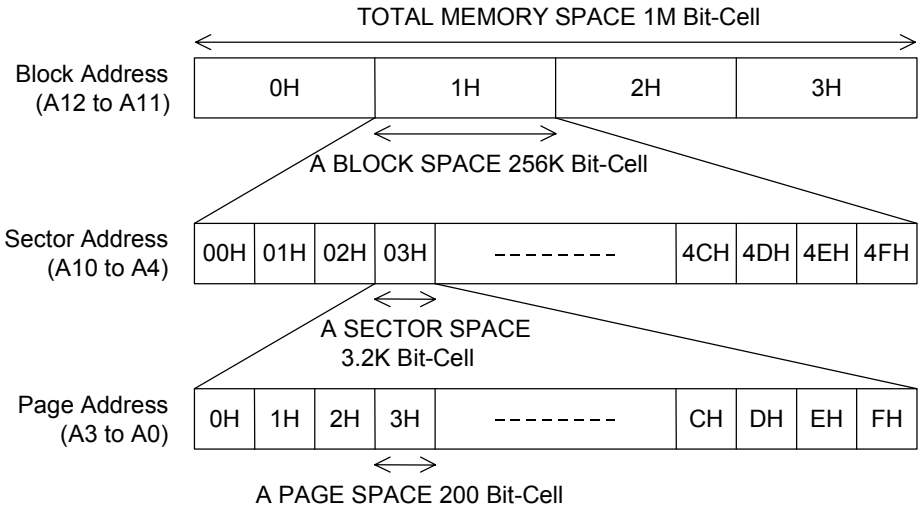
3. The List of Control Commands

Command				Data																				Command Name	Function
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		
0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NOOP	No Particular Function
0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REC	Start recording either at default or last-defined sampling frequency. (Initial frequency: 6.4 kHz)
				0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 4.0 kHz with int. oscillator or ext. clock at 8.192 MHz.
				0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 5.3 kHz with int. oscillator or ext. clock at 8.192 MHz.
				0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 6.4 kHz with int. oscillator or ext. clock at 8.192 MHz.
				0	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 5.3 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
				0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 6.4 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
				0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Record at fsam 4.0 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLAY	Start playback either at default or last-defined sampling frequency. (Initial frequency: 6.4 kHz)
				0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 4.0 kHz with int. oscillator or ext. clock 8.192 MHz.
				0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 5.3 kHz with int. oscillator or ext. clock 8.192 MHz.
				0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 6.4 kHz with int. oscillator or ext. clock 8.192 MHz.
				0	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 5.3 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
				0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 6.4 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
				0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		Playback at fsam 4.0 kHz with ext. clock at 4.096 MHz. *Not supported for int. osc.
0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STOP	Stop Record/Playback
0	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PAUSE	Pause Record/Playback, or reset PAUSE
0	1	0	1	X	X	X	X	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	STADR	Define Start Address for Record/Playback
0	1	1	0	X	X	X	X	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	SPADR	Define Stop Address for Record/Playback
0	1	1	1	X	X	X	X	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	RDADR	Read out Memory Address Counter value
1	0	0	0	X	X	X	X	O3	O2	O1	O0	0	0	0	0	—	—	—	—	—	—	—	—	RDSTAT	Read out Status Register data
1	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PDWN	Power-down to enter into power saving mode

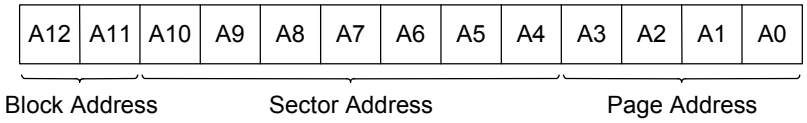
Note: The device is guaranteed for operation for the values included in the list above, so values other than those in the list should not be input.

Addressable Memory Space for Recording

The total memory space of the ML2500B is divided into 4 blocks, 256 K bit-cell for each block, and a block is divided into 80 sectors, 3.2 K bit-cell for each sector. Finally, a sector is divided into 16 pages, 200 bit-cell for each page.
A12 to A11 are assigned to represent a block address, A10 to A4 to represent a sector address, and A3 to A0 to represent a page address.



Address Assignment to Define Block, Sector and Page Address for Start and Stop Address



Prohibit specified addresses for Start Address and Stop Address
These below addresses are prohibited when Start Address or Stop Address is specified.

0500H—07FFH
0D00H—0FFFH
1500H—17FFH
1D00H—1FFFH

Example for setting address

The below table shows the example for Start Address and Stop Address when the memory which is divided into 8 phrases is recorded and played.

Phrase No.	Start Address				Stop Address			
	Block	Sector	Page	Specified Address	Block	Sector	Page	Specified Address
	A12,A11	A10—A4	A3—A0	A12—A0	A12,A11	A10—A4	A3—A0	A12—A0
	[0H—3H]	[00H—4FH]	[0H—FH]		[0H—3H]	[00H—4FH]	[0H—FH]	
CH1	0	00	0	0000	0	27	F	027F
CH2	0	28	0	0280	0	4F	F	04FF
CH3	1	00	0	0800	1	27	F	0A7F
CH4	1	28	0	0A80	1	4F	F	0CFF
CH5	2	00	0	1000	2	27	F	127F
CH6	2	28	0	1280	2	4F	F	14FF
CH7	3	00	0	1800	3	27	F	1A7F
CH8	3	28	0	1A80	3	4F	F	1CFF

Address Control

1. Address Control for Recording

The LSI is designed to make recording in sectors, as the minimum recording unit. When a user sets up the Starting Address for recording by using the STADR command, the page address, lower 4-bit of 13-bit user-defined Starting Address, is automatically set to “0H” internally. Thus recording always begins at the starting address of each sectors.
Meanwhile, when you define the Stop Address for recording by using the SPADR command, full 13-bit address definition is valid. This enables you to specify the Stop Address for recording in pages. However, within the LSI recording continues as far as to the last address of the following sector.

If the RDADR command is used to read the address value of the Memory Address Counter after completion of recording, output value represents the Memory Address Counter’s value either at the time when the Stop Address defined by the SPADR command has been reached, or when the LSI receives the STOP command that causes the LSI to stop recording.

2. Address Control for Playback

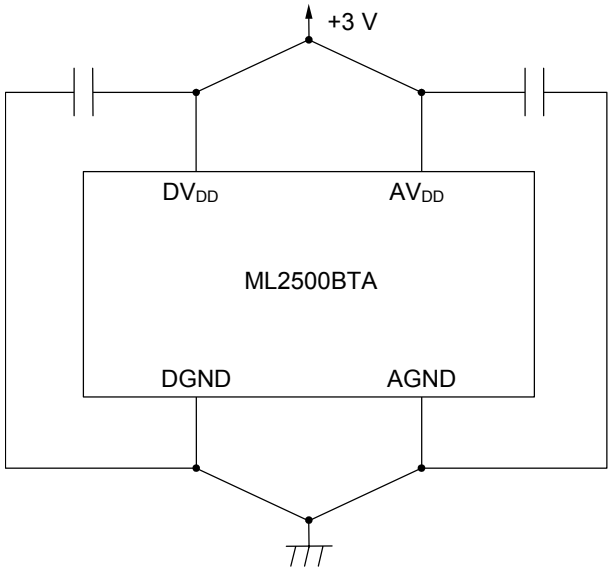
The LSI is designed to make playback in pages, as the minimum playback unit, so full 13-bit address definition is valid both with the STADR command and the SPADR command. You can, therefore, specify the start and stop location by unit of page.

LPF Characteristics

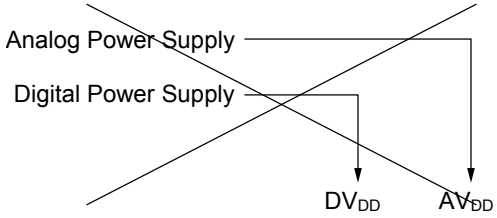
The LSI has an on-chip 4-stage LPF which utilizes Switched Capacitor Filtering technology. Attenuation is set to –40dB/oct. while the cut-off frequency and frequency characteristics vary in proportion to the sampling frequency (fs) selected. The cut-off frequency is set to 0.4 level of the selected sampling frequency.

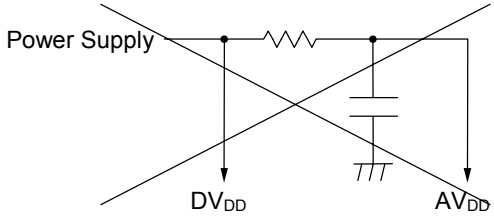
Power Supply Circuit Design

As shown in the following figure, power supply to the LSI must be designed to have a single power source, and separate wiring for analog section and logic section.

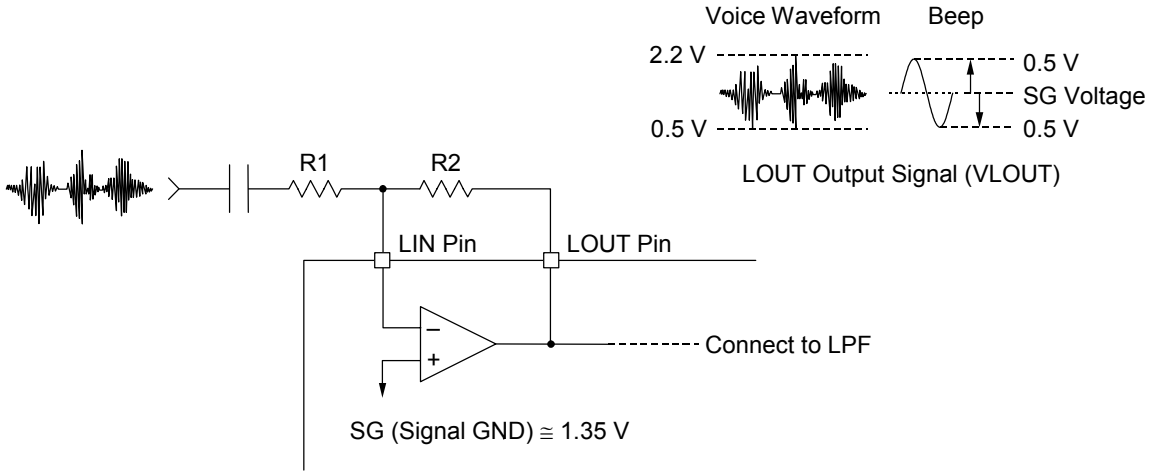


The following figures are bad wiring samples you should avoid.





LOUT Output Voltage Range Allowance



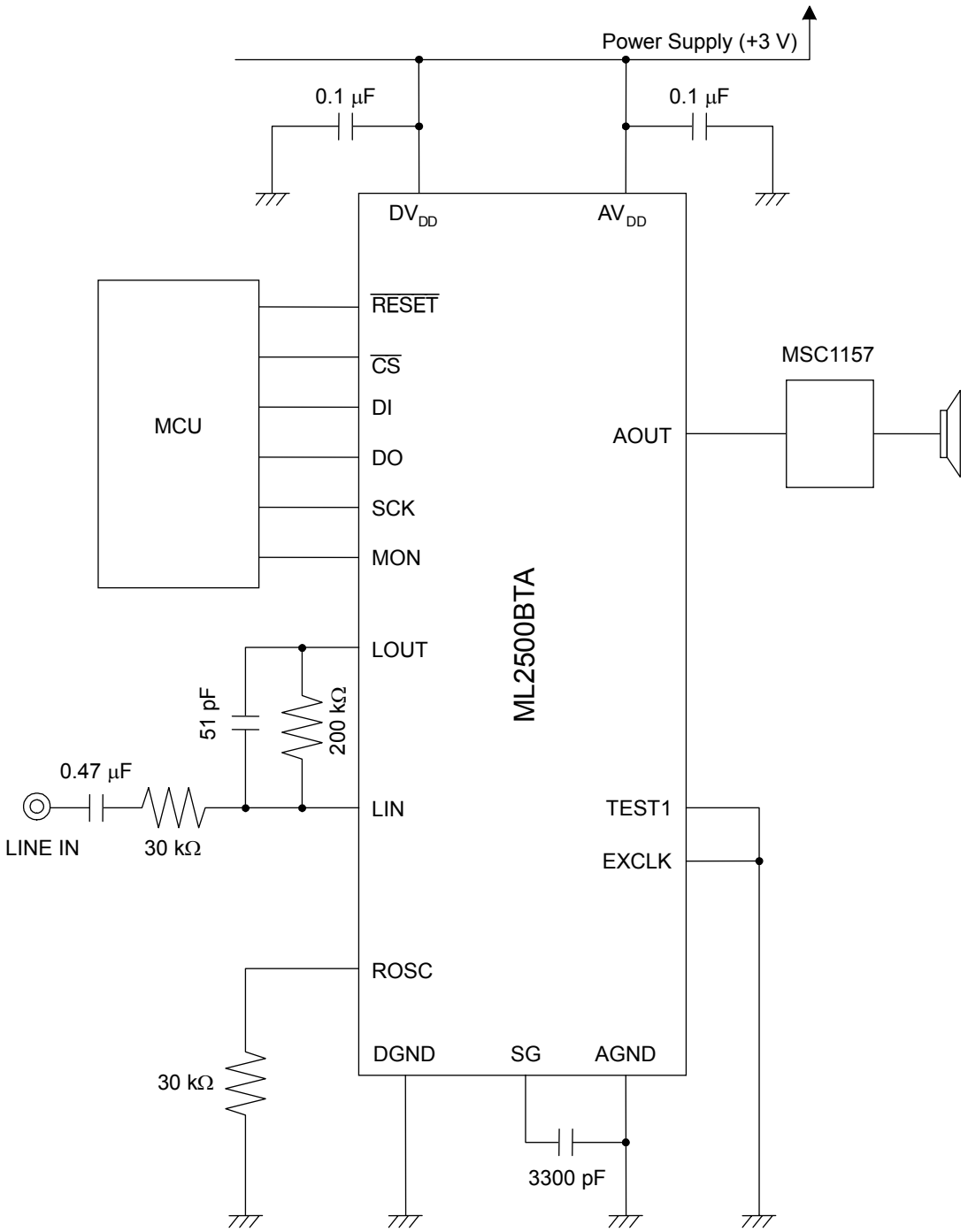
The LSI has a built-in OP amplifier to amplify incoming analog source signal. The inverting input pin to the OP amplifier (LIN pin) and the output pin from the OP amplifier (LOUT pin) are available. The non-inverting input is internally connected to the Reference Voltage (Signal Ground 1.35 V).
As shown in the above wiring sample, the ML2500B is configured so that recording signal can be created through inverting amplifying circuit configured by connecting external resistors, R1 and R2, to the LIN pin and the LOUT pin. The LOUT pin's output voltage (VLOUT) becomes actual recording voltage, and thus is input to the LPF within the LSI.

It is recommended to adjust the amplifying rate so that the dynamic range of the VLOUT voltage will be from 0.5 to 2.2 V for voice input and will be ±0.5 V with respect to the SG voltage for beep.
If the VLOUT voltage exceeds the recommended voltage range, then the LSI's internal LPF's output would be clipped waveform, resulting in degradation of memory reliability.

States of Output Pins during Power Down

Pins	States of output pins during power down
AOUT	GND level
DO	High impedance (Hi-Z)
MON	"L" level
SG	GND level

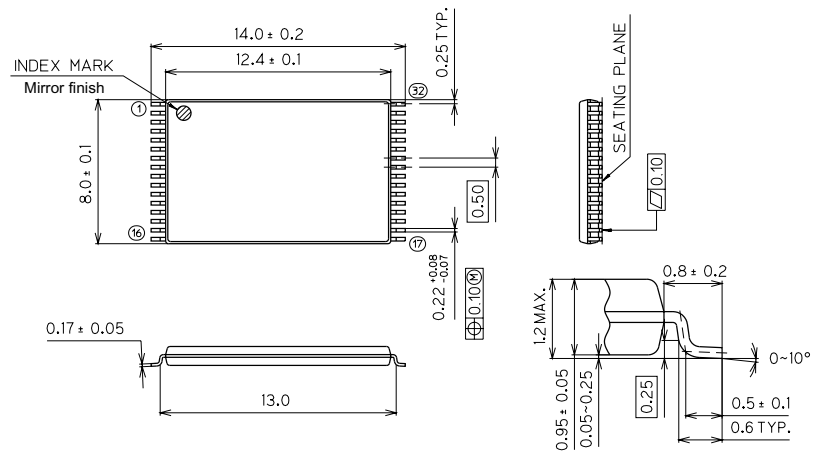
APPLICATION CIRCUITS



PACKAGE DIMENSIONS

(Unit: mm)

TSOP(1)32-P-0814-0.50-1K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.27 TYP.
Rev. No./Last Revised	3/Dec. 10, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2500BFULL-01	Nov, 2000	—	—	Final edition 1
FEDL2500BFULL-02	Aug. 9, 2004	14	14	Corrected the chart of 8bit command and format.
		—	20	Added mentioned about prohibiting specified addresses for Start Address and Stop Address.
		—	21	Added the Example for setting address.

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