

1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 72 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip EPROM size : 1K words
- ◆ Internal RAM size : 72 bytes
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.5 V ~ 4.5 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Sleep Mode for power saving
- ◆ 5 types of oscillator can be selected by programming option:
 - INTRC—Internal 4 MHz RC oscillator
 - RC—Low cost RC oscillator
 - LFXT—Low frequency crystal oscillator
 - XTAL—Standard crystal oscillator
 - HFXT—High frequency crystal oscillator
- ◆ 3 oscillator start-up time can be selected by programming option:
 - 20 ms, 40 ms, 80 ms
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ On-chip RC oscillator based Watchdog Timer(WDT)
- ◆ Wake-up from sleep on pin change

3. Applications

The application areas of this MDT10P55A range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

MDT10P55A1P/MDT10P55A1S				
VDD	1	14	VSS	
PB5	2	13	PB0	
PB4	3	12	PB1	
PB3	4	11	PB2	
PC5/RTCC	5	10	PC0	
PC4	6	9	PC1	
PC3	7	8	PC2	

MDT10P55A2P/MDT10P55A2S				
VDD	1	14	VSS	
OSC1	2	12	PB0	
OSC2/PB4	3	12	PB1	
PB3	4	11	PB2	
PC5/RTCC	5	10	PC0	
PC4	6	9	PC1	
PC3	7	8	PC2	

MDT10P55A3P/MDT10P55A3S				
VDD	1	14	VSS	
PB5	2	13	PB0	
PB4	3	12	PB1	
/MCLR	4	11	PB2	
PC5/RTCC	5	10	PC0	
PC4	6	9	PC1	
PC3	7	8	PC2	

MDT10P55A4P/MDT10P55A4S				
VDD	1	14	VSS	
OSC1	2	13	PB0	
OSC2/PB4	3	12	PB1	
/MCLR	4	11	PB2	
PC5/RTCC	5	10	PC0	
PC4	6	9	PC1	
PC3	7	8	PC2	

5. Pin Function Description

Pin Name	I/O	Function Description
PB5~0	I/O	Port B, TTL input level · PB3 input only.
PC4~0	I/O	Port C, TTL input level
PC5/RTCC	I/O	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

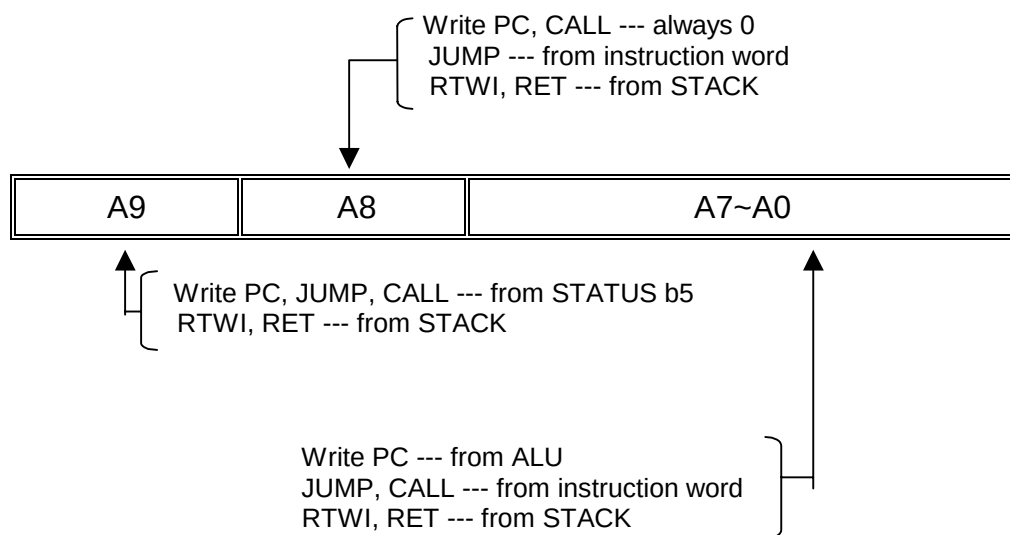
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
06	Port B
07	Port C
08~1F 30~3F 50~5F 70~7F	General purpose registers

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

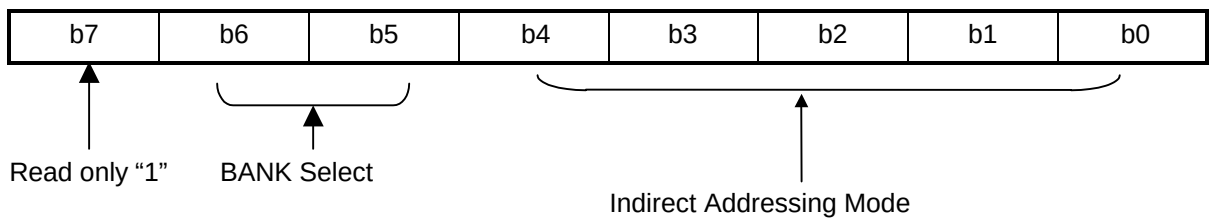
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down bit
4	TF	WDT Timer overflow Flag bit
5	PAGE	ROM page select bit
6	---	Unimplemented
7	PCWUF	Pin change wake up from sleep

(5) MSR (Memory Bank Select Register) : R4



(6) PORT B : R6

PB5~PB0, I/O Register → PB3 input only.

(7) PORT C: R7

PC5~PC0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
2—0	PS2—0	Prescaler Value		
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		

Bit	Symbol	Function
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin
6	PBPHB	PortB pull-high : 0 — Enable 1 — Disable
7	PBWUB	PortB wake-up : 0 — Enable 1 — Disable

(9) CPIO B , CPIO C (Control Port I/O Mode Register)

The CPIO register is "write-only"

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(10) Configurable options for EPROM (Set by writer) :

Oscillator Type	Oscillator Start-up Time
INTRC Oscillator	20ms,40ms,80ms
RC Oscillator	20ms,40ms,80ms
HFXT Oscillator	20 ms,40ms,80ms
XTAL Oscillator	20ms,40 ms,80ms
LFXT Oscillator	20ms,40 ms,80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Security state
Security Disable
Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR Reset	WDT Reset
CPIO B	--	--11 1111	--111 1111	--11 1111
CPIO C	--	--11 1111	--11 1111	--11 1111
TMR	--	1111 1111	1111 1111	--11 1111
IAR	00h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	0000 0000	0000 0000	0000 0000
STATUS	03h	0001 1xxx	#00# #uuu	#00# #uuu
MSR	04h	110x xxxx	11uu uuuu	11uu uuuu
PORT B	06h	--xx xxxx	--uu uuuu	--uu uuuu
PORT C	07h	--xx xxxx	--uu uuuu	--uu uuuu

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"

#=value depends on the condition of the following table

Condition	Status: bit 7	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	0	u	u
/MCLR reset during SLEEP	0	1	0
WDT reset (not during SLEEP)	0	0	1
WDT reset during SLEEP	0	0	0
Wake-up from SLEEP on pin change	1	1	0

9. Instruction Set :

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None

This specification are subject to be changed without notice. Any latest information please preview

Instruction Code	Mnemonic Operands	Function	Operating	Status
010001 1rrrrrrr	STWR R	Store W to register	$W \rightarrow R$	None
011000 trrrrrrr	LDR R, t	Load register	$R \rightarrow t$	Z
111010 iiiiii	LDWI i	Load immediate to W	$I \rightarrow W$	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	$[R(0\sim3) \leftrightarrow R(4\sim7)] \rightarrow t$	None
011001 trrrrrrr	INCR R, t	Increment register	$R + 1 \rightarrow t$	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	$R + 1 \rightarrow t$	None
011011 trrrrrrr	ADDWR R, t	Add W and register	$W + R \rightarrow t$	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	$R - W \rightarrow t$ or $(R+W+1 \rightarrow t)$	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	$R - 1 \rightarrow t$	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	$R - 1 \rightarrow t$	None
010010 trrrrrrr	ANDWR R, t	AND W and register	$R \cap W \rightarrow t$	Z
110100 iiiiii	ANDWI i	AND W and immediate	$i \cap W \rightarrow W$	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	$R \cup W \rightarrow t$	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	$i \cup W \rightarrow W$	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	$R \oplus W \rightarrow t$	Z
110110 iiiiii	XORWI i	Exclu. OR W and immediate	$i \oplus W \rightarrow W$	Z
011111 trrrrrrr	COMR R, t	Complement register	$\neg R \rightarrow t$	Z
010110 trrrrrrr	RRR R, t	Rotate right register	$R(n) \rightarrow R(n-1)$, $C \rightarrow R(7)$, $R(0) \rightarrow C$	C
010101 trrrrrrr	RLR R, t	Rotate left register	$R(n) \rightarrow R(n+1)$, $C \rightarrow R(0)$, $R(7) \rightarrow C$	C
010000 1xxxxxxx	CLRW	Clear working register	$0 \rightarrow W$	Z
010001 0rrrrrrr	CLRR R	Clear register	$0 \rightarrow R$	Z
0000bb brrrrrrr	BCR R, b	Bit clear	$0 \rightarrow R(b)$	None
0010bb brrrrrrr	BSR R, b	Bit set	$1 \rightarrow R(b)$	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if $R(b)=0$	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if $R(b)=1$	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	$n \rightarrow PC$, $PC+1 \rightarrow \text{Stack}$	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	$n \rightarrow PC$	None
110000 nnnnnnnn	CALL n	Call subroutine	$n \rightarrow PC$, $PC+1 \rightarrow \text{Stack}$	None
110001 iiiiii	RTWI i	Return, place immediate to W	$\text{Stack} \rightarrow PC, i \rightarrow W$	None
11001n nnnnnnnn	JUMP n	JUMP to address	$n \rightarrow PC$	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register	0	:	Working register
CPIO	:	Control I/O port register	1	:	General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive 'U'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

10. Oscillator start up timer condition :

Oscillator Type	Power-on reset	Subsequent resets
INTRC,RC	20ms,40ms,80ms	300us
HF,XT,LF	20ms,40ms,80ms	20ms,40ms,80ms

11. Electrical Characteristics

*Note: Temperature=25°C

1. Operation Current :**(1) HF (C=10p) , WDT - enable**

	4M	10M	20M	Sleep
2.5V	400uA	800uA	1.2mA	1.0uA
3.0V	800uA	1.3mA	2.3mA	10uA
4.0V	1.2mA	2.1mA	3.4mA	15uA
4.5V	1.8mA	3.3mA	4.9mA	30uA

These parameters are for reference only.

(2) XT (C=10p) , WDT - enable

	1M	4M	10M	Sleep
2.5V	100uA	250uA	500uA	1.0uA
3.0V	350uA	700uA	1.1mA	10uA
4.0V	500uA	1.1mA	2.0mA	15uA
4.5V	800uA	1.6mA	3.0mA	30uA

These parameters are for reference only.

(3) RC , WDT – Enable , @Vdd = 4.5V

C	R	Freq.	Current
3p	4.7k	7.4M	2.3mA
	10k	2.9M	950uA
	47k	884K	350uA
	100k	452K	200uA
	300k	148K	120uA
	470k	92K	120uA
20p	4.7k	4.2M	1.3mA
	10k	2.2M	750uA
	47k	484K	230uA
	100k	240K	150uA
	300k	80K	120uA
	470k	52K	120uA
100p	4.7k	1.4M	550uA
	10k	736K	300uA
	47k	160K	150uA
	100k	80K	120uA
	300k	27K	120uA
	470k	17K	120uA
300p	4.7k	632K	300uA
	10k	312K	200uA
	47k	68K	120uA
	100k	34K	120uA
	300k	11K	120uA
	470k	7K	120uA

These parameters are for reference only.

(4) LF (C=10p) , WDT - disable

	32K	455K	1M	Sleep
2.5V	30uA	X	X	1.0uA
3.0V	60uA	@3.2V,300uA	@3.2V,300uA	1.0uA
4.0V	150uA	450uA	450uA	1.0uA
4.5V	300uA	750uA	750uA	1.0uA

These parameters are for reference only.

2. Input Voltage (Vdd =4.5V) :

	Port	Min	Max
Vil	TTL	Vss	1.5V
	Schmitt trigger	Vss	0.8V
Vih	TTL	2.5V	Vdd
	Schmitt trigger	3.8V	Vdd

These parameters are for reference only.

3. Output Voltage (Vdd =4. 5V) :

	PA,PB	Condition
Voh	3.4V	Ioh =-20mA
Vol	0.8V	Iol =+20mA
Voh	4.3V	Ioh = -5mA
Vol	0.6V	Iol = +5mA

These parameters are for reference only.

4. Output Current (Max.) (Vdd = 4.5V) :

Port A:		Current
	Source current	25mA
	Sink current	25mA

These parameters are for reference only.

Port B:		Current
	Source current	25mA
	sink current	25mA

These parameters are for reference only.

5. The basic WDT time-out cycle time :

	Time
2.5V	25ms
3.0V	23ms
4.0V	20ms
4.5V	19ms

These parameters are for reference only.

6.

(1)INT_RC, WDT – disable

IC1:		4M	Sleep
	3.0V	900uA	1.0uA
	4.0V	1.5mA	1.0uA
	4.5V	2.1mA	1.0uA

These parameters are for reference only.

(2)INT_RC, WDT – enable

IC1:		4M	Sleep
	3.0V	900uA	5uA
	4.0V	1.5mA	15uA
	4.5V	2.1mA	30uA

These parameters are for reference only.

7. Min Operation Voltage :

C =>	10p	20p	30p
XT, 20M	2.4V	2.4V	2.6V
HF, 20M	2.5V	2.6V	3.0V

These parameters are for reference only.

RC, 1k, no cap.	2.2V
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These parameters are for reference only.

C =>	0p	10p	20p
LF, 1M	2.8V	3.2V	3.4V

These parameters are for reference only.

8. MCLR filter time :

Vdd=5V	
time	2us

These parameters are for reference only.