

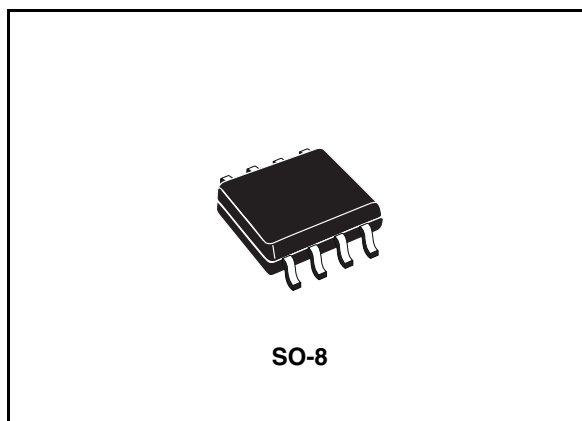


0.5A high-side driver industrial intelligent power switch

Preliminary Data

Features

- 0.5A output current
- 8V to 35V supply voltage range
- Internal current limiting
- Thermal shutdown
- Open ground protection
- Internal negative voltage clamping for fast demagnetization
- Differential inputs with large common mode range and threshold hysteresis
- Undervoltage lockout with hysteresis
- Open load detection
- Two diagnostic outputs
- Output status LED driver
- Non dissipative short circuit protection
- Immunity against burst transient (IEC 61000-4-4)
- ESD protection (human body model $\pm 2\text{kV}$)



Description

The L6375S is a monolithic Intelligent Power Switch in Multipower BCD Technology, for driving inductive or resistive loads with controlled output voltage slew rate and short circuit protection.

An internal Clamping Diode enables the fast demagnetization of inductive loads. Diagnostic for CPU feedback and extensive use of electrical protections make this device extremely rugged and specially suitable for industrial automation applications.

Table 1. Device summary

Order codes	Op. temp. range, °C	Package	Packaging
L6375S	-25 to +125	SO-8	Tube
L6375STR	-25 to +125	SO-8	Tape & Reel

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1 Block diagram and pin description

Figure 1. Block diagram

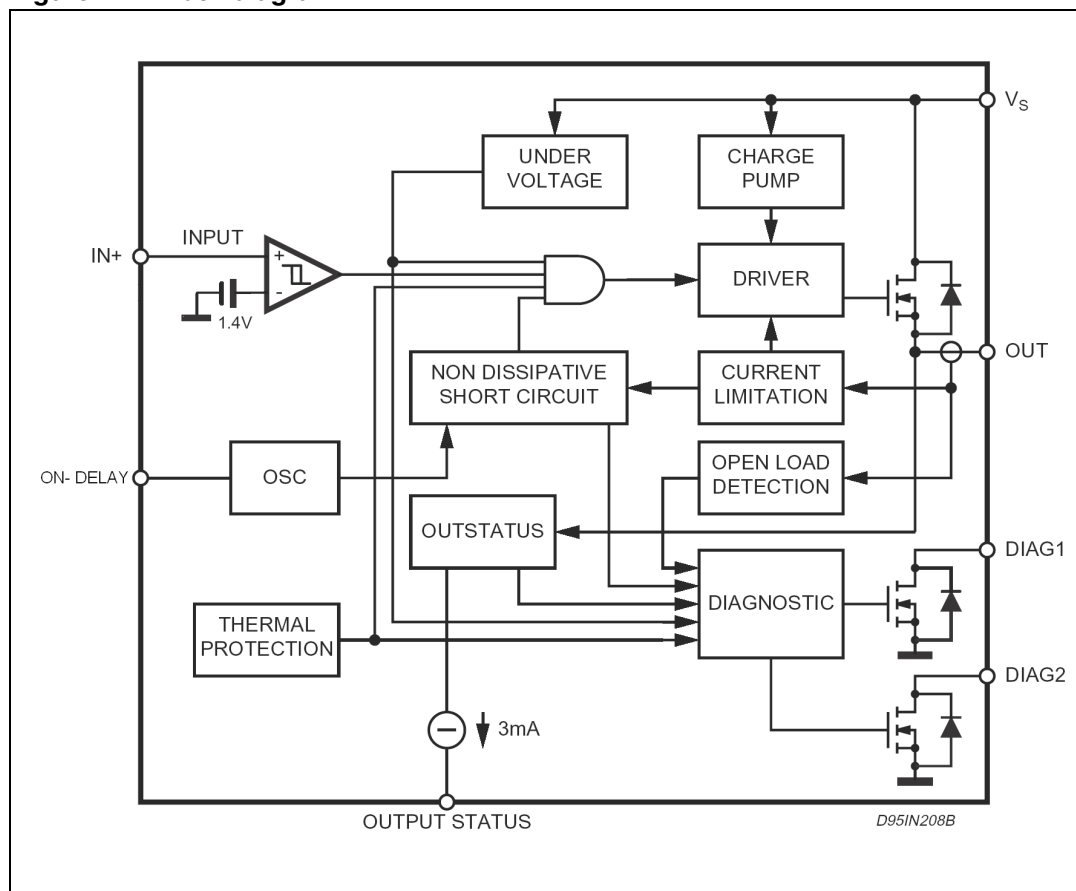
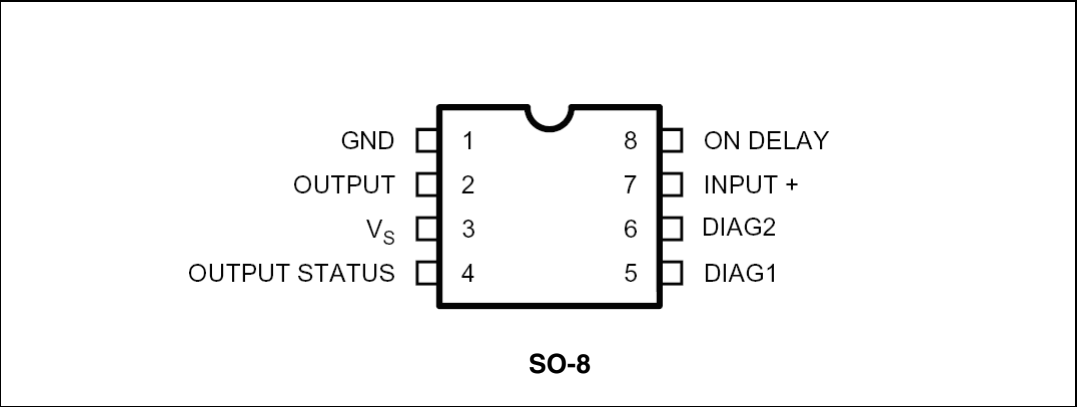


Figure 2. Pin connection (top view)



1.1 Pin description

Table 2. Pin description

Pin N°	Pin name	Function
1	GND	Ground
2	OUT	High Side output with built-in current limitation
3	V_S	Supply Voltage Input, the value of the supply voltage is monitored to detect under voltage condition
4	Output status	This current source output is capable of driving a LED to signal the status of the output pin. The pin is active (source current) when the output pin is considered high (See Figure 4)
5	DIAG1	DIAGNOSTIC 1 output. This open drain reports the IC working conditions. (See Diagnostic truth Table 6)
6	DIAG2	DIAGNOSTIC 2 output. This open drain reports the IC working conditions. (See Diagnostic truth Table 6)
7	IN+	Comparator inverting input
8	ON-DELAY	Programmable ON time interval duration during short circuit operation

2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _s	Supply voltage (tw < 10 ms)	50	V
V _s	Supply voltage (DC)	40	V
V _s -V _{out}	Supply to output differential voltage	internally limited	V
V _{od}	Externally forced voltage	-0.3 to 7	V
I _{od}	Externally forced current	±1	mA
I _{out}	Output current (see also I _{sc})	internally limited	A
V _{out}	Output voltage	internally limited	V
P _{TOT}	Power dissipation	internally limited	W
V _{diag}	External voltage	-0.3 to 40	V
I _{diag}	Externally forced current	-10 to 10	mA
I _i	Input current	20	mA
V _i	Input voltage	-10 to V _s +0.3	V
T _{op}	Ambient temperature, operating range	-25 to 85	°C
T _J	Junction temperature, operating range (see Overtemperature Protection)	-25 to 125	°C
T _{STG}	Storage temperature	-55 to 150	°C
E _I	Energy inductive load T _J = 85°C	200	mJ

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA}	Thermal resistance junction-ambient Max	100 ⁽¹⁾	°C/W
R _{thJP}	Thermal resistance junction-pins Max	15	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35µm) thick connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Table 5. Electrical characteristics
($V_S = 24V$; $T_J = -25$ to $+125^\circ C$, unless otherwise specified)

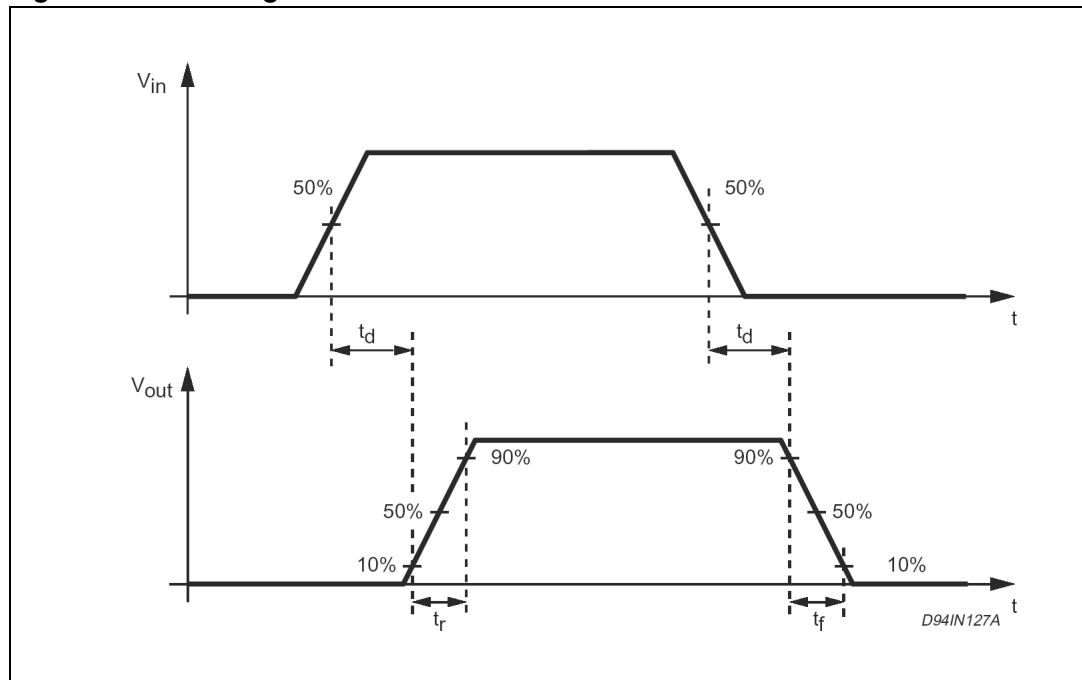
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{smin}	Supply voltage for valid diagnostic	$I_{diag} = > 0.5mA$; $V_{diag} = 1.5V$;	4		35	V
V_S	Operative supply voltage		8	24	35	V
V_{sth1}	Undervoltage threshold 1		7	7.5	8	V
V_{sth2}	Undervoltage threshold 2		6.5	7	7.5	V
V_{shys}	Under voltage hysteresis		300	500	700	mV
I_q	Quiescent current	Output open		800		μA
I_{qo}	Quiescent current	Output ON		1.6		mA
V_{ith}	Input threshold voltage		0.8	1.3	2	V
V_{iths}	Input threshold hysteresis		50		400	mV
V_{il}	Input low level voltage		-7		0.8	V
V_{ih}	Input high level voltage	$V_S < 18V$	2		$V_S - 3$	V
V_{ih}	Input high level voltage	$V_S > 18V$	2		15	V
I_{ib}	Input bias current	$V_i = -7$ to $15V$	-250		250	mA
I_{dch}	Delay capacitor charging current	ON DELAY pin shorted to Ground		2.5		mA
V_{don}	Output voltage drop	$I_{out} = 500mA$ $T_J = 25^\circ C$ $T_J = 125^\circ C$ $I_{out} = 625mA$ $T_J = 25^\circ C$ $T_J = 125^\circ C$		200 320 250 400	280 440 350 550	mV mV mV mV
I_{olk}	Output leakage current	$V_i = LOW$; $V_{out} = 0$			100	μA
V_{ol}	Output low state voltage	$V_i = HIGH$; pin floating		0.8	1.5	V
V_{cl}	Internal voltage clamp ($V_S - V_{out}$)	$I_o = 200mA$ single pulsed = 300ms	48	53	58	V
I_{sc}	Short circuit output current	$V_S = 8$ to $35V$; $R_l = 2\Omega$;	0.75	1.1	1.5	A
I_{old}	Open load detection current	$V_i = V_{ih}$; $T_A = 0$ to $+85^\circ C$	1	3	6	mA
V_{oth1}	Output status threshold 1 voltage		4.5	5	5.5	V
V_{oth2}	Output status threshold 2 voltage		4	4.5	5	V
V_{ohys}	Output status threshold hysteresis		300	500	700	mV
I_{osd}	Output status source current	$V_{out} > V_{oth1}$; $V_{os} = 2.5V$	2		4	mA

Table 5. Electrical characteristics (continued)
($V_S = 24V$; $T_J = -25$ to $+125^\circ C$, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{osd}	Active output status driver drop voltage	$V_S - V_{OS}$; $I_{OS} = 2mA$ $T_A = 0$ to $+85^\circ C$		1.5	3	V
I_{oslk}	Output status driver leakage current	$V_{out} < V_{oth2}$; $V_{OS} = 0V$ $V_S = 18$ to $35V$			25	mA
V_{dgl}	Diagnostic drop voltage	$D1 / D2 = L$; $I_{diag} = 0.5mA$ $D1 / D2 = L$; $I_{diag} = 3mA$		40 250		mV mV
I_{dglk}	Diagnostic leakage current	$D1 / D2 = H$; $0 < V_{dg} < V_S$ $V_S = 15.6$ to $35V$			5	μA
T_{max}	Over temperature upper threshold			150		$^\circ C$
T_{hys}	Over temperature hysteresis			20		$^\circ C$
AC operation (pin numbering referred to Minidip package)						
$t_r - t_f$	Rise or fall time	$V_S = 24V$; $R_I = 70\Omega$ R_I to ground		20		μs
t_d	Delay time	$V_S = 24V$; $R_I = 70\Omega$ R_I to ground		5		μs
dV/dt	Slew rate (rise and fall edge)		7	1	15	V/ μs
t_{ON}	On time during short circuit condition	$50pF < C_{DON} < 2nF$		1.28		$\mu s/pF$
t_{OFF}	Off time during short circuit condition			64		t_{ON}
f_{max}	Maximum operating frequency			25		KHz
Source drain NDMOS diode						
V_f	Forward on voltage	@ $I_{fsd} = 625mA$		1	1.5	V
I_{fD}	Forward peak voltage	$t = 10ms$; $d = 20\%$			2	A
t_{rr}	Reverse recovery time	$I_f = 625mA$ $di/dt = 25A/ms$		200		ns
t_{fr}	Forward recovery time			50		ns

2.4 Switching waveform

Figure 3. Switching waveform



2.5 Input section

An Single ended Input TTL/CMOS compatible with wide voltage range and high noise immunity (thanks to a built in hysteresis) is available.

2.6 Over temperature protection (OVT)

An on-chip Over Temperature Protection provides an excellent protection of the device in extreme conditions. Whenever the temperature - measured on a central portion of the chip exceeds $T_{max} = 150^{\circ}\text{C}$ (typical value) the device is shut off, and the DIAG2 output goes LOW. Normal operation is resumed as the chip temperature (normally after few seconds) falls below $T_{max} - T_{hys} = 130^{\circ}\text{C}$ (typical value). The hysteresis avoid that is an intermittent behavior take place.

2.7 Under voltage protection (UV)

The supply voltage is expected to range from 8 to 35V. In this range the device operates correctly. To avoid any misfunctioning the supply voltage is continuously monitored to provide an under voltage protection. As V_s falls below $V_{sth} - V_{shys}$ (typically 7.5 V, see fig.1) the output power MOS is switched off and DIAG1 and DIAG2 (see Diagnostic truth table). Normal operation is resumed as soon as V_s exceeds V_{sth} . The hysteretic behavior prevents intermittent operation at low supply voltage.

2.8 Over current operation

In order to implement a short circuit protection the output power MOS is driven in linear mode to limit the output current to the I_{sc} (1.1A typical value). This condition (current limited to the I_{sc} value) lasts for a T_{on} time interval, that can be set by means of a capacitor (C_{don}) connected to the ON DELAY pin according to the following formula:

$$T_{on} = 1.28 \mu\text{sec/pF}$$

for

$$50\text{pF} < C_{don} < 2\text{nF}$$

After the T_{on} interval has expired the output power MOS is switched off for the T_{off} time interval with:

$$T_{off} = 64 \cdot T_{on}$$

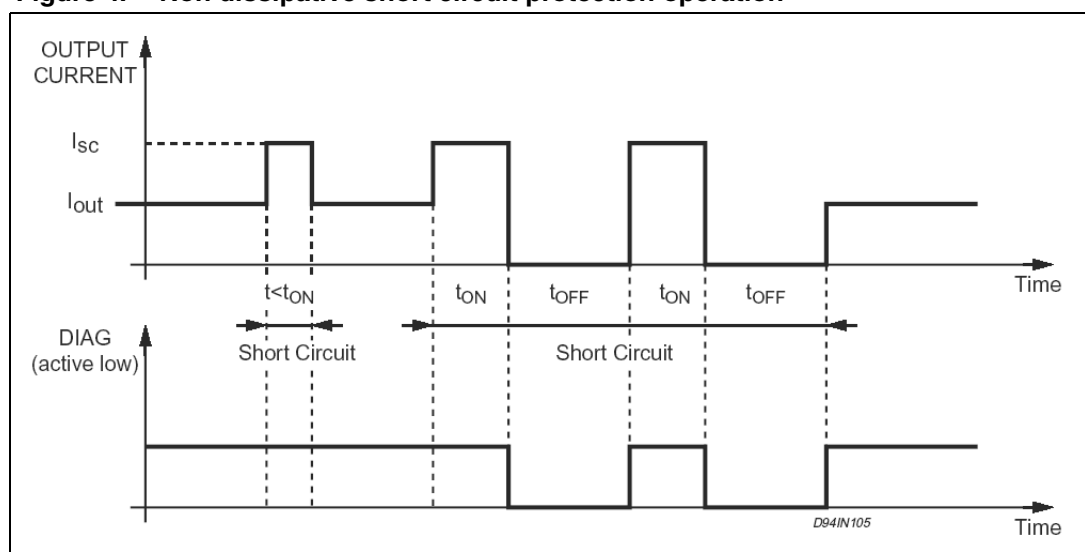
When also the T_{off} interval has expired, the out-put power MOS is switched ON. At this point in time two conditions may occur

- The overloads still present, and then the output power MOS is again driven in linear mode (limiting the output current to I_{sc}) for another T_{on} , starting a new cycle, or
- the over load the overload condition is removed, and the output power MOS is no longer driven in linear mode. All these occurrences are presented on the DIAG2 pin (see fig 2).

We call this unique feature Non Dissipative Short Circuit Protection and it ensures a very safe operation even in permanent overload conditions. Note that choosing the most appropriate value for the T_{on} interval (i.e. the value of the C_{don} capacitor) a delay (the T_{on} itself) will prevent that a misleading Short Circuit information is presented on the DIAG2 output, when driving capacitive loads (that acts like short circuit in the very beginning)

or Incandescent Lamp (a cold filament has a very low resistive value). The Non Dissipative Short Circuit Protection can be disabled (keeping $T_{on} = 0$ but with the output current still limited to I_{sc} , and Diagnostic disabled) simply shorting to ground the ON DELAY pin.

Figure 4. Non dissipative short circuit protection operation



2.9 Diagnostic logic

The operating conditions of the device are permanently monitored and the following occurrences are signalled via the DIAG1/DIAG2 open-drain output pins see diagnostic Truth Table.

- Short Circuit versus ground.
- Short Circuit versus VS.
- Under Voltage (UV)
- Over Temperature (OVT)
- Open Load, if the output current is less than 3mA (typical value).

2.10 Demagnetization of inductive loads

An internal zener diode, limiting the voltage across the Power MOS to between 50 and 60V (Vcl), provides safe and fast demagnetization of inductive loads without external clamping devices. The maximum energy that can be absorbed from an inductive load is specified as 200mJ (at $T_J = 85^{\circ}\text{C}$)

2.11 Diagnostic truth table

Table 6. Diagnostic truth table

Diagnostic conditions	Input	Output	Diag1	Diag2
Normal Operation	L H	L H	H H	H H
Open Load Condition ($I_o < I_{old}$)	L H	L H	H L	H H
Short to V_S	L H	H H	L L	H H
Short Circuit to Ground ($I_o = I_{SC}$) ⁽¹⁾ (pin ON-DELAY grounded)	H L	X L	H H	H H
Output DMOS Open	L H	L L	H L	H H
Overttemperature	L H	L L	H H	L L
Supply Undervoltage ($V_S < V_{sth2}$)	L H	L L	L L	L L

1. A cold lamp filament, or a capacitive load may activate the current limiting circuit of the IPS, when the IPS is initially turned on.

3 Application circuits

Figure 5. Inductive load equivalent circuit

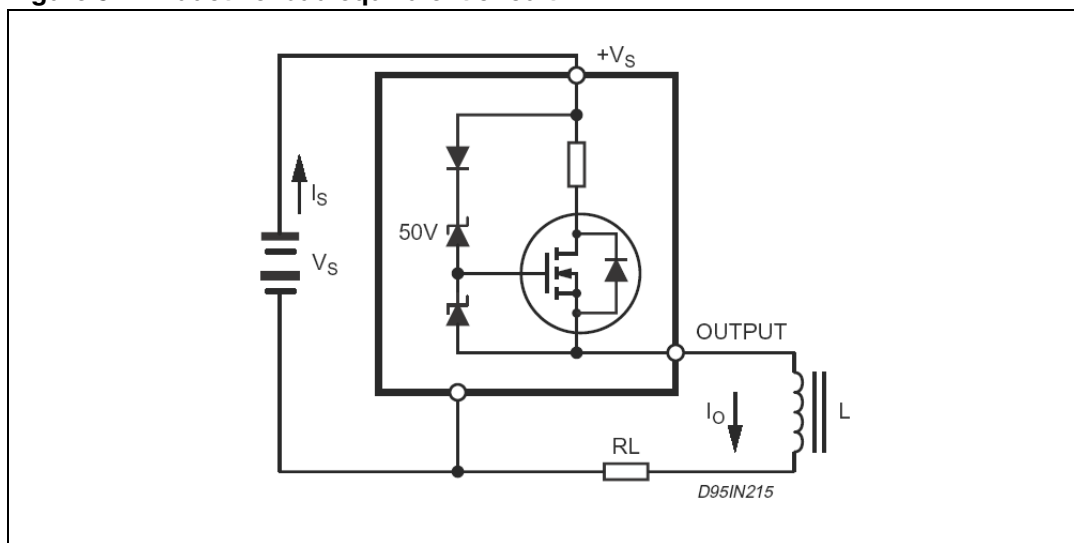
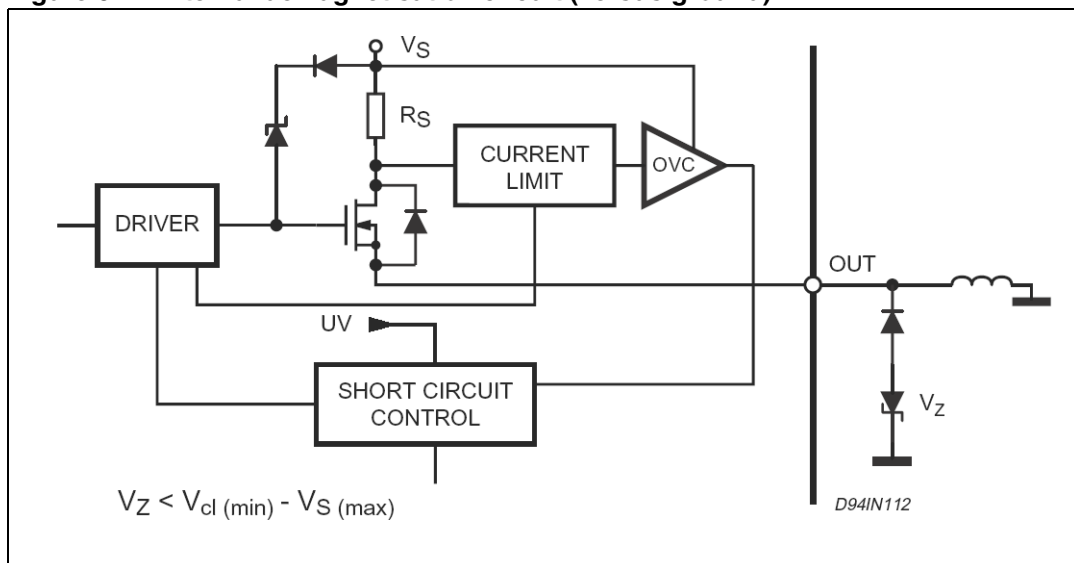


Figure 6. External demagnetisation circuit (versus ground)



The diagram illustrates a buck converter circuit with several protection features. The input voltage is V_S . The circuit includes a MOSFET driver, a MOSFET, a diode, and a sense resistor R_S . The MOSFET's gate is driven by a DRIVER. The sense resistor R_S is placed in the MOSFET's source path. The voltage across R_S is monitored by a CURRENT LIMIT block, which is connected to an OVC (Overcurrent Comparator) block. The OVC block's output is connected to the UV (Under-Voltage) block. The UV block's output is connected to the SHORT CIRCUIT CONTROL block. The SHORT CIRCUIT CONTROL block's output is connected to the MOSFET's gate. The MOSFET's drain is connected to the output filter inductor, which is connected to the output terminal OUT. The output terminal OUT is also connected to a load resistor and a Zener diode V_Z in parallel with the output. The Zener diode V_Z is connected to the input voltage V_S . The output voltage is V_{OUT} . The circuit is labeled D94IN111A.

$V_S (\text{max}) < V_Z < V_{cl} (\text{min})$

D94IN111A

The diagram illustrates the internal architecture of the Transil ST15KExx. Key components and connections include:

- Inputs:** IN+ (with a 1.4V reference), ON-DELAY, and THERMAL PROTECTION.
- Internal Blocks:** UNDER VOLTAGE, CHARGE PUMP, DRIVER, CURRENT LIMITATION, OPEN LOAD DETECTION, NON DISSIPATIVE SHORT CIRCUIT, OUTSTATUS, and DIAGNOSTIC.
- Outputs:** OUT, DIAG1, and DIAG2.
- External Components:** A 2.2μF electrolytic capacitor connected to V_s, and a 10nF ceramic capacitor connected to OUT.
- Current Source:** A 3mA current source connected to the bottom rail.

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. SO-8 mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					

Figure 9. Package dimensions

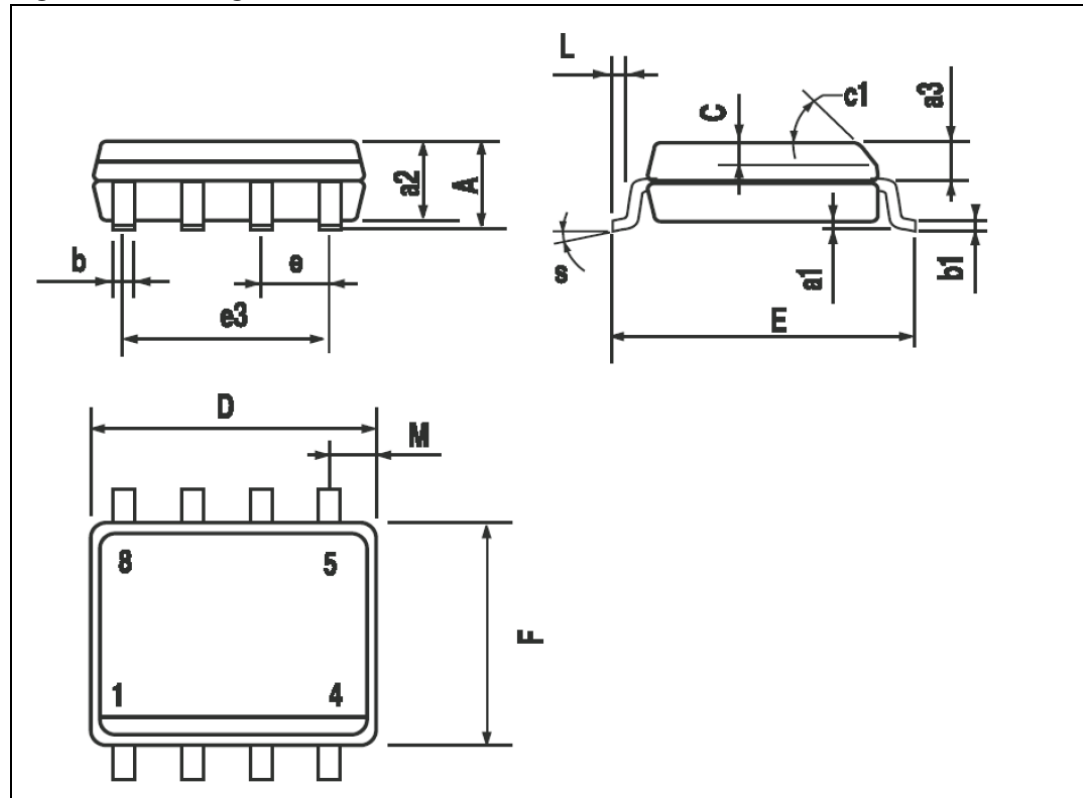
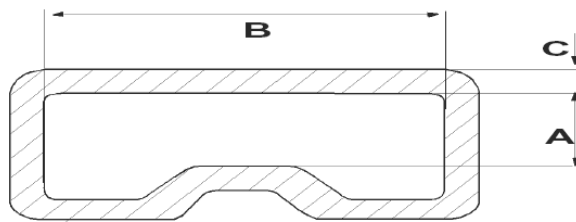
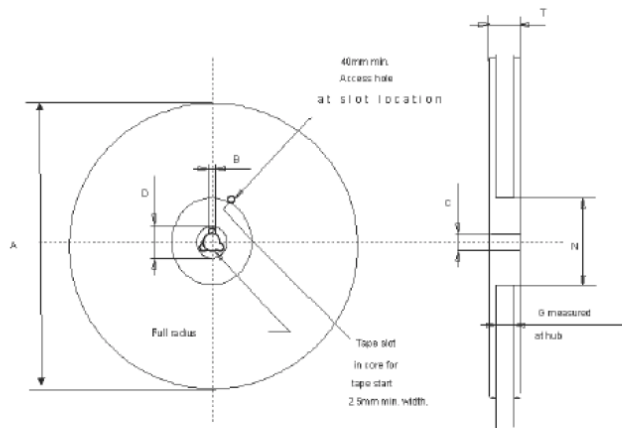


Figure 10. SO-8 Tape and reel information



Base Q.ty	100
Bulk Q.ty	2000
Tube Length(± 0.5)	532
A	3.2
B	6
C(± 0.1)	0.6



Reel Dimension

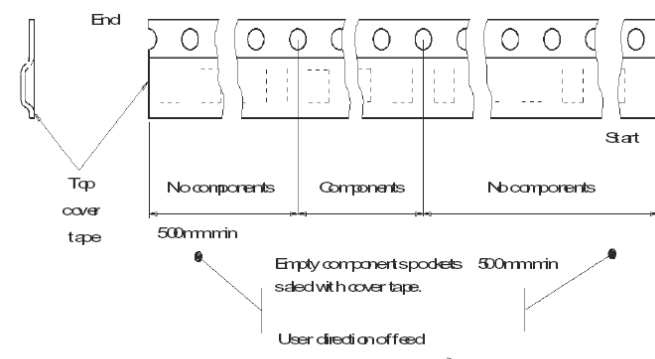
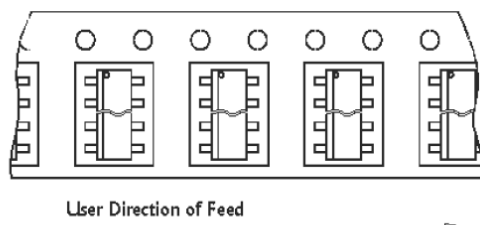
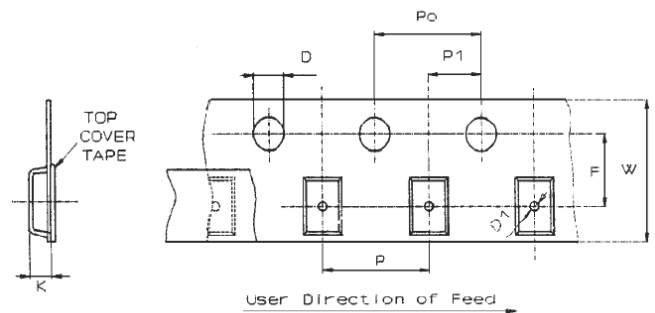
Base Q.ty	2500
Bulk Q.ty	2500
A(Max)	330
B(Min)	1.5
C(± 0.2)	13
F	20.2
G($+2/-0$)	12.4
N(Min)	60
T(Max)	18.4

Tape Dimension

According to Electronic Industries Association(EIA)
Standard 481 rev. A, Feb 1986

Tape Width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D($\pm 0.2/-0$)	1.5
Hole Diameter	D1(Min)	1.5
Hole Position	F(± 0.05)	5.5
Compartment Depth	K(Max)	4.5
Hole Spacing	P1(± 0.1)	2

All dimension are in mm.



5 Revision history

Table 8. Revision history

Date	Revision	Changes
18-Sep-2006	1	Initial release
19-Jun-2007	2	Truth table updated
05-Jul-2007	3	Typo in Table 5 on page 6
16-Jul-2007	4	Pin out updated
15-Oct-2007	5	Updated Table 4 on page 5

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