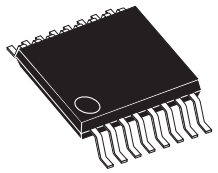
L6731B

Adjustable step-down controller with synchronous rectification Dedicated to DDR Memory

Features

- Input voltage range from 1.8V to 14V
- Supply voltage range from 4.5V to 14V
- Adjustable output voltage down to 0.6V with ±0.8% accuracy over line voltage and temperature (0°C~125°C)
- Fixed frequency voltage mode control
- T_{ON} lower than 100ns
- 0% to 100% duty cycle
- V_{DDR} input sense
- Regulates V_{TT} and V_{TTREF} within 1% of V_{DDQ}
- Soft-start and inhibit
- High current embedded drivers
- Predictive anti-cross conduction control
- Programmable high-side and low-side $R_{DS(on)}$ sense over-current-protection
- Selectable switching frequency 250KHz/ 500KHz
- Power good output
- Sink/source capability for ddr memory and termination supply
- Over voltage protection
- Thermal shut-down
- Package: HTSSOP16



HTSSOP16 (Exposed Pad)

Applications

- High performance / high density DC-DC modules
- Low voltage distributed DC-DC
- niPOL converters
- DDR memory supply
- DDR termination supply
- Graphic cards

Order Codes

Part number	Package	Packing
L6731B	HTSSOP16	Tube
L6731BTR	HTSSOP16	Tape & Reel

Contents

1 Summary description

The controller is an integrated circuit realized in BCD5 (BiCMOS-DMOS, version 5) fabrication that provides complete control logic and protection for high performance step-down DC-DC and niPOL converters.

It is designed to drive N-Channel MOSFETs in a synchronous rectified buck topology. The output voltage of the converter can be precisely regulated down to 600mV with a maximum tolerance of ±0.8%. If an external reference is used, it will be trasferred divided by 2 to the N.I. input of the error-amplifier, in accordance to the DDR memory specifications.

An internal resistor divider and a voltage buffer allow to achieve an accuracy of 1% on both Vtt and Vttref. It's possibile to provide an external reference from 0V to 2.5V in order to meet the specification for DDRI and DDRII. The input voltage can range from 1.8V to 14V, while the supply voltage can range from 4.5V to 14V. High peak current gate drivers provide for fast switching to the external power section, and the output current can be in excess of 20A.

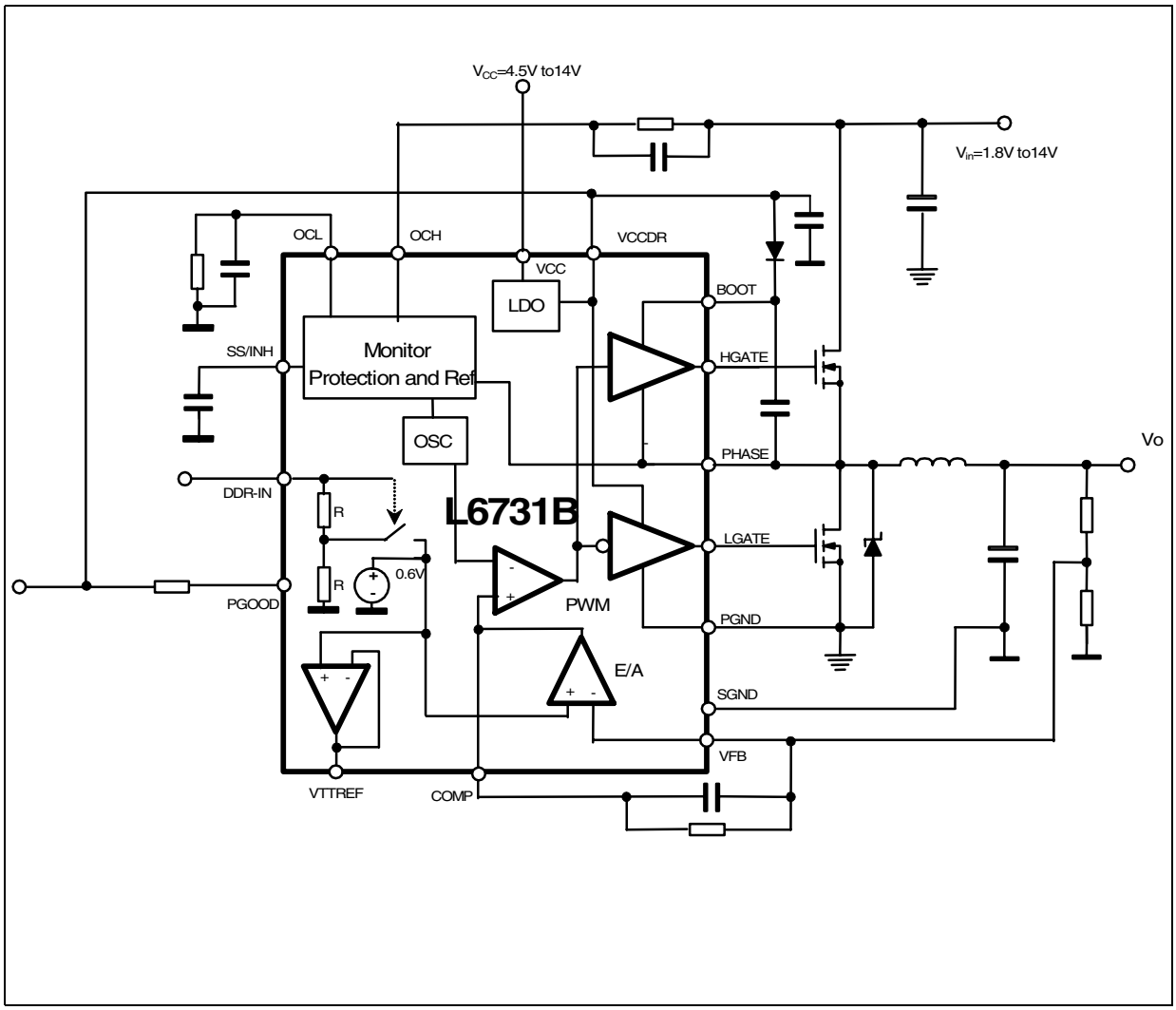
The PWM duty cycle can range from 0% to 100% with a minimum on-time ($T_{ON, MIN}$) lower than 100ns making possible conversions with very low duty cycle at high switching frequency. The device provides voltage-mode control that includes a selectable frequency oscillator (250KHz or 500KHz).

The error amplifier features a 10MHz gain-bandwidth-product and 5V/µs slew-rate that permits to realize high converter bandwidth for fast transient response. The device monitors the current by using the $R_{DS(on)}$ of both the high-side and low-side MOSFET(s), eliminating the need for a current sensing resistor and guaranteeing an effective over-current-protection in all the application conditions.

When necessary, two different current limit protections can be externally set through two external resistors. During the soft-start phase a constant current protection is provided while after the soft-start the device enters in hiccup mode in case of over-current. The converter can always sink current. Other features are Power-Good, not latched over-voltage-protection, feed-back disconnection and thermal shutdown. The HTSSOP16 package allows the realization of really compact DC/DC converters.

1.1 Functional description

Figure 1. Block Diagram



2 Electrical data

2.1 Maximum rating

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND and PGND, OCH, PGOOD	-0.3 to 18	V
V_{BOOT} - V_{PHASE}	Boot Voltage	0 to 6	V
V_{HGATE} - V_{PHASE}		0 to V_{BOOT} - V_{PHASE}	V
V_{BOOT}	BOOT	-0.3 to 24	V
V_{PHASE}	PHASE	-1 to 18	V
	PHASE Spike, transient < 50ns (F_{SW} = 500KHz)	-3	
		+24	
	SS, FB, VTTREF, DDR-IN, SYNC, OCL, LGATE, COMP, V_{CCDR}	-0.3 to 6	V
OCH Pin	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002 "Human Body Model" Acceptance Criteria: "Normal Performance"	±1500	V
PGOOD Pin		±1000	
OTHER PINS		±2000	

2.2 Thermal data

Table 2. Thermal data

Symbol	Description	Value	Unit
R_{thJA} (1)	Thermal Resistance Junction to ambient	50	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Ambient operating temperature range	-40 to +85	°C

1. Package mounted on demoboard

3 Pin connections and functions

Figure 2. Pins connection (Top view)

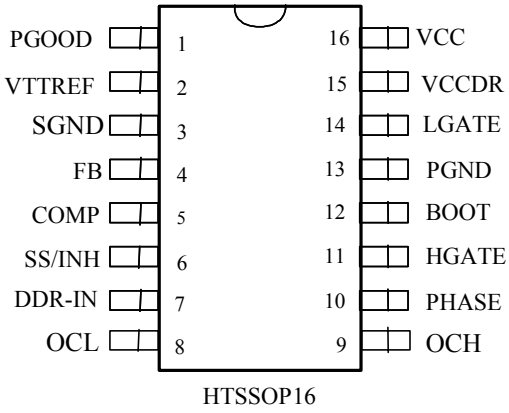


Table 3. Pin functions

Pin n.	Name	Function
1	PGOOD	This pin is an open collector output and it is pulled low if the output voltage is not within the specified thresholds (90%-110%). If not used it may be left floating. Pull-up this pin to V_{CCDR} with a 10K resistor to obtain a logical signal.
2	V_{TTREF}	This pin is connected to the output of an internal buffer that provides ½ of DDR-IN. This pin can be connected to the V_{TTREF} input of the DDR memory itself. Filter to GND with 10nF capacitor.
3	SGND	All the internal references are referred to this pin.
4	FB	This pin is connected to the error amplifier inverting input. Connect it to V_{OUT} through the compensation network. This pin is also used to sense the output voltage in order to manage the over voltage conditions and the PGood signal.
5	COMP	This pin is connected to the error amplifier output and is used to compensate the voltage control feedback loop.
6	SS/INH	The soft-start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces a current of 10µA through the capacitor. When the voltage at this pin is lower than 0.5V the device is disabled.
7	DDR-IN	By setting the voltage at this pin is possible to select the internal/external reference and the switching frequency: V_{EAREF} 0-80% of V_{CCDR} -> External Reference/F_{SW}=250KHz V_{EAREF} = 80%-95% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW}=500KHz V_{EAREF} = 95%-100% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW}=250KHz An internal clamp limits the maximum V_{EAREF} at 2.5V (typ.). The device captures the analog value present at this pin at the start-up when V_{CC} meets the UVLO threshold.

Table 3. Pin functions

8	OCL	A resistor connected from this pin to ground sets the valley- current-limit. The valley current is sensed through the low-side MOSFET(s). The internal current generator sources a current of 100µA (I_{OCL}) from this pin to ground through the external resistor (R_{OCL}). The over-current threshold is given by the following equation: $$I_{VALLEY} = \frac{I_{OCL} \bullet I_{OCL}}{2 \bullet R_{DSONLS}}$$ Connecting a capacitor from this pin to GND helps in reducing the noise injected from V_{CC} to the device, but can be a low impedance path for the high-frequency noise related to the GND. Connect a capacitor only to a "clean" GND.
9	OCH	A resistor connected from this pin and the high-side MOSFET(s) drain sets the peak-current-limit. The peak current is sensed through the high-side MOSFET(s). The internal 100µA current generator (I_{OCH}) sinks a current from the drain through the external resistor (R_{OCH}). The over-current threshold is given by the following equation: $$I_{PEAK} = \frac{I_{OCH} \bullet R_{OCH}}{R_{DSONHS}}$$
10	PHASE	This pin is connected to the source of the high-side MOSFET(s) and provides the return path for the high-side driver. This pin monitors the drop across both the upper and lower MOSFET(s) for the current limit together with OCH and OCL.
11	HGATE	This pin is connected to the high-side MOSFET(s) gate.
12	BOOT	Through this pin is supplied the high-side driver. Connect a capacitor from this pin to the PHASE pin and a diode from V_{CCDR} to this pin (cathode versus BOOT).
13	PGND	This pin has to be connected closely to the low-side MOSFET(s) source in order to reduce the noise injection into the device.
14	LGATE	This pin is connected to the low-side MOSFET(s) gate.
15	V_{CCDR}	5V internally regulated voltage. It is used to supply the internal drivers. Filter it to ground with at least 1µF ceramic cap.
16	V_{CC}	Supply voltage pin. The operative supply voltage range is from 4.5V to 14V.

4 Electrical characteristics

V_{CC} = 12V, T_A = 25°C unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} SUPPLY CURRENT						
I_{CC}	V_{CC} Stand By current	OSC = open; SS to GND		7	9	mA
	V_{CC} quiescent current	OSC= open; HG = open, LG = open, PH=open		8.5	10	
Power-ON						
V_{CC}	Turn-ON V_{CC} threshold	V_{OCH} = 1.7V	4.0	4.2	4.4	V
	Turn-OFF V_{CC} threshold	V_{OCH} = 1.7V	3.6	3.8	4.0	V
$V_{IN\ OK}$	Turn-ON V_{OCH} threshold		1.1	1.25	1.47	V
$V_{IN\ OK}$	Turn-OFF V_{OCH} threshold		0.9	1.05	1.27	V
V_{CCDR} Regulation						
	V_{CCDR} voltage	V_{CC} =5.5V to 14V I_{DR} = 1mA to 100mA	4.5	5	5.5	V
Soft Start and Inhibit						
I_{SS}	Soft Start Current	SS = 2V	7	10	13	µA
		SS = 0 to 0.5V	20	30	45	
Oscillator						
f_{OSC}	Accuracy		237	250	263	KHz
			450	500	550	KHz
ΔV_{OSC}	Ramp Amplitude			2.1		V
Output Voltage						
V_{FB}	Output Voltage	V_{DIS} = 0 to V_{th}	0.597	0.6	0.603	V

Table 4. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Error Amplifier						
R_{EAREF}	EAREF Input Resistance	Vs. GND	70	100	150	kΩ
I_{FB}	I.I. bias current	V_{FB} = 0V		0.290	0.5	µA
Ext Ref Clamp			2.3			V
V_{OFFSET}	Error amplifier offset	Vref = 0.6V	-5		+5	mV
G_V	Open Loop Voltage Gain	Guaranteed by design		100		dB
GBWP	Gain-Bandwidth Product	Guaranteed by design		10		MHz
SR	Slew-Rate	COMP = 10pF Guaranteed by design		5		V/µs
Gate Drivers						
R_{HGATE_ON}	High Side Source Resistance	V_{BOOT} - V_{PHASE} = 5V		1.7		Ω
R_{HGATE_OFF}	High Side Sink Resistance	V_{BOOT} - V_{PHASE} = 5V		1.12		Ω
R_{LGATE_ON}	Low Side Source Resistance	V_{CCDR} = 5V		1.15		Ω
R_{LGATE_OFF}	Low Side Sink Resistance	V_{CCDR} = 5V		0.6		Ω
Protections						
I_{OCH}	OCH Current Source	V_{OCH} = 1.7V	90	100	110	µA
I_{OCL}	OCL Current Source		90	100	110	µA
OVP	Over Voltage Trip (VFB / VEAREF)	V_{FB} Rising V_{EAREF} = 0.6V		120		%
		V_{FB} Falling V_{EAREF} = 0.6V		117		%
Power Good						
	Upper Threshold (V_{FB} / V_{EAREF})	VFB Rising	108	110	112	%
	Lower Threshold (V_{FB} / V_{EAREF})	V_{FB} Falling	88	90	92	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -5mA		0.5		ϖ

Table 5. Thermal Characteristics (V_{CC} = 12V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Output Voltage						
V_{FB}	Output Voltage	T_J = 0°C~ 125°C	0.596	0.6	0.605	V
		T_J = -40°C~ 125°C	0.593	0.6	0.605	

5 Device description

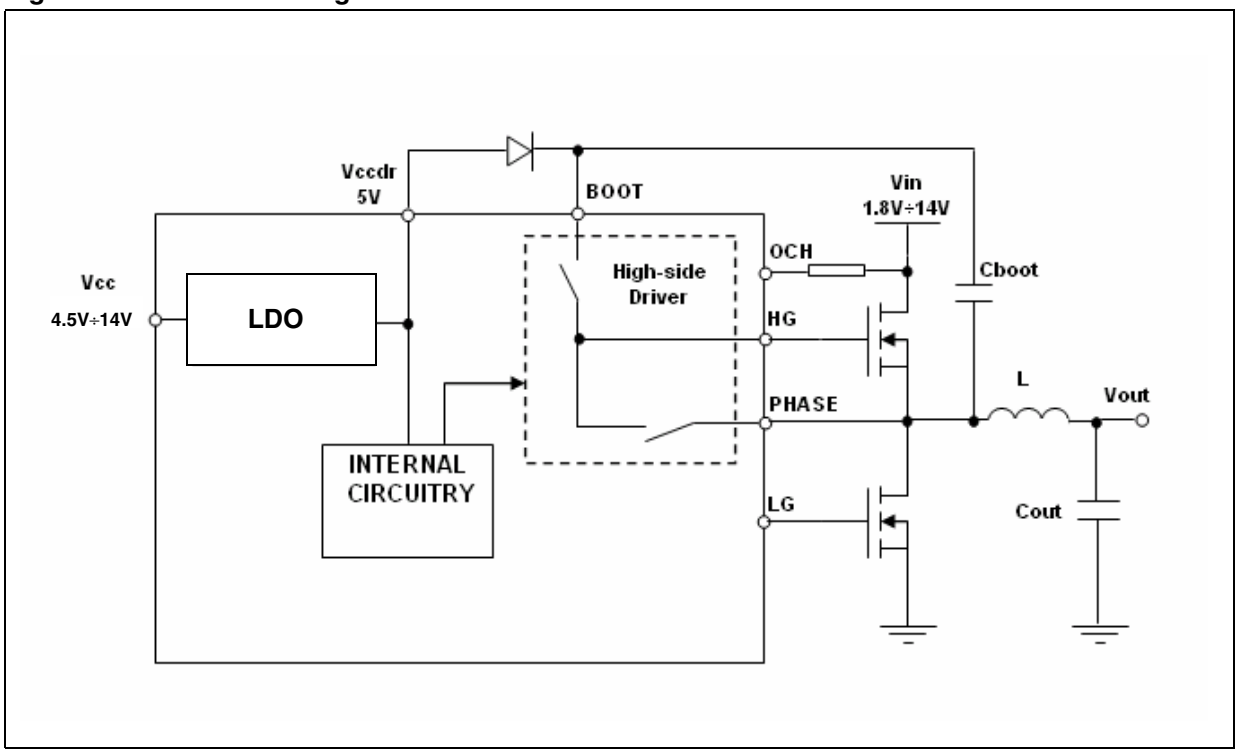
5.1 Oscillator

The switching frequency can be fixed to two values: 250KHz or 500KHz by setting the proper voltage at the EAREF pin (see *Table 3.* Pins function and section 4.3 Internal and external reference).

5.2 Internal LDO

An internal LDO supplies the internal circuitry of the device. The input of this stage is the V_{CC} pin and the output (5V) is the V_{CCDR} pin (*Figure 3.*).

Figure 3. LDO block diagram.

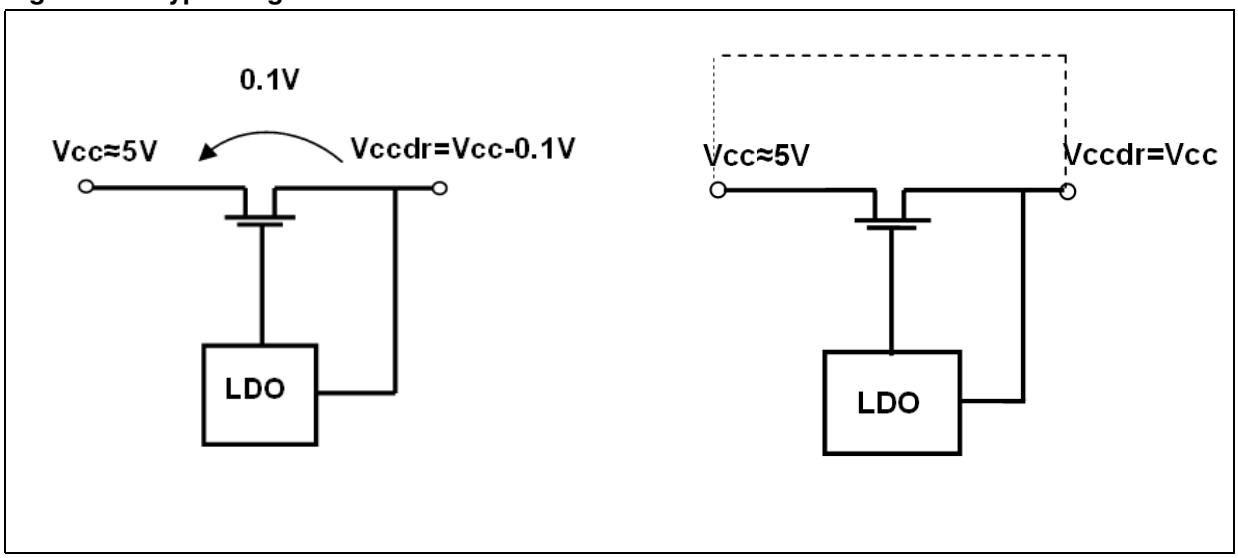


The LDO can be by-passed, providing directly a 5V voltage to V_{CCDR}. In this case V_{CC} and V_{CCDR} pins must be shorted together as shown in *Figure 4.* V_{CCDR} pin must be filtered with at least 1µF capacitor to sustain the internal LDO during the recharge of the bootstrap capacitor. V_{CCDR} also represents a voltage reference for PGOOD pin (see *Table 3.* Pins Function).

5.3 Bypassing the LDO to avoid the voltage drop with low Vcc

If $V_{CC} \approx$ 5V the internal LDO works in dropout with an output resistance of about 1Ω The maximum LDO output current is about 100mA and so the output voltage drop is 100mV, to avoid this the LDO can be bypassed.

Figure 4. Bypassing the LDO



5.4 Internal and external references

It is possible to set the internal/external reference and the switching frequency by setting the proper voltage at the DDR-IN pin. The maximum value of the external reference is 2.5V (typ.):

- V_{EAREF} from 0% to 80% of V_{CCDR} -> External reference/F_{SW} = 250KHz
- V_{EAREF} from 80% to 95% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW}=500KHz
- V_{EAREF} from 95% to 100% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW}=250KHz

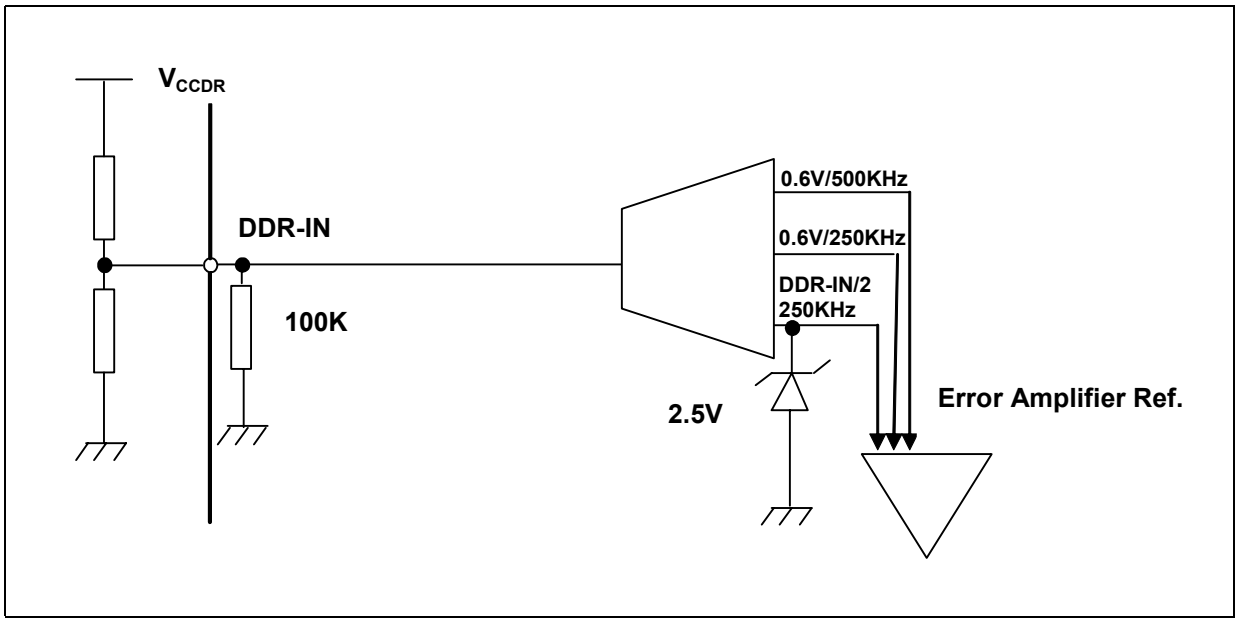
Providing an external reference from 0V to 450mV the output voltage will be regulated but some restrictions must be considered:

- The minimum OVP threshold is set at 300mV;
- The under-voltage-protection doesn't work;
- The PGOOD signal remains low;

To set the resistor divider it must be considered that a 100K pull-down resistor is integrated into the device (see *Figure 5.*). Finally it must be taken into account that the voltage at the DDR-IN pin is captured by the device at the start-up when V_{CC} is about 4V.

5.5 Error amplifier

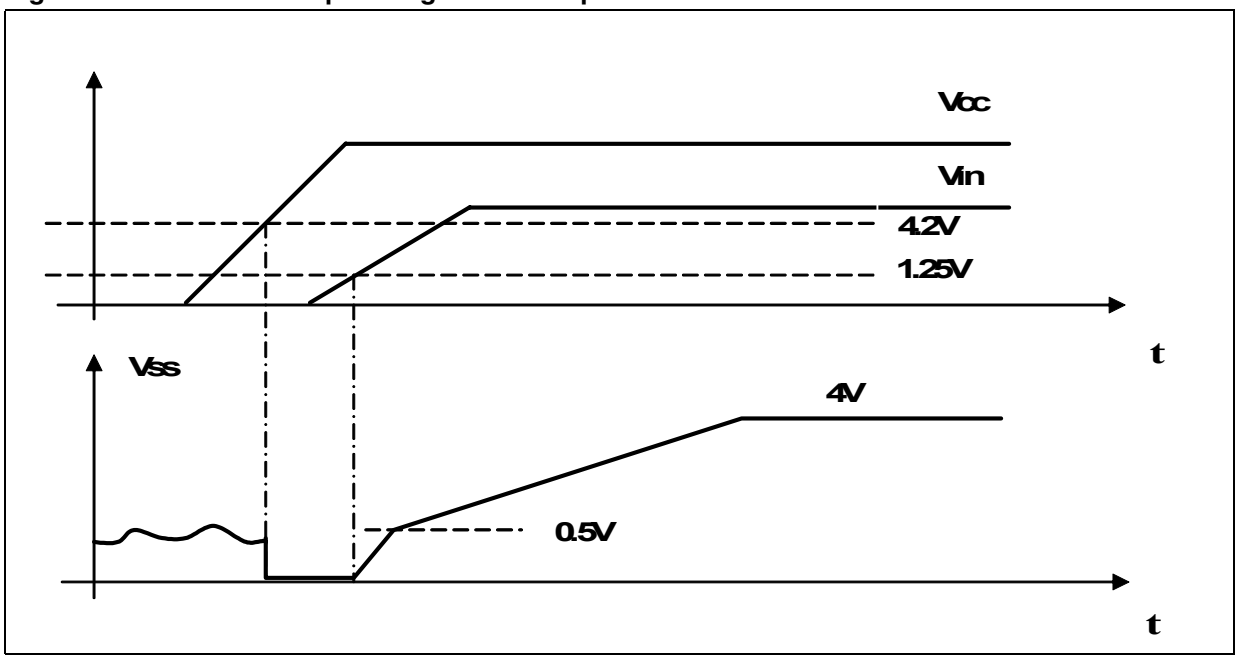
Figure 5. Error Amplifier Reference



5.6 Soft start

When both V_{CC} and V_{IN} are above their turn-ON thresholds (V_{IN} is monitored by the OCH pin) the start-up phase takes place. Otherwise the SS pin is internally shorted to GND. At start-up, a ramp is generated charging the external capacitor C_{SS} with an internal current generator. The initial value for this current is 35µA and charges the capacitor up to 0.5V. After that it becomes 10µA until the final charge value of approximately 4V (see *Figure 6.*).

Figure 6. Device start-up: Voltage at the SS pin.



The output of the error amplifier is clamped with this voltage (Vss) until it reaches the programmed value. No switching activity is observable if V_{SS} is lower than 0.5V and both MOSFETs are off. When Vss is between 0.5V and 1.1V the low-side MOSFET is turned on because the comp signal is lower than the valley of the triangular wave and so the duty-cycle is 0%. As V_{SS} reaches 1.1V (i.e. the oscillator triangular wave inferior limit) even the high-side MOSFET begins to switch and the output voltage starts to increase. The L6731B can always sink or source current. If an over current is detected during the soft-start phase, the device provides a constant-current-protection. In this way, in case of short soft-start time and/or small inductor value and/or high output capacitors value and so, in case of high ripple current during the soft-start, the converter can start in any case, limiting the current (see *5.8: Monitoring and protections*) but not entering in HICCUP mode. During normal operation, if any under-voltage is detected on one of the two supplies, the SS pin is internally shorted to GND and so the SS capacitor is rapidly discharged.

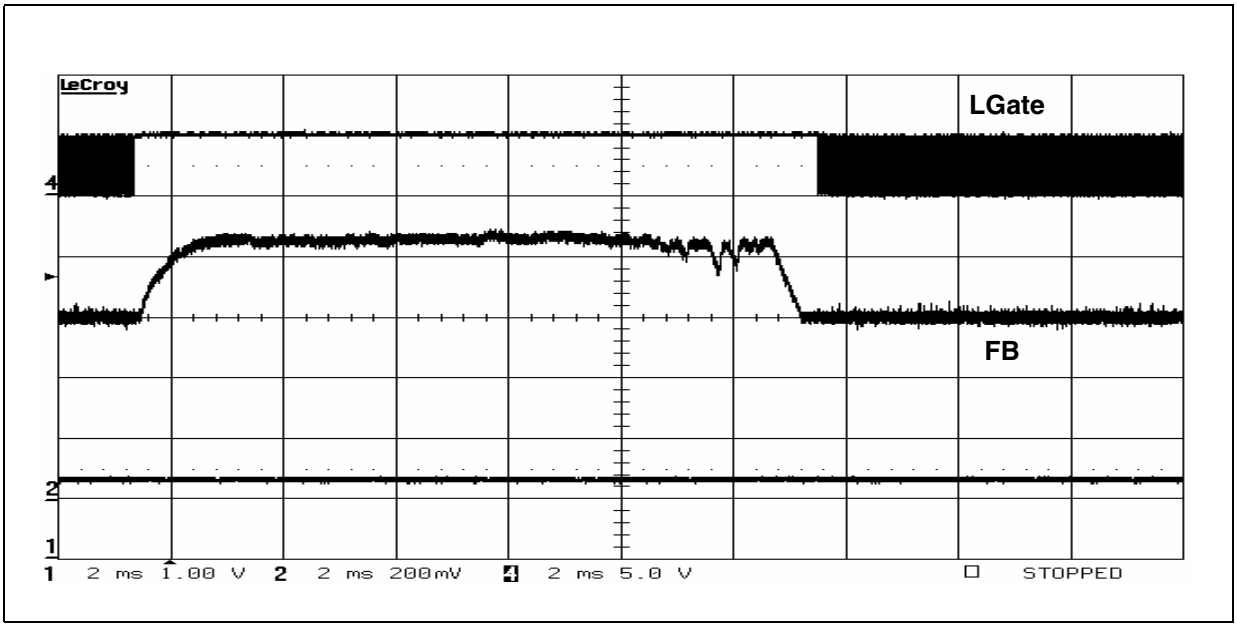
5.7 Driver section

The high-side and low-side drivers allow using different types of power MOSFETs (also multiple MOSFETs to reduce the $R_{DS(on)}$), maintaining fast switching transitions. The low-side driver is supplied by V_{CCDR} while the high-side driver is supplied by the BOOT pin. A predictive dead time control avoids MOSFETs cross-conduction maintaining very short dead time duration in the range of 20ns. The control monitors the phase node in order to sense the low-side body diode recirculation. If the phase node voltage is less than a certain threshold (-350mV typ.) during the dead time, it will be reduced in the next PWM cycle. The predictive dead time control doesn't work when the high-side body diode is conducting because the phase node doesn't go negative. This situation happens when the converter is sinking current for example and, in this case, an adaptive dead time control operates.

5.8 Monitoring and protections

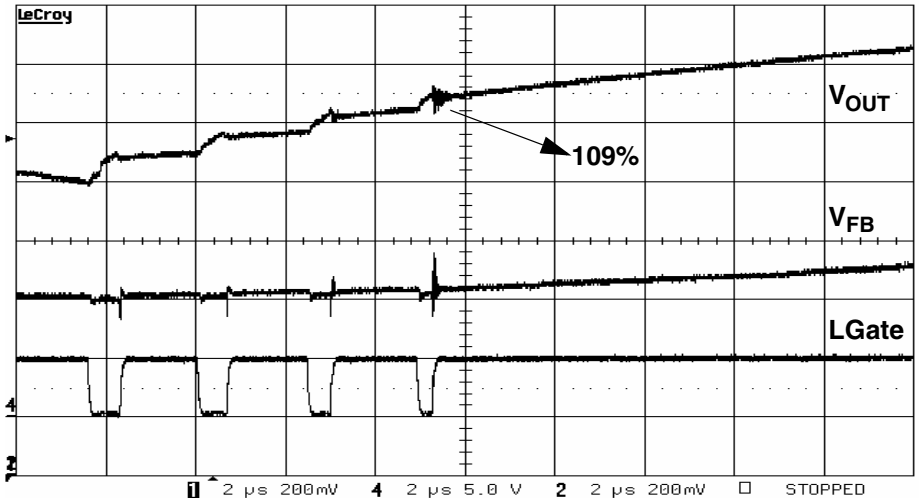
The output voltage is monitored by means of pin FB. If it is not within ±10% (typ.) of the programmed value, the Power-Good (PGOOD) output is forced low. The device provides over-voltage-protection: when the voltage sensed on FB pin reaches a value 20% (typ.) greater than the reference, the low-side driver is turned on as long as the over voltage is detected (see *Figure 7.*).

Figure 7. OVP



It must be taken into account that there is an electrical network between the output terminal and the FB pin and therefore the voltage at the pin is not a perfect replica of the output voltage. However due to the fact that the converter can sink current, in the most of cases the low-side will turn-on before the output voltage exceeds the over-voltage threshold, because the error amplifier will throw off balance in advance. Even if the device doesn't report an over-voltage, the behavior is the same, because the low-side is turned-on immediately. The following figure shows the device behavior during an over-voltage event. The output voltage rises with a slope of 100mV/µs, emulating in this way the breaking of the high-side MOSFET as an over-voltage cause.

Figure 8. OVP: the low-side MOSFET is turned-on in advance.



The device realizes the over-current-protection (OCP) sensing the current both on the high-side MOSFET(s) and the low-side MOSFET(s) and so 2 current limit thresholds can be set (see OCH pin and OCL pin in *Table 3.* Pins function):

- Peak Current Limit
- Valley Current Limit

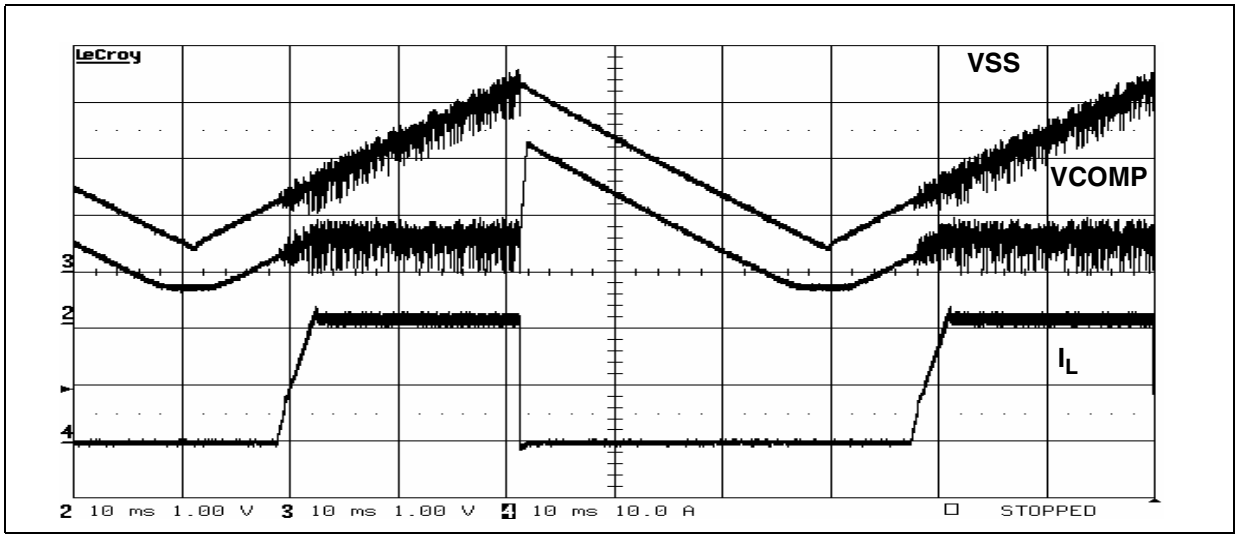
The Peak Current Protection is active when the high-side MOSFET(s) is turned on, after a masking time of about 100ns. The valley-current-protection is enabled when the low-side MOSFET(s) is turned on after a masking time of about 400ns. If, when the soft-start phase is completed, an over current event occurs during the on time (peak-current-protection) or during the off time (valley-current-protection) the device enters in HICCUP mode: the high-side and low-side MOSFET(s) are turned off, the soft-start capacitor is discharged with a constant current of 10µA and when the voltage at the SS pin reaches 0.5V the soft-start phase restarts. During the soft-start phase the OCP provides a constant-current-protection. If during the T_{ON} the OCH comparator triggers an over current the high-side MOSFET(s) is immediately turned off (after the masking time and the internal delay) and returned on at the next pwm cycle. The limit of this protection is that the T_{ON} can't be less than masking time plus propagation delay because during the masking time the peak-current-protection is disabled. In case of very hard short circuit, even with this short T_{ON}, the current could escalate. The valley-current-protection is very helpful in this case to limit the current. If during the off-time the OCL comparator triggers an over current, the high-side MOSFET(s) is not turned on until the current is over the valley-current-limit. This implies that, if it is necessary, some pulses of the high-side MOSFET(s) will be skipped, guaranteeing a maximum current due to the following formula:

$$I_{MAX} = I_{VALLEY} + \frac{Vin - Vout}{L} \cdot T_{ON,MIN}$$

In constant current protection a current control loop limits the value of the error amplifier output (comp), in order to avoid its saturation and thus recover faster when the output returns in regulation. *Figure 9.* shows the behaviour of the device during an over current condition that persists also in the soft-start phase.

5.9 HICCUP mode during an OCP

Figure 9. Constant current and Hiccup Mode during an OCP.



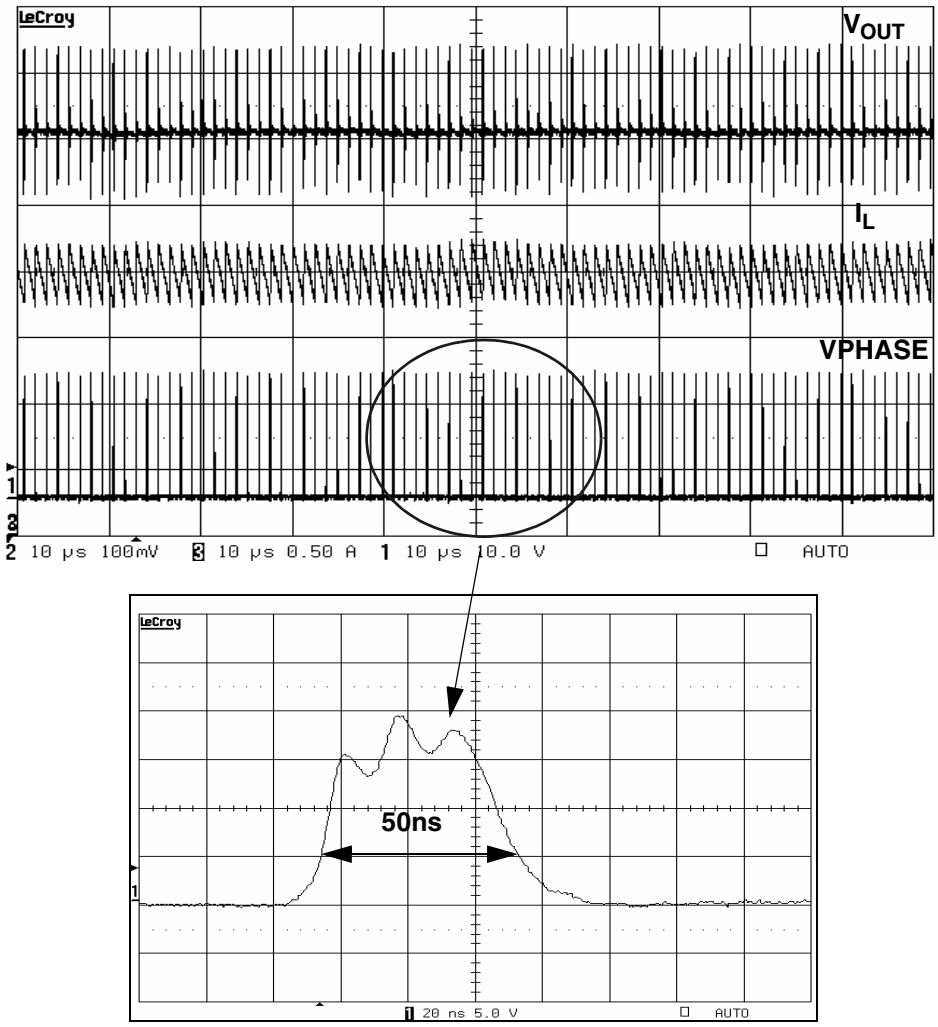
5.10 Thermal shutdown

When the junction temperature reaches 150°C ±10°C the device enters in thermal shutdown. Both MOSFETs are turned off and the soft-start capacitor is rapidly discharged with an internal switch. The device doesn't restart until the junction temperature goes down to 120°C and, in any case, until the voltage at the soft-start pin reaches 500mV.

5.11 Minimum on-time ($T_{ON, MIN}$)

The device can manage minimum on-times lower than 100ns. This feature comes down from the control topology and from the particular over-current-protection system of the L6731B. In fact, in a voltage mode controller the current has not to be sensed to perform the regulation and, in the case of L6731B, neither for the over-current protection, given that during the off-time the valley-current-protection can operate in every case. The first advantage related to this feature is the possibility to realize extremely low conversion ratios. *Figure 10.* shows a conversion from 14V to 0.3V at 500KHz with a T_{ON} of about 50ns.

Figure 10. 14V -> 0.3V@500KHz, 5A



The on-time is limited by the turn-on and turn-off times of the MOSFETs.

6 Application details

6.1 Inductor design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current. The inductance value can be calculated with the following relationship:

$$L \cong \frac{Vin - Vout}{Fsw \cdot \Delta I_L} \cdot \frac{Vout}{Vin} \quad (2)$$

Where F_{SW} is the switching frequency, Vin is the input voltage and Vout is the output voltage. Increasing the value of the inductance reduces the ripple current but, at the same time, increases the converter response time to a load transient. If the compensation network is well designed, during a load transient the device is able to set the duty cycle to 100% or to 0%. When one of these conditions is reached, the response time is limited by the time required to change the inductor current. During this time the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitor size.

6.2 Output capacitors

The output capacitors are basic components for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient. During a load transient, the output capacitors supply the current to the load or absorb the current stored in the inductor until the converter reacts. In fact, even if the controller recognizes immediately the load transient and sets the duty cycle at 100% or 0%, the current slope is limited by the inductor value. The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta Vout_{ESR} = \Delta Iout \cdot ESR \quad (3)$$

Moreover, there is an additional drop due to the effective capacitor discharge or charge that is given by the following formulas:

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot (Vin, \min \cdot D \max - Vout)} \quad (4)$$

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot Vout} \quad (5)$$

Formula (4) is valid in case of positive load transient while the formula (5) is valid in case of negative load transient. D_{MAX} is the maximum duty cycle value that in the L6731D is 100%. For a given inductor value, minimum input voltage, output voltage and maximum load transient, a maximum ESR and a minimum Cout value can be set. The ESR and Cout values also affect the static output voltage ripple. In the worst case the output voltage ripple can be calculated with the following formula:

$$\Delta Vout = \Delta I_L \cdot (ESR + \frac{1}{8 \cdot Cout \cdot Fsw}) \quad (6)$$

Usually the voltage drop due to the ESR is the biggest one while the drop due to the capacitor discharge is almost negligible.

6.3 Input capacitors

The input capacitors have to sustain the RMS current flowing through them, that is:

$$Irms = Iout \cdot \sqrt{D \cdot (1 - D)}$$

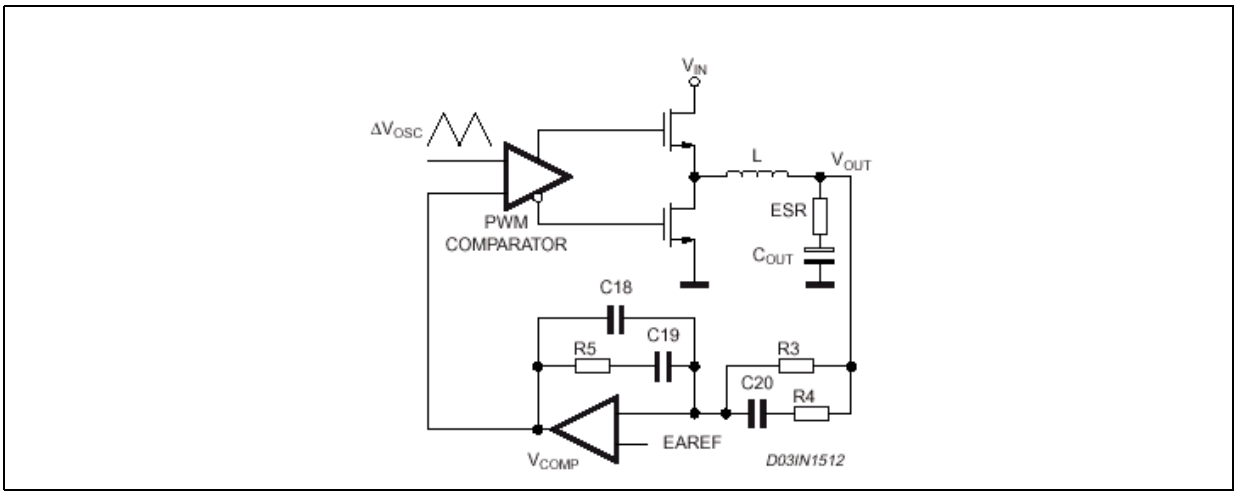
Where D is the duty cycle. The equation reaches its maximum value, I_{OUT} /2 with D = 0.5. The losses in worst case are:

$$P = ESR \cdot (0.5 \cdot Iout)^2$$

6.4 Compensation network

The loop is based on a voltage mode control (*Figure 18.*). The output voltage is regulated to the internal/external reference voltage and scaled by the external resistor divider. The error amplifier output V_{COMP} is then compared with the oscillator triangular wave to provide a pulse-width modulated (PWM) with an amplitude of V_{IN} at the PHASE node. This waveform is filtered by the output filter. The modulator transfer function is the small signal transfer function of V_{OUT}/ V_{COMP}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at FESR depending on the output capacitor's ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage: V_{OSC}.

Figure 11. Compensation Network



The compensation network consists in the internal error amplifier, the impedance networks Z_{IN} (R3, R4 and C20) and Z_{FB} (R5, C18 and C19). The compensation network has to provide a closed loop transfer function with the highest 0dB crossing frequency to have fastest transient response (but always lower than fsw/10) and the highest gain in DC conditions to minimize the load regulation error. A stable control loop has a gain crossing the 0dB axis with -20dB/decade slope and a phase margin greater than 45°. To locate poles and zeroes of the compensation networks, the following suggestions may be used:

- Modulator singularity frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L \cdot Cout}} \quad (13) \qquad \omega_{ESR} = \frac{1}{ESR \cdot Cout} \quad (14)$$

- Compensation network singularity frequencies:

$$\omega_{P1} = \frac{1}{R_5 \cdot \left(\frac{C_{18} \cdot C_{19}}{C_{18} + C_{19}} \right)} \quad (15) \qquad \omega_{P2} = \frac{1}{R_4 \cdot C_{20}} \quad (16)$$

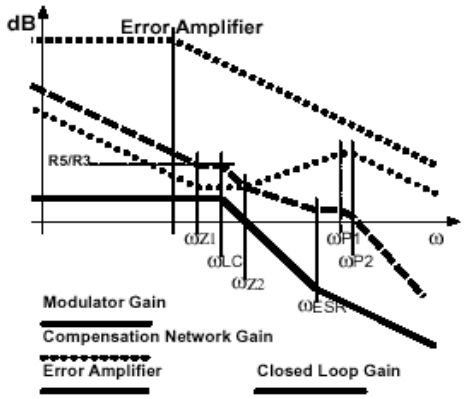
$$\omega_{Z1} = \frac{1}{R_5 \cdot C_{19}} \quad (17) \qquad \omega_{Z2} = \frac{1}{C_{20} \cdot (R_3 + R_4)} \quad (18)$$

- Compensation network design:
  - Put the gain R_5/R_3 in order to obtain the desired converter bandwidth

$$\varpi_C = \frac{R_5}{R_3} \cdot \frac{Vin}{\Delta Vosc} \cdot \varpi_{LC} \quad (19)$$

  - Place ω_{Z1} before the output filter resonance ω_{LC};
  - Place ω_{Z2} at the output filter resonance ω_{LC};
  - Place ω_{P1} at the output capacitor ESR zero ω_{ESR};
  - Place ω_{P2} at one half of the switching frequency;
  - Check the loop gain considering the error amplifier open loop gain.

Figure 12. Asymptotic Bode plot of Converter's open loop gain



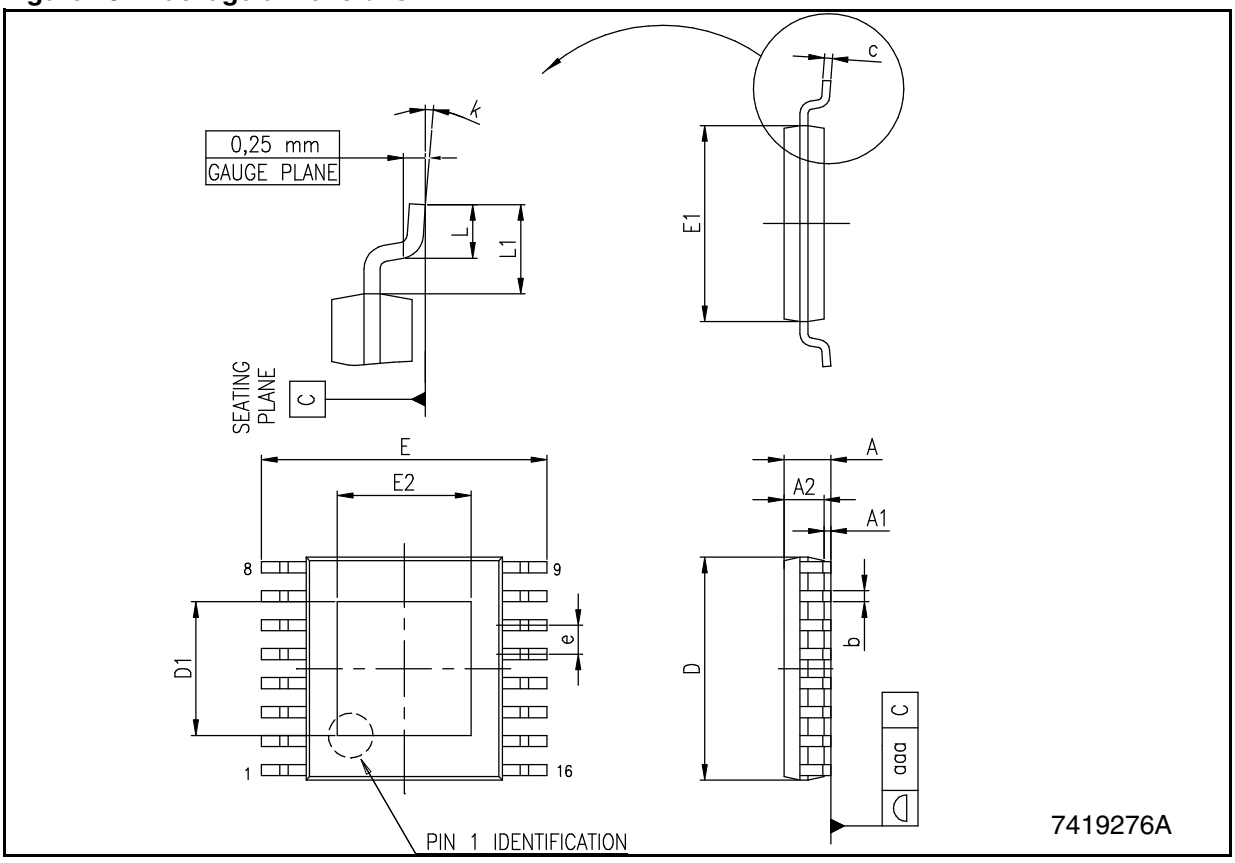
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 6. HTSSOP16 mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
D1	1.7			0.067		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 13. Package dimensions



8 Revision history

Table 7. Revision history

Date	Revision	Changes
22-Dec-2005	1	Initial release
31-May-2006	2	New template, thermal data updated
26-Jun-2006	3	Note page 5 deleted

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