FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28824-3E

ASSP for Screen Display Control

CMOS

ON-Screen Display Controller

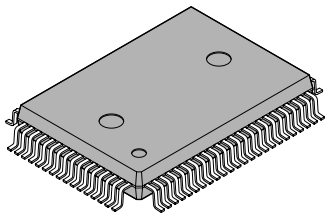
MB90092

■ DESCRIPTION

The MB90092 is the display controller for displaying text and graphics on the TV screen.
The MB90092 incorporates display memory (VRAM), a font memory interface, and a video signal generator, allowing text and graphics to be displayed in conjunction with a small number of external components.
The MB90092 can provide two screens, called the main screen and the sub-screen, either independently or overlayed one on top of the other.
The main screen consists of 24 characters by 12 lines and allows data to be set for each character. The sub-screen consists of 32 characters by 12 lines or up to 32 characters by 16 lines. Data can be set either for each line in the former configuration or collectively for the entire screen in the latter configuration.
For output of video signals, the MB90092 has the composite video signal, Y/C-separated video signal, and RGB digital output pins. The MB90092 also has video signal input pins, allowing superimpose display over either composite video signals and Y/C-separated video signals.

■ PACKAGE

80-pin Plastic QFP



(FPT-80P-M06)

■ FEATURES

- **Main Screen Display**
  - Screen display capacity:24 characters × 12 lines (up to 288 characters)
  - Character dot configuration:24 × 32 dots (per character)
  - Character types: 16384 different characters (when using a 16 M bit external clock)
  - Character sizes: Standard, double width, double height, double width × double height, quadruple width × double height (Setting possible for each line)
  - Display position control : Horizontal display position :Set in 1/3-character units
    Vertical display position :Set in raster units
    Line spacing control :Set in raster units (0 to 15 rasters)
  - Display priority control:Capable of controlling display priority over the sub-screen (for each line)
- **Sub-Screen Display**

  Screen display position: Settable horizontally and vertically in 2-dot units
  - Normal screen mode:Screen capacity:32 characters × 12 lines (up to 384 characters)
    256 horizontal dots × 384 vertical dots (graphics characters only) (The actual display screen depends on the television system and dot clock frequency.) Normal character/graphic character display selectable for each line (Header display character code is specified for each line.)
    Character string length:Selectable from among 1, 2, 4, 8, 16, 24, and 32 digits
  - Full-screen mode
    Screen capacity: 32 characters × 16 lines (up to 512 characters)
    256 horizontal dots × 512 vertical dots
    (The actual display screen depends on the television system and dot clock frequency.)
    Virtual screen capacity:Mode A:32 characters × 16 lines (× 32 screens)
    256 horizontal dots × 512 vertical dots
    Mode B:512 characters × 32 lines
    4096 horizontal dots × 1024 vertical dots

Screen Background Display

Screen background color: 8 colors (set for the entire screen)

Analog Inputs

- Composite video signal input
- Y/C-separated inputs

Analog Outputs

- Composite video signal output
- Y/C-separated outputs

Digital Outputs

- G (Green), R (Red), and B (Blue) output
- VOC (character) output, VOB (character + background) output
- Characters, character background, line background, and screen background each capable of being displayed in eight colors

Internal Synchronization Control (Video Signal Generator)

- Internal video signal generator supporting the NTSC and PAL systems
- Interlaced/noninterlaced display selectable

(Continued)

(Continued)

External Synchronization Control

- Separated sync signal input/composite sync signal input selectable

External Interface

- 8-bit serial inputs (3 signal input pins)
  Chip select: $\overline{CS}$
  Serial clock: SCLK
  Serial data: SIN

Package

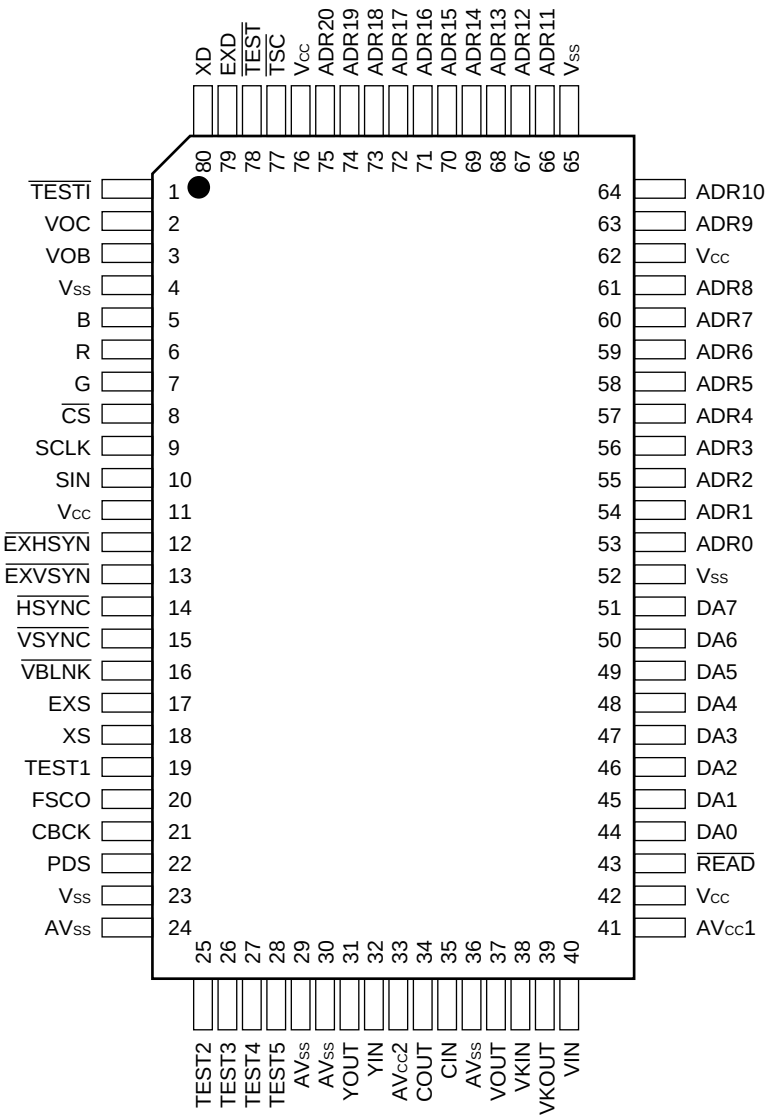
- QFP-80

Miscellaneous

- Internal power-on reset circuit

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-80P-M06)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Circuit type	Function
1	$\overline{\text{TESTI}}$	I	B	Test signal input pin. Input High level signal during normal operation. This pin also can be used as a reset signal input pin by Low-level input to the $\overline{\text{TEST}}$ pin. That is effective only after release of power-on reset. This pin is a hysteresis input with an internal pull-up resistor.
2	VOC	O	C	Character interval signal output pin. The output signal represents the character dot output interval.
3	VOB	O	C	Character/background internal signal output pin. During internal synchronization control operation, the output signal represents the character, character background, line background, or screen background output interval.
5 6 7	B R G	O	C	Color signal output pins. These pins output the character, character background, line background, and screen background color signals.
8	$\overline{\text{CS}}$	I	B	Chip select pin. For serial transfer, set this pin to the Low level. This pin is also used to release a power-on reset. The pin is a hysteresis input with an internal pull-up resistor.
9	SCLK	I	B	Shift clock input pin for serial transfer. This pin is a hysteresis input with an internal pull-up resistor.
10	SIN	I	B	Serial data input pin. The pin is a hysteresis input with an internal pull-up resistor.
12	$\overline{\text{EXHSYN}}$	I	B	External horizontal sync signal input pin. Input negative logic signal. This pin can also serve as a composite sync signal input pin depending on the internal register setting. The pin is a hysteresis input with an internal pull-up resistor.
13	$\overline{\text{EXVSYN}}$	I	B	External vertical sync signal input pin. Input negative logic signal. Input to this pin is disabled when composite sync signal input has been selected by setting the internal register. The pin is a hysteresis input with an internal pull-up resistor.
14	$\overline{\text{HSYNC}}$	O	C	Horizontal sync signal output pin. This pin can also output composite sync signals depending on the internal register setting. The pin outputs the signal (FSC) resulting from dividing the 4FSC clock frequency by setting the $\overline{\text{TEST}}$ pin to the Low level.
15	$\overline{\text{VSYNC}}$	O	C	Vertical sync signal output pin. This pin is fixed at the High level when composite sync signal output has been selected by setting the internal register. The pin outputs the dot clock oscillator signal when the $\overline{\text{TEST}}$ pin goes into Low.
16	$\overline{\text{VBLNK}}$	O	C	Vertical blanking interval signal output pin. This pin outputs the Low-level signal in the vertical blanking interval.

(Continued)

Pin no.	Pin name	I/O	Circuit type	Function
17 18	EXS XS	I O	H	External circuit pins for color burst clock generator. Connect an external crystal oscillator (14.31818 MHz for NTSC or 17.734475 MHz for PAL) and load capacitance (C) to these pins to form a crystal oscillator circuit.
20	FSCO	O	C	Internal color burst clock output pin. This pin controls internal color burst clock output depending on the FO bit of command 7.
21	CBCK	I	G	External color burst clock input pin
22	PDS	O	D	Pin for output of the result of color burst clock phase comparison
31	YOUT	O	F	Luminance signal output pin. This pin outputs a signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V).
32	YIN	I	E	Luminance signal input pin for superimpose display. This pin inputs a DC-reproduced (DC-clamped) signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V).
34	COUT	O	F	Saturation signal output pin. This pin outputs a signal at 1.57 VDC and a color burst signal amplitude of 0.57 V_{P-P}.
35	CIN	I	E	Saturation signal input pin for superimpose display. This pin inputs a signal at 1.57 VDC and a color burst signal amplitude of 0.57 V_{P-P}.
37	VOUT	O	F	Composite video signal output pin. This pin outputs a signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V).
38	VKIN	I	E	Background level control input pin for halftone background display of external input composite video signals (input to the VIN pin and output from the VOUT pin). Halftone background display is controlled by setting the KID bit of command 5 to “1”.
39	VKOUT	O	F	Background level control output pin for halftone background display of external input composite video signals (input to the VIN pin and output from the VOUT pin). Halftone background display is controlled by setting the KID bit of command 5 to “1”.
40	VIN	I	E	Composite video signal input pin for superimpose display. This pin inputs a DC-reproduced (DC-clamped) signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V).
43	$\overline{\text{READ}}$	O	D	External font memory read control pin. This pin outputs the Low-level signal in the font memory read period. The pin enters the high impedance state when the $\overline{\text{TSC}}$ pin inputs a Low-level signal.

(Continued)

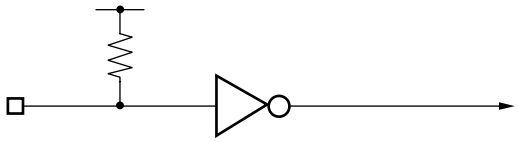
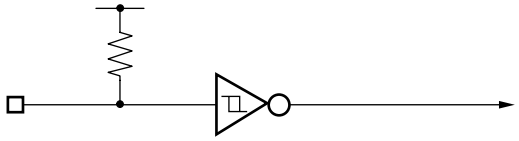
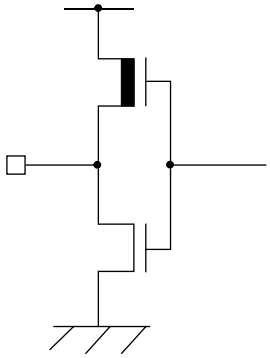
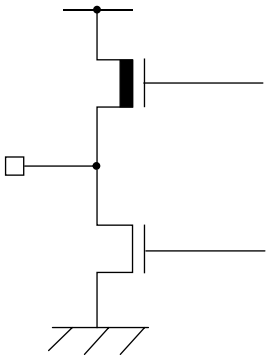
Pin no.	Pin name	I/O	Circuit type	Function
44 45 46 47 48 49 50 51	DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7	I	A	External font memory data input pins. These pins are inputs with an internal pull-up resistor.
53 54 55 56 57 58 59 60 61 63 64 66 67 68 69 70 71 72 73 74 75	ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7 ADR8 ADR9 ADR10 ADR11 ADR12 ADR13 ADR14 ADR15 ADR16 ADR17 ADR18 ADR19 ADR20	O	D	External font memory address output pins. These pins enter the high impedance state when the $\overline{TSC}$ pin inputs a Low-level signal. ADR0 to ADR4: Raster address ADR5 — M0, SM0 (*1, *2) ADR6 — M1, SM1 ADR7 — M2, SM2 ADR8 — M3, SM3 ADR9 — M4, SM4 ADR10 — M5, SM5 ADR11 — M6, SM6 (ADR5 to ADR11: Character code (Lower bits)) ADR12, ADR13: Data distinction bits (12,13 = 00: Left, 10: Center, 01: Right) ADR14 — M7, SM7 ADR15 — M8, SM8 ADR16 — M9, SM9 ADR17 — MA, SMA ADR18 — MB, SMB ADR19 — MC, SMC ADR20 — MD, SMD (ADR14 to ADR20: Character code (Higher bits)) *1: M0 to MD are control bits for main screen character control data setting (the commands 1-1 and 2-1) *2: SM0 to SMD are control bits for sub-screen character control data setting (the commands 1-2 and 2-2)
77	$\overline{TSC}$	I	B	Tristate control input pin for external font memory control bus. When this pin inputs a Low-level signal, the ADR0 to ADR20 pins and the $\overline{READ}$ pin enter the high impedance state. The pin is a hysteresis input with an internal pull-up resistor.
78	$\overline{TEST}$	I	B	Test signal input pin. This pin usually inputs a High-level (fixed) signal.
79 80	EXD XD	I O	I	External circuit pins for display dot clock generator. Connect these pins to external “L” and “C” to form an LC oscillator circuit.

(Continued)

(Continued)

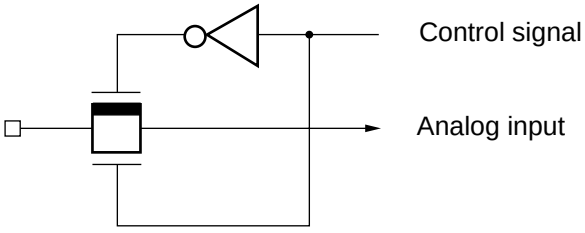
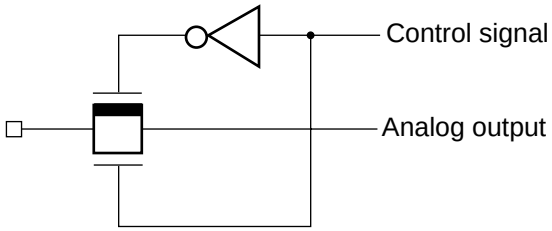
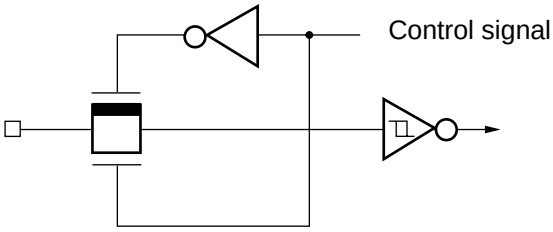
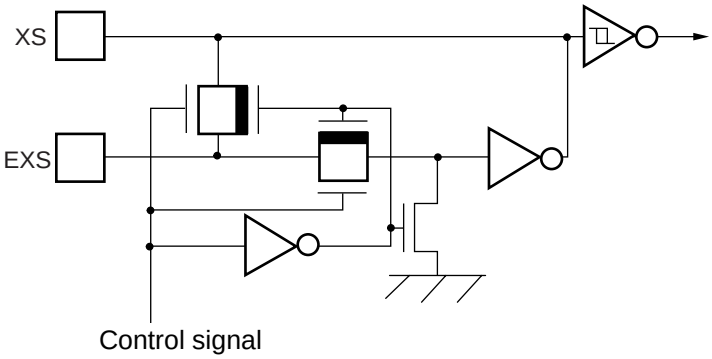
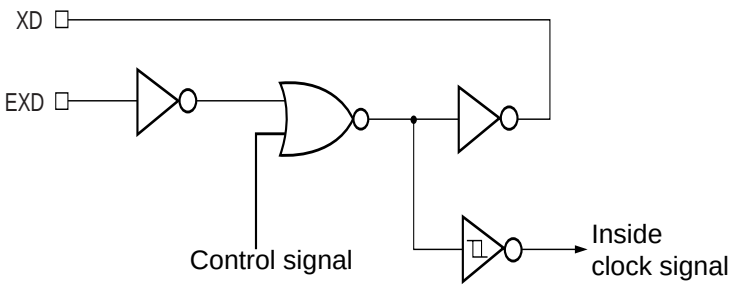
Pin no.	Pin name	I/O	Circuit type	Function
19 25 26 27 28	TEST1 TEST2 TEST3 TEST4 TEST5	O	—	Leave these pins unconnected.
11 42 62 76	V_{CC}	—	—	Power-supply pins (+5 V)
4 23 52 65	V_{SS}	—	—	Ground pins
41	$AV_{CC}1$	—	—	Analog power pin for composite video signals (VIN-VOUT)
33	$AV_{CC}2$	—	—	Analog power pin for luminance (YIN-YOUT) and chroma (CIN-COUT) signals
24 29 30 36	AV_{SS}	—	—	Analog circuit ground pins. Set these pins to the same level as the V_{SS} pin.

■ I / O CIRCUIT TYPE

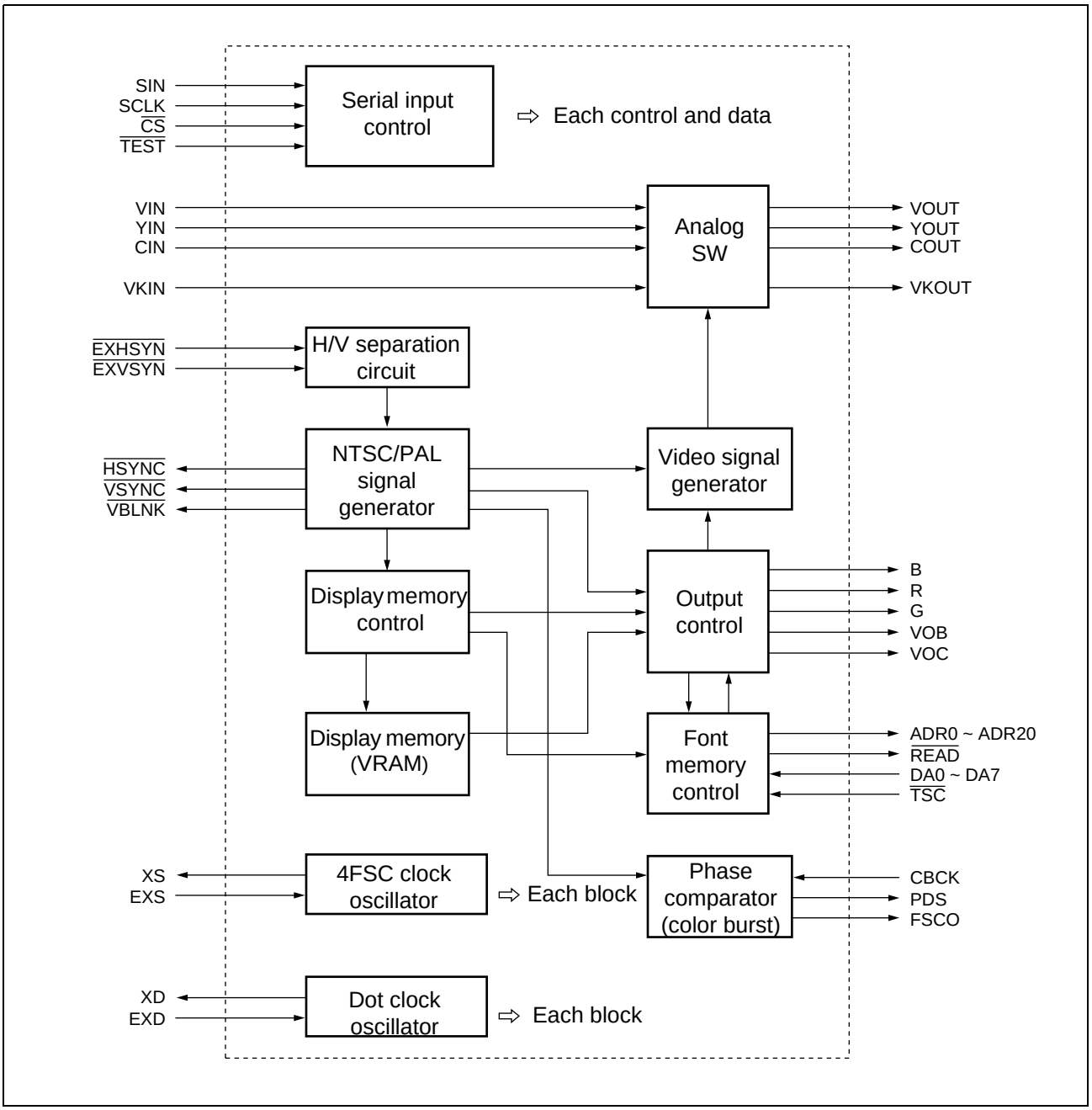
Type	Circuit	Remarks
A		CMOS level input With pull-up resistor: approximately 50 kΩ
B		CMOS level, hysteresis input With pull-up resistor: approximately 50 kΩ
C		CMOS output
D		CMOS three state output

(Continued)

(Continued)

E		Analog input CMOS analog SW
F		Analog output CMOS analog SW
G		CMOS level, hysteresis input
H		Crystal oscillation circuit
I		LC oscillation circuit

■ BLOCK DIAGRAM



■ DISPLAY CONTROL COMMANDS

Command no.	Function	First byte				Second byte							
		Command code/data				Data							
		76543	2	1	0	7	6	5	4	3	2	1	0
0	VRAM address setting	10000	VSL	RA8	RA7	0	RA6	RA5	CA4	CA3	CA2	CA1	CA0
1-1	Main screen character control data setting 1*	10001	MA	MB	AT	0	CG	CR	CB	MC	BG (GR)*	BR (BS)*	BB (MD)*
2-1	Main screen character control data setting 2	10010	M9	M8	M7	0	M6	M5	M4	M3	M2	M1	M0
1-2	Sub-screen line control data setting 1	10001	SMA	SMB	0	0	SCG	SCR	SCB	SMC	SGR	SDC	SMD
2-2	Sub-screen line control data setting 2	10010	SM9	SM8	SM7	0	SM6	SM5	SM4	SM3	SM2	SM1	SM0
1-3	Main screen line control data setting 1	10001	OF1	OF0	0	0	0	0	0	PC	PG	PR	PB
2-3	Main screen line control data setting 2	10010	G2	G1	G0	0	SOC	VD	DG	KC	KG	KR	KB
3	VRAM write control	10011	FIL	0	0	0	0	0	0	0	0	0	0
4	Screen control 1	10100	IE	IN	EB	0	EO	CM	ZM	NP	P2	P0	DC
5	Screen control 2	10101	KID	APC	GYZ	0	BH2	BH1	BH0	W3	W2	W1	W0
6	Main screen line control	10110	G2	G1	G0	0	SOC	VD	DG	N3	N2	N1	N0
7	Main screen vertical display position control	10111	EC	LP	FO	0	0	Y5	Y4	Y3	Y2	Y1	Y0
8	Main screen horizontal display position control	11000	SC	0	FC	0	0	X5	X4	X3	X2	X1	X0
9	Main screen display mode control	11001	0	0	GRM	0	RP1	RP0	S16	SF1	DW4	RM1	RM0
10	Color control	11010	0	0	RB	0	BK	CC	BC	UC	UG	UR	UB
11	Sub-screen control	11011	SG2	SG1	SG0	0	0	SCC	SBC	SGC	SBG	SBR	SBB
12	Sub-screen vertical display position control	11100	SGA	0	SY7	0	SY6	SY5	SY4	SY3	SY2	SY1	SY0
13	Sub-screen horizontal display position control	11101	0	SX8	SX7	0	SX6	SX5	SX4	SX3	SX2	SX1	SX0
14	(Reserved)	11110	—	—	—	0	—	—	—	—	—	—	—
15	(Reserved)	11111	—	—	—	0	—	—	—	—	—	—	—

*: Parenthesized bit names are used for extended graphics mode.

Note: DC bit of screen control 1 (command 4) is initialized at “0” and display is off by reset. All command data and all VRAM are needed to set after release of power-on reset.

■ COMMAND

1. VRAM Address Setting (Command 0)

	MSB							LSB
First byte	1	0	0	0	0	VSL	RA8	RA7
	MSB							LSB
Second byte	0	RA6	RA5	CA4	CA3	CA2	CA1	CA0

VSL : VRAM write control
RA8 to RA5 : VRAM row address setting (0_H to B_H)
CA4 to CA0 : VRAM column address setting (00_H to 17_H)

2. VRAM Data Settings 1 and 2 (Commands 1 and 2)

(1) Writing main screen character control data (when command 0: VSL = 0)

• Command 1-1 (Main screen character control data setting 1)

	MSB							LSB
First byte	1	0	0	0	1	MA	MB	AT
	MSB							LSB
Second byte	0	CG	CR	CB	MC	BG (GR)	BR (BS)	BB (MD) *

*: Parenthesized bit names are used for extended graphics mode.

• Command 2-1 (Main screen character control data setting 2)

	MSB							LSB
First byte	1	0	0	1	0	M9	M8	M7
	MSB							LSB
Second byte	0	M6	M5	M4	M3	M2	M1	M0

(MD), MC to M0 : Character code
AT : Specify character attribute display.
CG, CR, CB : Character colors
BG, BR, BB : Character background colors
(GR) : Specify normal character/graphic character display.
(BS) : Specify shaded background display.

(2) Writing sub-screen line control data (when command 0: VSL = 1, CA0 = 0)

• Command 1-2 (Sub-screen line control data setting 1)

	MSB							LSB
First byte	1	0	0	0	1	SMA	SMB	0
	MSB							LSB
Second byte	0	SCG	SCR	SCB	SMC	SGR	SDC	SMD

• Command 2-2 (Sub-screen line control data setting 2)

	MSB							LSB
First byte	1	0	0	1	0	SM9	SM8	SM7
	MSB							LSB
Second byte	0	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SMD to SM0 : Sub-screen line first character code
SDC : Sub-screen line output control
SGR : Sub-screen line character display control
SCG to SCB : Sub-screen line character colors (when SGR = 0)
SCG : Sub-screen line graphic color transparency control (when SGR = 1)
SCR, SCB : Sub-screen line graphic color phase control (when SGR = 1)

(3) Writing main screen control data (when command 0: VSL = 1, CA0 = 1)

- Command 1-3 (Main screen line control data setting 1)

	MSB							LSB
First byte	1	0	0	0	1	OF1	OF0	0
	MSB							LSB
Second byte	0	0	0	0	PC	PG	PR	PB

- Command 2-3 (Main screen line control data setting 2)

	MSB							LSB
First byte	1	0	0	1	0	G2	G1	G0
	MSB							LSB
Second byte	0	SOC	VD	DG	KC	KG	KR	KB

OF1, OF0	: Character color phase control
PC	: Shaded pattern background color/monochrome control
PG, PR, PB	: Shaded pattern background color
G2, G1, G0	: Character size control
SOC	: Output priority control
VD	: Video signal output control
DG	: Digital signal output control
KC	: Line background color/monochrome control
KG, KR, KB	: Line background color

3. VRAM Write Control (Command 3)

	MSB							LSB
First byte	1	0	0	1	1	FIL	0	0
	MSB							LSB
Second byte	0	0	0	0	0	0	0	0

FIL: VRAM fill control

4. Screen Control 1 (Command 4)

	MSB							LSB
First byte	1	0	1	0	0	IE	IN	EB

	MSB							LSB
Second byte	0	EO	CM	ZM	NP	P2	P0	DC

IE : Internal/external synchronization control
IN : Interlaced/noninterlaced display control
EB : Screen background display control
EO : Field control
CM : Color/monochrome display control
ZM : Zoom-in control
NP : NTSC/PAL control
P2, P0 : Pattern background control
DC : Display control

5. Screen Control 2 (Command 5)

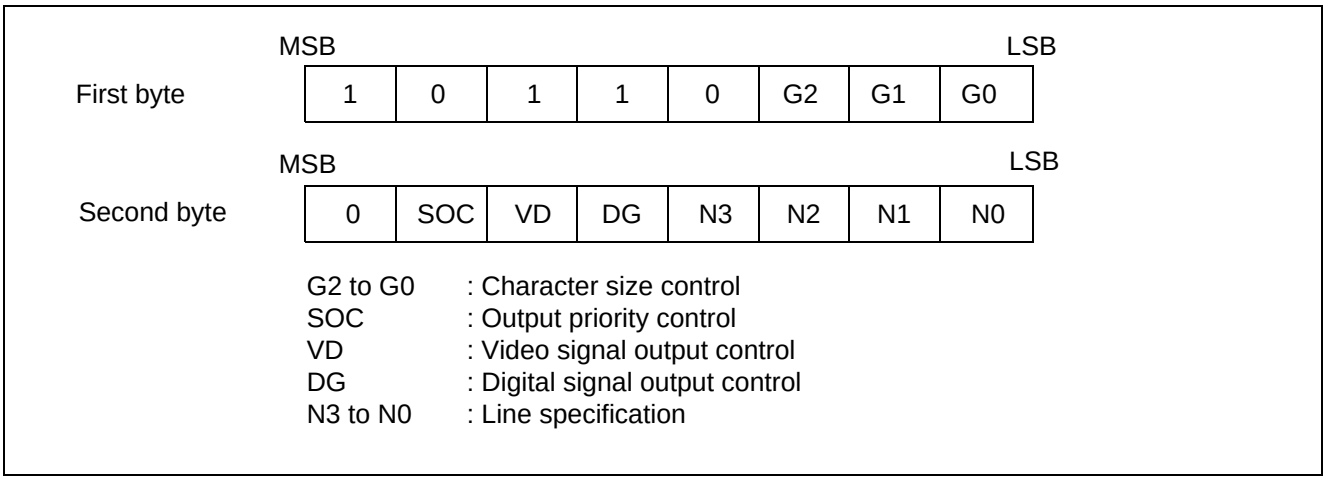
	MSB							LSB
First byte	1	0	1	0	1	KID	APC	GYZ

	MSB							LSB
Second byte	0	BH2	BH1	BH0	W3	W2	W1	W0

KID : Halftone control
APC : Reserve*
GYZ : Main screen line enlargement control
BH2 to BH0 : Reserve*
W3 to W0 : Main screen line spacing control

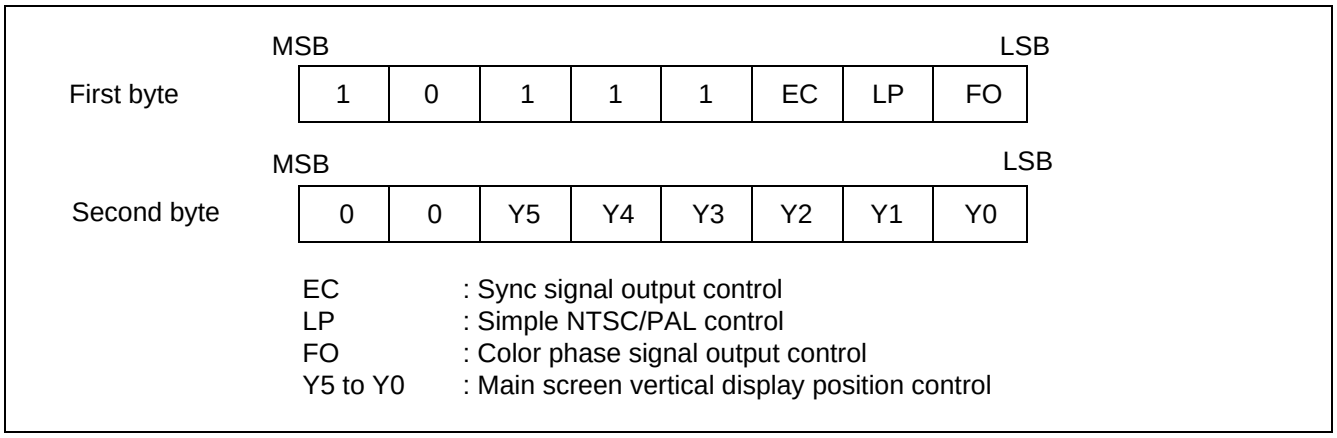
*: Reserve must be set at “ 0 ”.

6. Main Screen Line Control (Command 6)



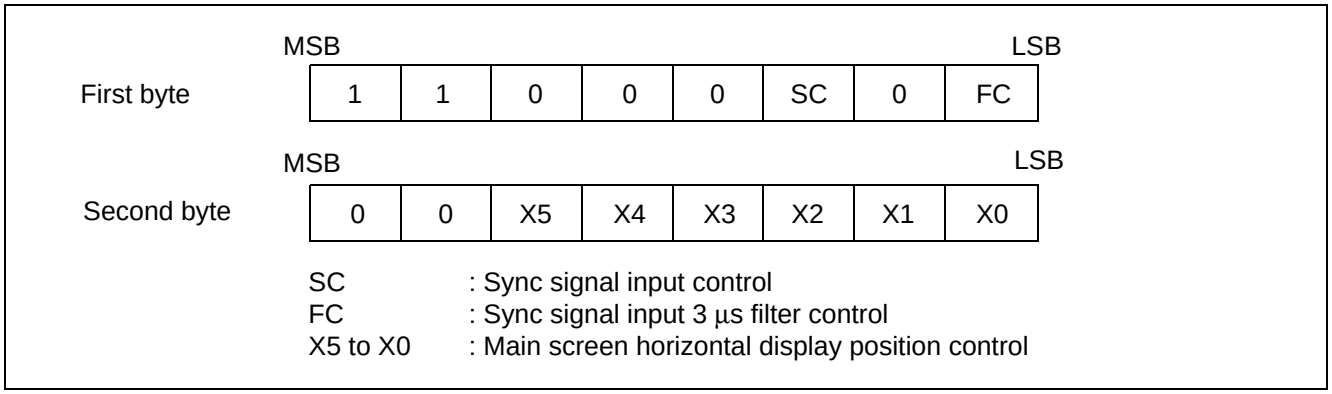
G2 to G0 : Character size control
SOC : Output priority control
VD : Video signal output control
DG : Digital signal output control
N3 to N0 : Line specification

7. Main Screen Vertical Display Position Control (Command 7)



EC : Sync signal output control
LP : Simple NTSC/PAL control
FO : Color phase signal output control
Y5 to Y0 : Main screen vertical display position control

8. Main Screen Horizontal Display Position Control (Command 8)



SC : Sync signal input control
FC : Sync signal input 3 μs filter control
X5 to X0 : Main screen horizontal display position control

9. Main Screen Display Mode Control (Command 9)

	MSB							LSB
First byte	1	1	0	0	1	0	0	GRM

	MSB							LSB
Second byte	0	RP1	RP0	S16	SF1	DW4	RM1	RM0

GRM: Main screen display mode control
RP1, RPO : Reserve 4*
S16 : Reserve 3*
SF1 : Reserve 2*
DW4 : Reserve 1*
RM1, RM0 : Reserve 0*

*: Reserve 0 to reserve 4 must be set at “0”.

10. Color Control (Command 10)

	MSB							LSB
First byte	1	1	0	1	0	0	0	RB

	MSB							LSB
Second byte	0	BK	CC	BC	UC	UG	UR	UB

RB : Main screen solid-fill background display control
BK : Main screen blink display control
CC : Main screen character color/monochrome control
BC : Main screen character background color/monochrome control
(Main screen graphic color/monochrome control)
UC : Screen background color/monochrome control
UG, UR, UB : Screen background color

11. Sub-Screen Control (Command 11)

	MSB							LSB
First byte	1	1	0	1	1	SG2	SG1	SG0
	MSB							LSB
Second byte	0	0	SCC	SBC	SGC	SBG	SBR	SBB

SG2 to SG0 : Sub-screen configuration control
SCC : Sub-screen character color/monochrome control
SBC : Sub-screen character background color/monochrome control
SGC : Sub-screen graphic color/monochrome control
SBG, SBR, SBB : Sub-screen pattern background color

12. Sub-Screen Vertical Display Position Control (Command 12)

	MSB							LSB
First byte	1	1	1	0	0	SGA	0	SY7
	MSB							LSB
Second byte	0	SY6	SY5	SY4	SY3	SY2	SY1	SY0

SGA : Sub-screen full-screen mode control
SY7 to SY0 : Sub-screen vertical display position

13. Sub-Screen Horizontal Display Position Control (Command 13)

	MSB							LSB
First byte	1	1	1	0	1	0	SX8	SX7
	MSB							LSB
Second byte	0	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX8 to SX0 : Sub-screen horizontal display position

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*1
	$AV_{CC}1$	V_{SS} – 0.3	V_{SS} + 7.0	V	*1
	$AV_{CC}2$	V_{SS} – 0.3	V_{SS} + 7.0	V	*1
Input voltage	V_{IN}	V_{SS} – 0.3	V_{SS} + 7.0	V	*2
Output voltage	V_{OUT}	V_{SS} – 0.3	V_{SS} + 7.0	V	*2
Power consumption	Pd	—	600	mW	
Operating temperature	Ta	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: AV_{SS} and V_{SS} must have equal potential.

*2: Neither V_{IN} nor V_{OUT} must exceed "V_{CC} + 0.3 V."

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	4.5	5.5	V	Specification guarantee range
	$AV_{CC}1$	4.5	5.5	V	*1, *2
	$AV_{CC}2$	4.5	5.5	V	*1, *3
"H" level input voltage	V_{IHS1}	2.2	V_{CC} + 0.3	V	DA0 to DA7
	V_{IHS2}	0.8 × V_{CC}	V_{CC} + 0.3	V	Except DA0 to DA7
"L" level input voltage	V_{ILS1}	–0.3	+ 0.8	V	DA0 to DA7
	V_{ILS2}	–0.3	0.2 × V_{CC}	V	Except DA0 to DA7
Operating temperature	Ta	–40	+85	°C	
Analog input voltage	AV_{IN}	0	V_{CC}	V	

*1: AV_{SS} and V_{SS} must have equal potential.

*2: "$AV_{CC}1$ = AV_{SS}" is allowed if composite video signals (VIN-VOUT pins) are not used.

*3: "$AV_{CC}2$ = AV_{SS}" is allowed if Y/C-separated video signals (YIN-YOUT and CIN-COUT pins) are not used.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Ta = –40°C to +85°C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	VOC, $\overline{\text{VOB}}$, B, R, G, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{VBLNK}}$, FSCO, $\overline{\text{READ}}$, ADR0 to ADR20	V_{CC} = 4.5 V I_{OH} = –2 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}		V_{CC} = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
Input current	I_{IL}	$\overline{\text{TESTI}}$, $\overline{\text{CS}}$, SCLK, SIN, $\overline{\text{EXHSYN}}$, $\overline{\text{EXVSYN}}$, CBCK, DA0 to DA7, $\overline{\text{TSC}}$, $\overline{\text{TEST}}$	V_{CC} = 5.5 V V_{IL} = 0.0 V	–200	—	–50	µA	
Supply current	I_{CC}	V_{CC}, $AV_{CC}1$, $AV_{CC}2$	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 5.5 V 4fsc = 17.734475 MHz f_{DC} = 16.0 MHz No load	—	—	50	mA	
Analog supply current	I_A	$AV_{CC}1$, $AV_{CC}2$	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 5.5 V 4fsc = f_{DC} = 0 MHz AV_{IN} = 1.65 V No load	—	—	30	mA	
ON resistance	R_{ON}	VIN-VOUT, YIN-YOUT, CIN-COUT, VIN-VKOUT, VKIN-VOUT	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 4.5 V I_{OL} = 100 µA	—	100	320	Ω	
Off leakage current	I_{OFF}	VIN, YIN, CIN, VKIN	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 5.5 V AV_{IN} = 5.5 V	—	0.1	10	µA	
Output resistance	R_{OUT}	VOUT, YOUT, COUT, VKOUT	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 4.5 V I_{OL} = 100 µA	100	—	1800	Ω	

(Continued)

(Ta = –40°C to +85°C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min.	Typ.	Max.		
Yellow High level	V_{YELH}	VOUT	V_{CC} = AV_{CC}1 = AV_{CC}2 = 5.0 V	2.89	3.00	3.11	V	See Figure "VOUT output"
Yellow Low level	V_{YELL}			2.03	2.14	2.25	V	
Cyan High level	V_{CYAH}			2.89	3.00	3.11	V	
Cyan Low level	V_{CYAL}			1.63	1.74	1.85	V	
Green High level	V_{GREH}			2.66	2.77	2.88	V	
Green Low level	V_{GREL}			1.63	1.74	1.85	V	
Magenta High level	V_{MAGH}			2.49	2.60	2.71	V	
Magenta Low level	V_{MAGL}			1.46	1.57	1.68	V	
Red High level	V_{REDH}			2.49	2.60	2.71	V	
Red Low level	V_{REDL}			1.23	1.34	1.45	V	
Blue High level	V_{BLUH}			2.15	2.26	2.37	V	
Blue Low level	V_{BLUL}			1.23	1.34	1.45	V	
Color burst High level	V_{BSTH}			1.80	1.91	2.02	V	
Color burst Low level	V_{BSTL}			1.12	1.23	1.34	V	

(Continued)

(Ta = –40°C to +85°C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Values			Unit	Remarks
				Min.	Typ.	Max.		
White level 3 ϕ = – 270°	V_{WHT3} Y_{WHT3}	VOUT, YOUT	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 5.0 V	2.83	2.94	3.05	V	See Figures "VOUT Output" and "YOUT Output".
White level 2 ϕ = – 180°	V_{WHT2} Y_{WHT2}			2.72	2.83	2.94	V	
White level 1 ϕ = – 90°	V_{WHT1} Y_{WHT1}			2.60	2.71	2.82	V	
White level 0 ϕ = 0°	V_{WHT0} Y_{WHT0}			2.49	2.60	2.71	V	
Gray level 6	V_{GRY6} Y_{GRY6}			2.43	2.54	2.65	V	
Gray level 5	V_{GRY5} Y_{GRY5}			2.26	2.37	2.48	V	
Gray level 4	V_{GRY4} Y_{GRY4}			2.15	2.26	2.37	V	
Gray level 3	V_{GRY3} Y_{GRY3}			1.98	2.09	2.20	V	
Gray level 2	V_{GRY2} Y_{GRY2}			1.86	1.97	2.08	V	
Gray level 1	V_{GRY1} Y_{GRY1}			1.69	1.80	1.91	V	
Black level 3 ϕ = – 270°	V_{BLK3} Y_{BLK3}			1.92	2.03	2.14	V	
Black level 2 ϕ = – 180°	V_{BLK2} Y_{BLK2}			1.80	1.91	2.02	V	
Black level 1 ϕ = – 90°	V_{BLK1} Y_{BLK1}			1.69	1.80	1.91	V	
Black level 0 ϕ = 0°	V_{BLK0} Y_{BLK0}			1.57	1.68	1.79	V	
Pedestal level	V_{PDS} Y_{PDS}			1.46	1.57	1.68	V	
SYNC level	V_{TIP} Y_{TIP}			0.84	1.00	1.16	V	

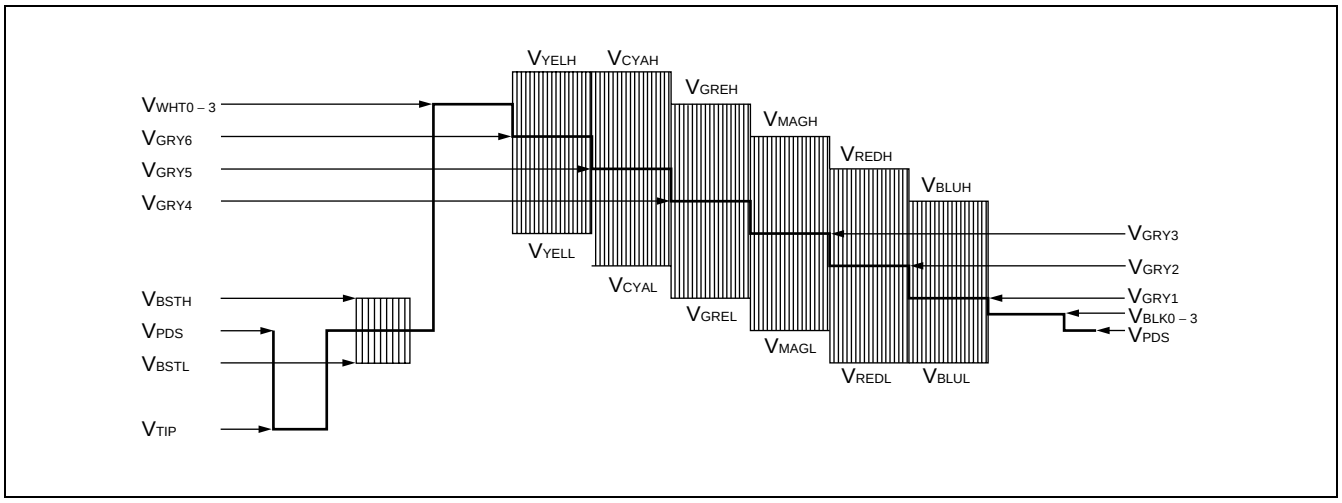
(Continued)

(Continued)

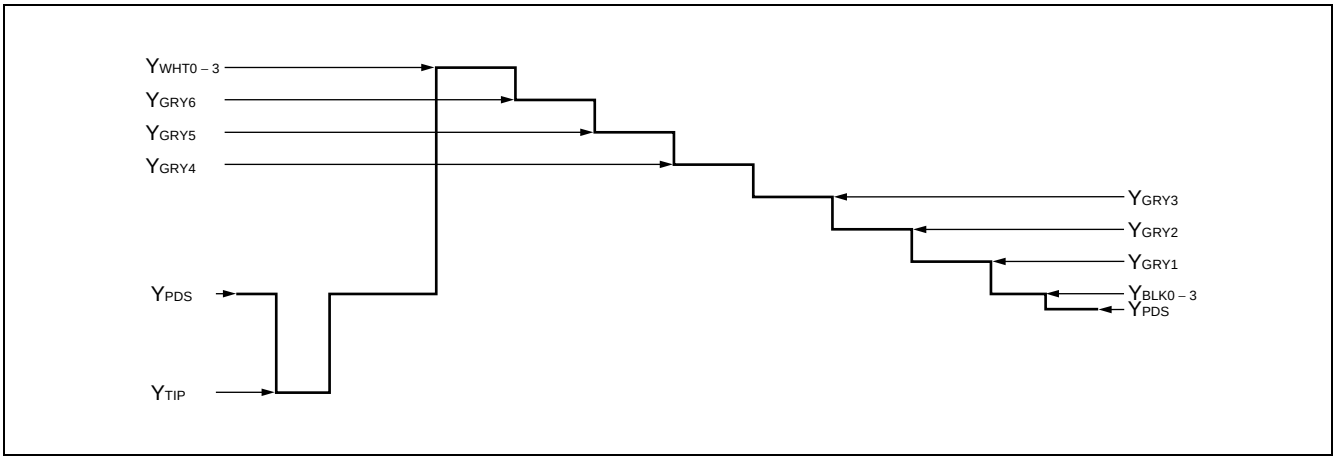
(Ta = –40°C to +85°C, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Conditions	Value			Unit	Remarks
				Min.	Typ.	Max.		
Yellow High level	C_{YELH}	COUT	V_{CC} = $AV_{CC}1$ = $AV_{CC}2$ = 5.0 V	1.92	2.03	2.14	V	See Figure "COUT Output"
Yellow Low level	C_{YELL}			1.00	1.11	1.22	V	
Cyan High level	C_{CYAH}			2.09	2.20	2.31	V	
Cyan Low level	C_{CYAL}			0.89	1.00	1.11	V	
Green High level	C_{GREH}			1.98	2.09	2.20	V	
Green Low level	C_{GREL}			0.95	1.06	1.17	V	
Magenta High level	C_{MAGH}			1.98	2.09	2.20	V	
Magenta Low level	C_{MAGL}			0.95	1.06	1.17	V	
Red High level	C_{REDH}			2.09	2.20	2.31	V	
Red Low level	C_{REDL}			0.89	1.00	1.11	V	
Blue High level	C_{BLUH}			1.92	2.03	2.14	V	
Blue Low level	C_{BLUL}			1.00	1.11	1.22	V	
Color burst High level	C_{BSTH}			1.80	1.91	2.02	V	
Color burst Low level	C_{BSTL}			1.12	1.23	1.34	V	
Pedestal level	C_{PDSC}			1.46	1.57	1.68	V	

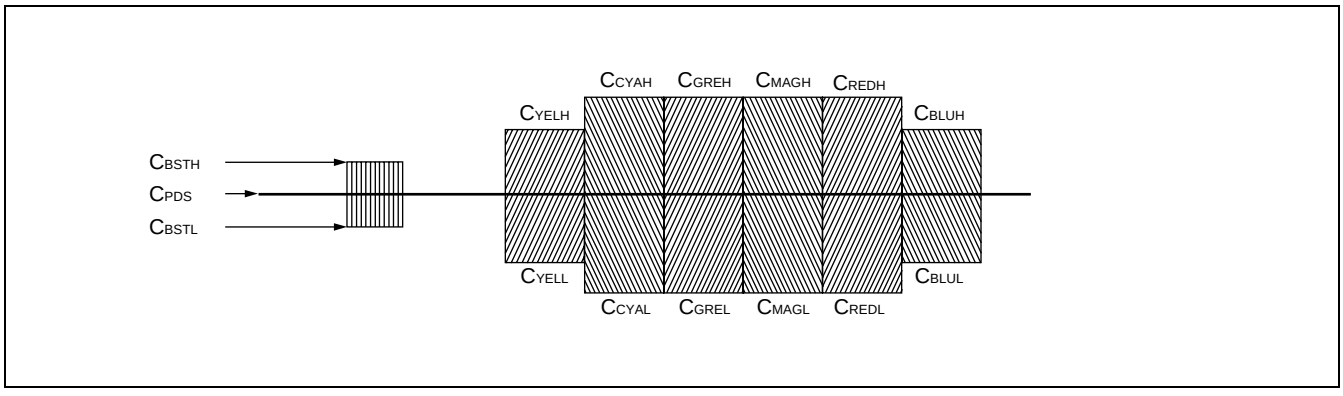
- **VOUT Output**



- **YOUT Output**



- **COUT Output**



2. AC Characteristics

(Ta = –40°C to +85°C, V_{CC} = 5.0 V±10%, V_{SS} = 0 V)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Shift clock cycle time	t_{CYC}	SCLK	1000	—	ns	See Figure "Serial Input Timings".
Shift clock pulse width	t_{WCH}	SCLK	450	—	ns	
	t_{WCL}		450	—	ns	
Shift clock signal rise/fall time	t_{CR}	SCLK	—	200	ns	
	t_{CF}		—	200	ns	
Shift clock start time	t_{SS}	SCLK	200	—	ns	
Data setup time	t_{SU}	SIN	200	—	ns	
Data hold time	t_H	SIN	100	—	ns	
Chip select end time	t_{EC}	$\overline{CS}$	500	—	ns	
Chip select signal rise/fall time	t_{CRC}	$\overline{CS}$	—	200	ns	
	t_{CFC}		—	200	ns	
Horizontal sync signal rise time	t_{HR}	$\overline{EXHSYN}$	—	200	ns	See Figure "Vertical and Horizontal Sync Signal Input Timings".
Horizontal sync signal fall time	t_{HF}	$\overline{EXHSYN}$	—	200	ns	
Vertical sync signal rise time	t_{VR}	$\overline{EXVSYN}$	—	200	ns	
Vertical sync signal fall time	t_{VF}	$\overline{EXVSYN}$	—	200	ns	
Horizontal sync signal pulse width*1	t_{WH}	$\overline{EXHSYN}$	4.0	8.0	µs	
Vertical sync signal pulse width *1	t_{WV}	$\overline{EXVSYN}$	1	5	H	
Horizontal sync detection pulse width *2	t_{WCSH}	$\overline{EXHSYN}$	4.0	8.0	µs	See Figure "Composite Sync Signal input Timings".
Vertical sync detection pulse width*2	t_{WCSV}	$\overline{EXHSYN}$	13	28	µs	
Reset input pulse width	t_{WR}	$\overline{TESTI}$ ($\overline{TEST}$ = Low)*3	10	—	µs	See Figure "Reset Signal Input Timing".
ROM read cycle *4	t_{rcyc}	—	250	500	ns	See Figure "Address Data Hold Timings".
Address valid delay	t_{ab}	ADR0 to ADR20	—	60	ns	
$\overline{READ}$ active delay	t_{ra}	$\overline{READ}$	—	38	ns	
Read data setup time	t_{ds}	DA0 to DA7	30	—	ns	
Read data hold time	t_{dh}	DA0 to DA7	30	—	ns	
Address invalid delay	t_{ai}	ADR0 to ADR20	0	—	ns	
$\overline{READ}$ inactive delay	t_{ri}	$\overline{READ}$	0	—	ns	
Tristate address delay	t_{tad}	ADR0 to ADR20	—	100	ns	See Figure "Address and $\overline{READ}$ Signal Delays at $\overline{TSC}$ Signal Input"
Tristate $\overline{READ}$ delay	t_{trd}	$\overline{READ}$	—	100	ns	

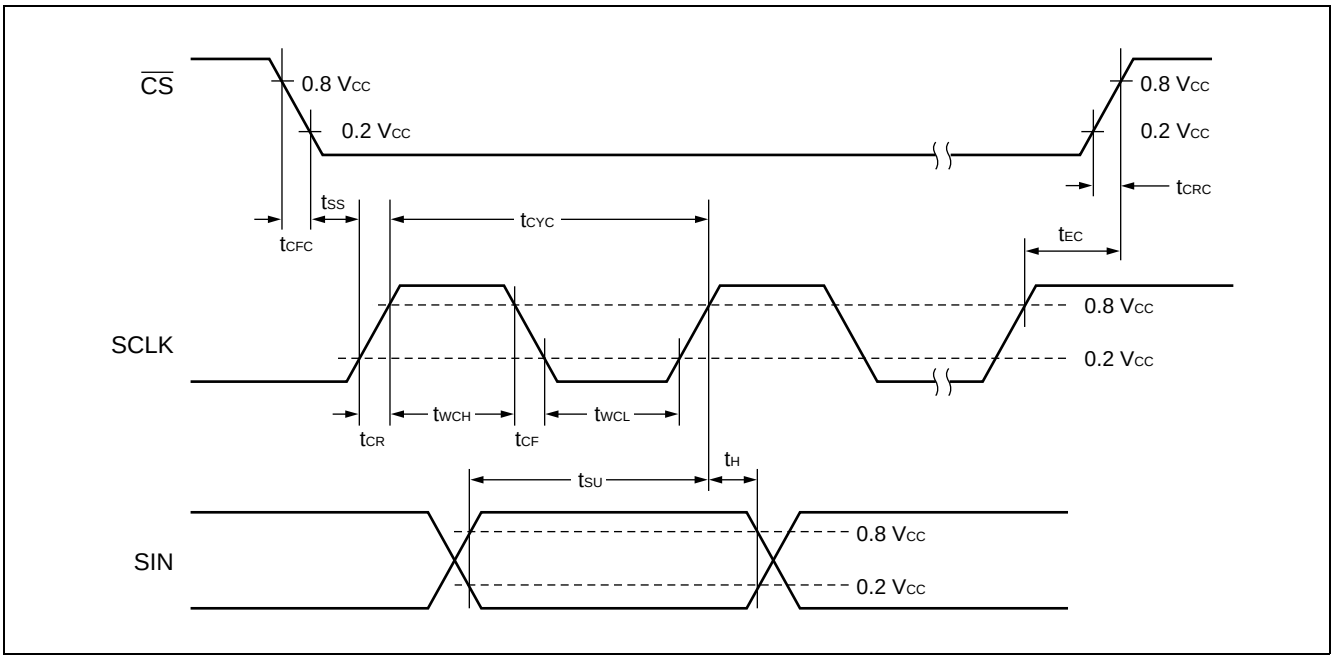
*1: The values assume H/V-separated sync signal input.

*2: The values assume composite sync signal input.

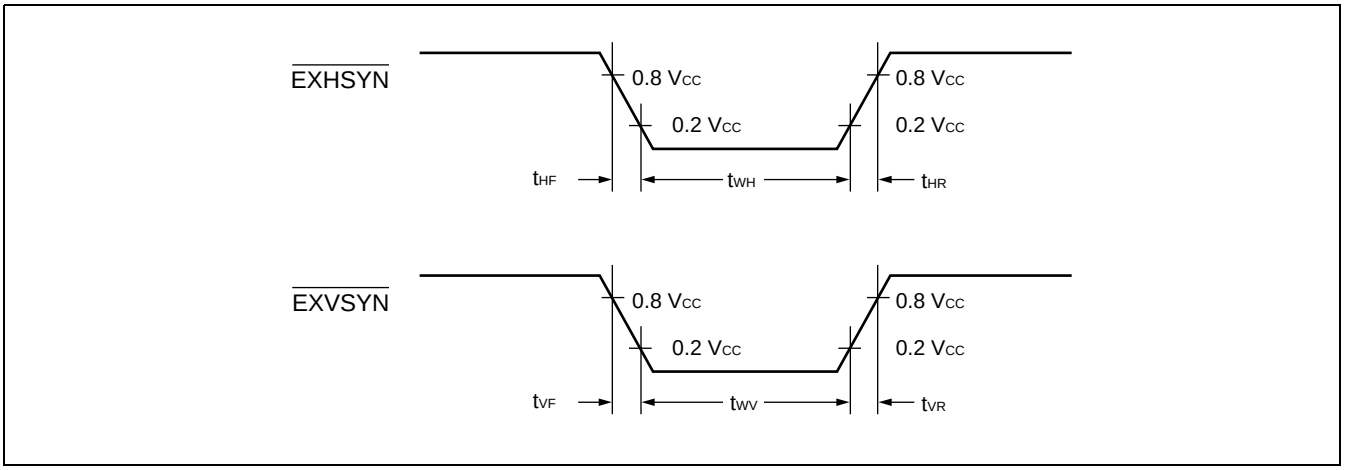
*3: When the $\overline{TEST}$ pin is a Low-level input, the $\overline{TESTI}$ pin serves as a reset pin input. (The $\overline{TESTI}$ and $\overline{TEST}$ pins can be Low level at the same time.)

*4: Depends on the dot clock oscillation frequency. (t_{rcyc} = 4/f_{DC})

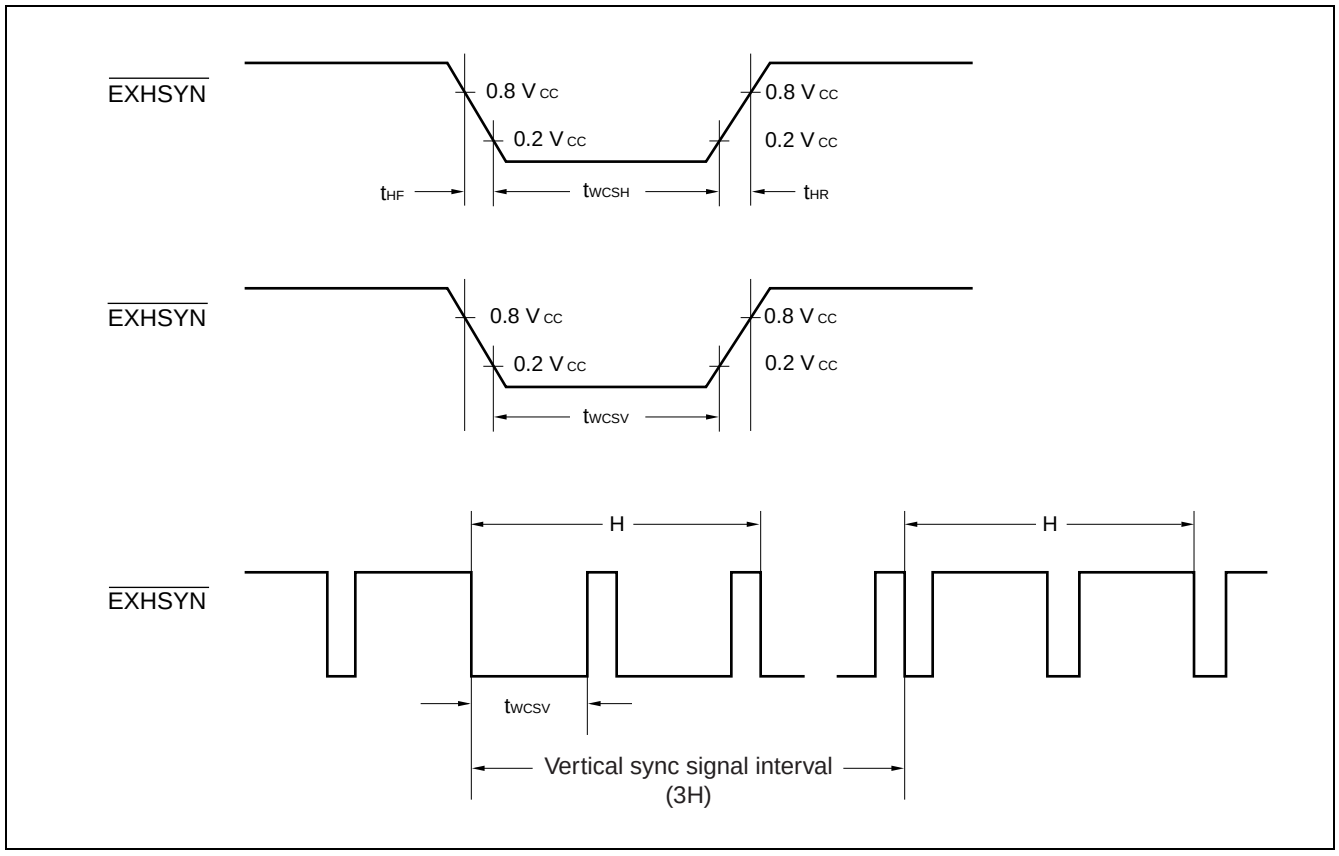
- **Serial Input Timings**



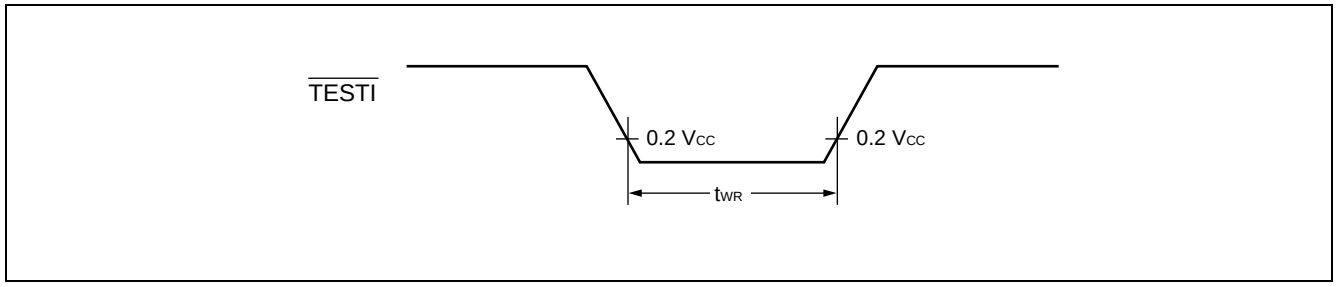
- **Vertical and Horizontal Sync Signal Input Timings**



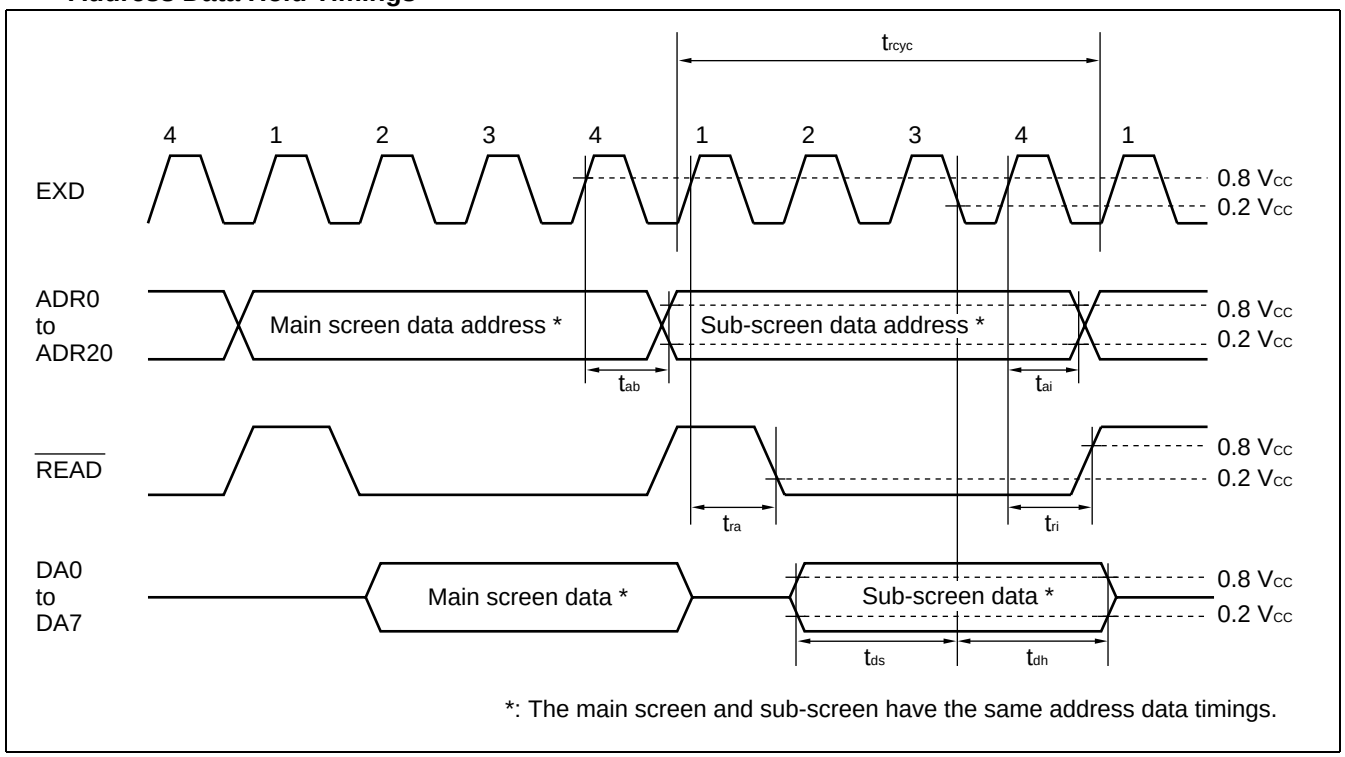
- **Composite Sync Signal Input Timings**



- **Reset Signal Input Timing**

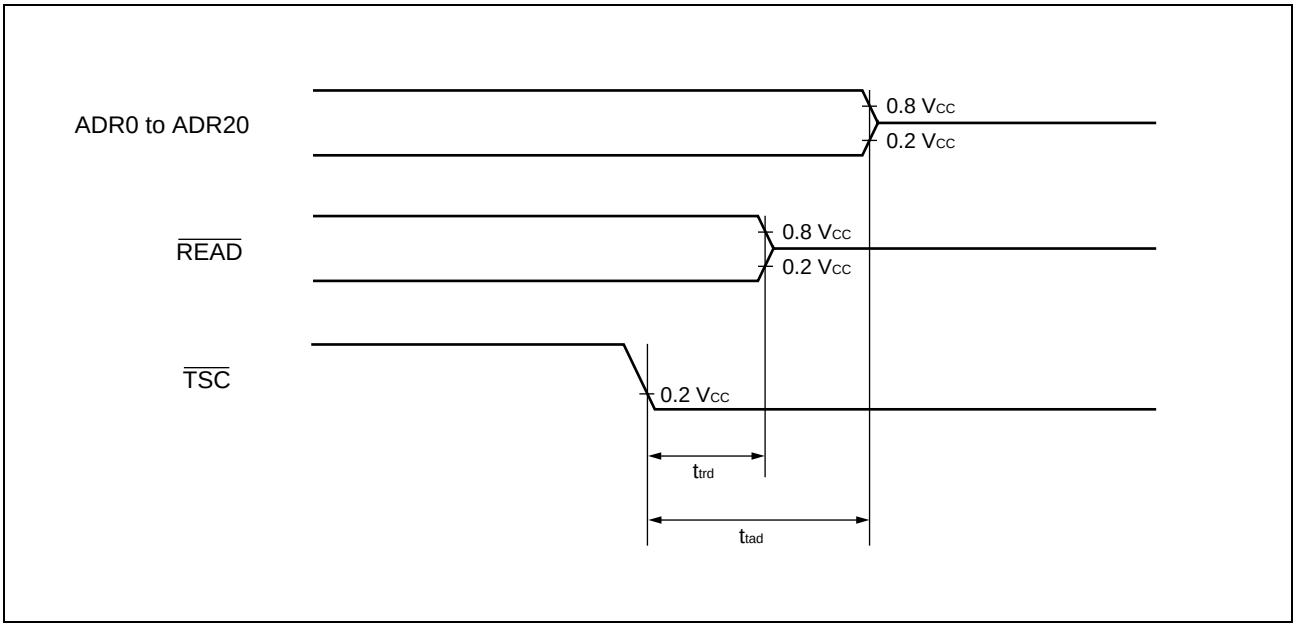


- **Address Data Hold Timings**



*: The main screen and sub-screen have the same address data timings.

- **Address and $\overline{\text{READ}}$ Signal Delays at $\overline{\text{TSC}}$ Signal Input**



3. Clock Timing Specifications

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Display dot clock*	f_{DC}	EXD, XD	8	—	16	MHz	
Color burst clock (NTSC)*	4 f_{SC}	EXS, XS	—	14.318185	—	MHz	
Color burst clock (PAL)*			—	17.734475	—	MHz	

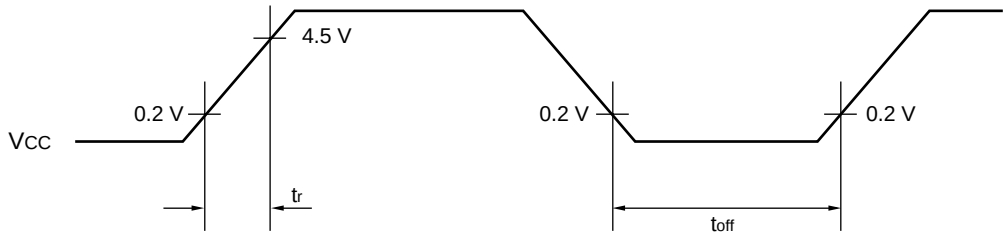
* : Input the signal with a duty cycle of 50%.

4. Power-on Reset Specifications

(Ta = –40°C to +85°C)

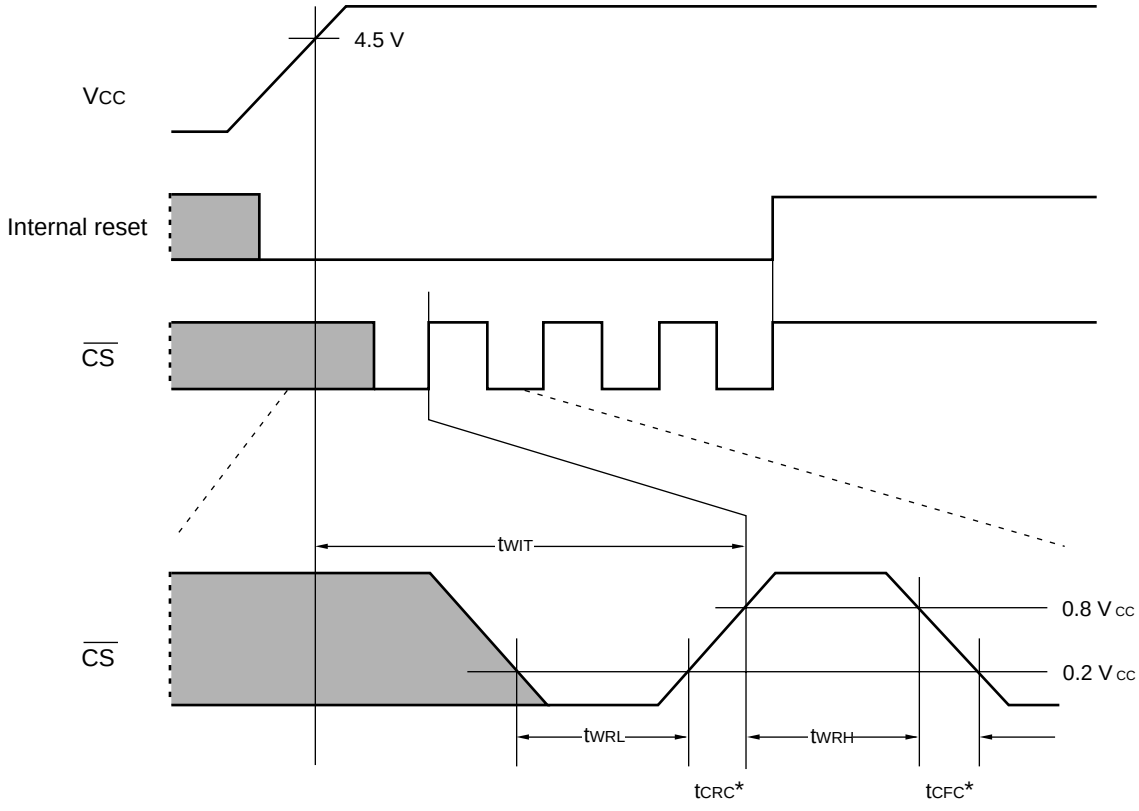
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Power-supply rise time	t_r	V_{CC}	0.05	50	ms	Conditions which activate the power-on reset circuit (See Figure “Power ON/ OFF Timing”).
Power-supply off time	t_{off}		1	—	ms	Conditions in which the circuit repeatedly operate normally (See Figure “Power ON/OFF Timing”).
Time after power-supply rise	t_{WIT}	$\overline{CS}$	450	—	ns	Power-on reset cancel timing (See Figure “Power-on Reset Cancel Timing”).
Reset cancel pulse width	t_{WRH}		450	—	ns	
	t_{WRL}		450	—		

- **Power ON/OFF Timing**



Note: The power supply must be activated smoothly.

- **Power-on Reset Cancel Timing**



*: See Section 2, “AC Characteristics”.

5. Recommended Input Timings

(1) Composite sync signal input timing

Parameter	NTSC	PAL	Unit	Remarks
Number of frame scan lines	525	625	Lines	
Field frequency	60 (59.94)	50	Hz	*1
Line frequency	15750 (15734.264)	15625	Hz	*1
Vertical retrace blanking interval	19 to 21	25	H	*2
First equalizing pulse interval	3	2.5	H	*2
Vertical sync pulse interval	3	2.5	H	*2
Second equalizing pulse interval	3	2.5	H	*2
Equalizing pulse width	2.29 to 2.54	2.34 to 2.36	µs	
Equalizing pulse cycle	0.5	0.5	H	*2
Cut-in pulse width	3.81 to 5.34	4.5 to 4.9	µs	
Cut-in pulse cycle	0.5	0.5	H	*2
Horizontal sync signal cycle	63.492 (63.5555)	64	µs	
Horizontal sync signal pulse width	4.19 to 5.71 (4.7±0.1)	4.5 to 4.9	µs	*1
Horizontal retrace blanking interval	10.2 to 11.4 (10.5 to 11.4)	11.7 to 12.3	µs	*1

*1: Parenthesized values are specifications for color information display.

*2: 1 H is assumed to be one horizontal sync signal period.

(2) H/V-separated sync signal input timing

Parameter	NTSC	PAL	Unit	Remarks
Vertical sync signal frequency	60 (59.94)	50	Hz	*1
Vertical sync signal pulse width	1 to 5	1 to 4	H	*2
Horizontal sync signal cycle	63.492 (63.5555)	64	µs	*1
Horizontal sync signal pulse width	4.19 to 5.71 (4.7±0.1)	4.5 to 4.9	µs	*1

*1: Parenthesized values are specifications for color information display.

*2: 1 H is assumed to be one horizontal sync signal period.

6. Output Timings

(1) Horizontal timing

Symbol	NTSC	PAL	Remarks
HPS	0	0	See Figure “NTSC/PAL Horizontal Timings”.
EQP1E	34	42	
HPE	68	84	
BSTS	76	100	
BSTE	112	140	
HBLKE	143	186	
SEP1S	388	484	
EQP2S	455	568	
EQP2E	489	610	
SEP2S	842	1050	
HBLKS	888	1106	
IHCLR	910	1135 (1137)*	

*: Parenthesized values assume the last raster in each V cycle (field).

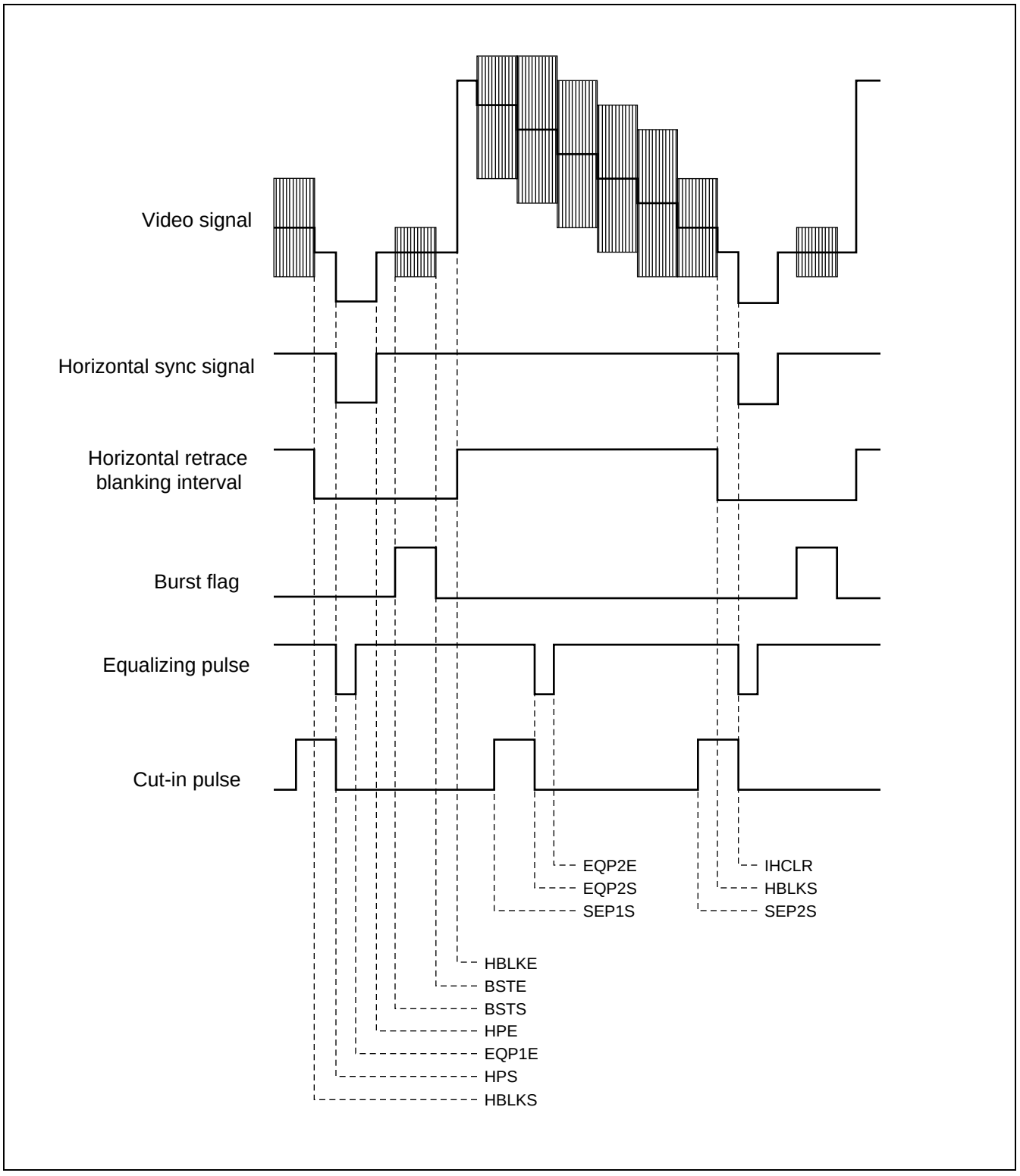
Note: The values in the above list are $4f_{SC}$ count values.

(2) Vertical timing

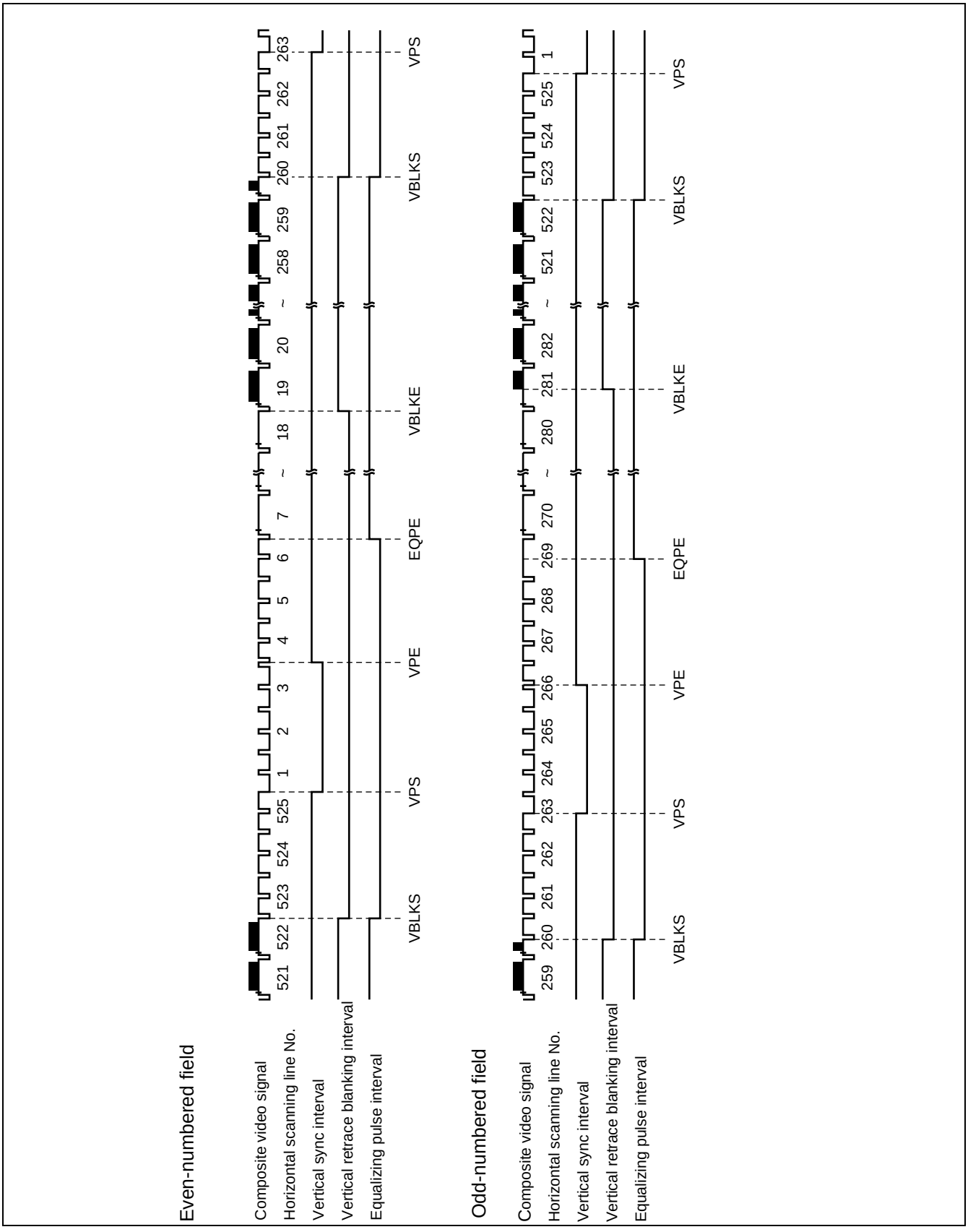
Symbol	NTSC		PAL		Remarks
	Interlaced	Noninterlaced	Interlaced	Noninterlaced	
VPS	0	0	0	0	See Figures “NTSC Vertical Timings” and “PAL Vertical Timings”.
VPE	6	6	5	5	
EQPE	12	12	10	10	
VBLKE	36	36	45	45	
VBLKS	519	519	620	620	
VPS	525	526	625	624	

Note: The values in the above list are 1/2H count values.

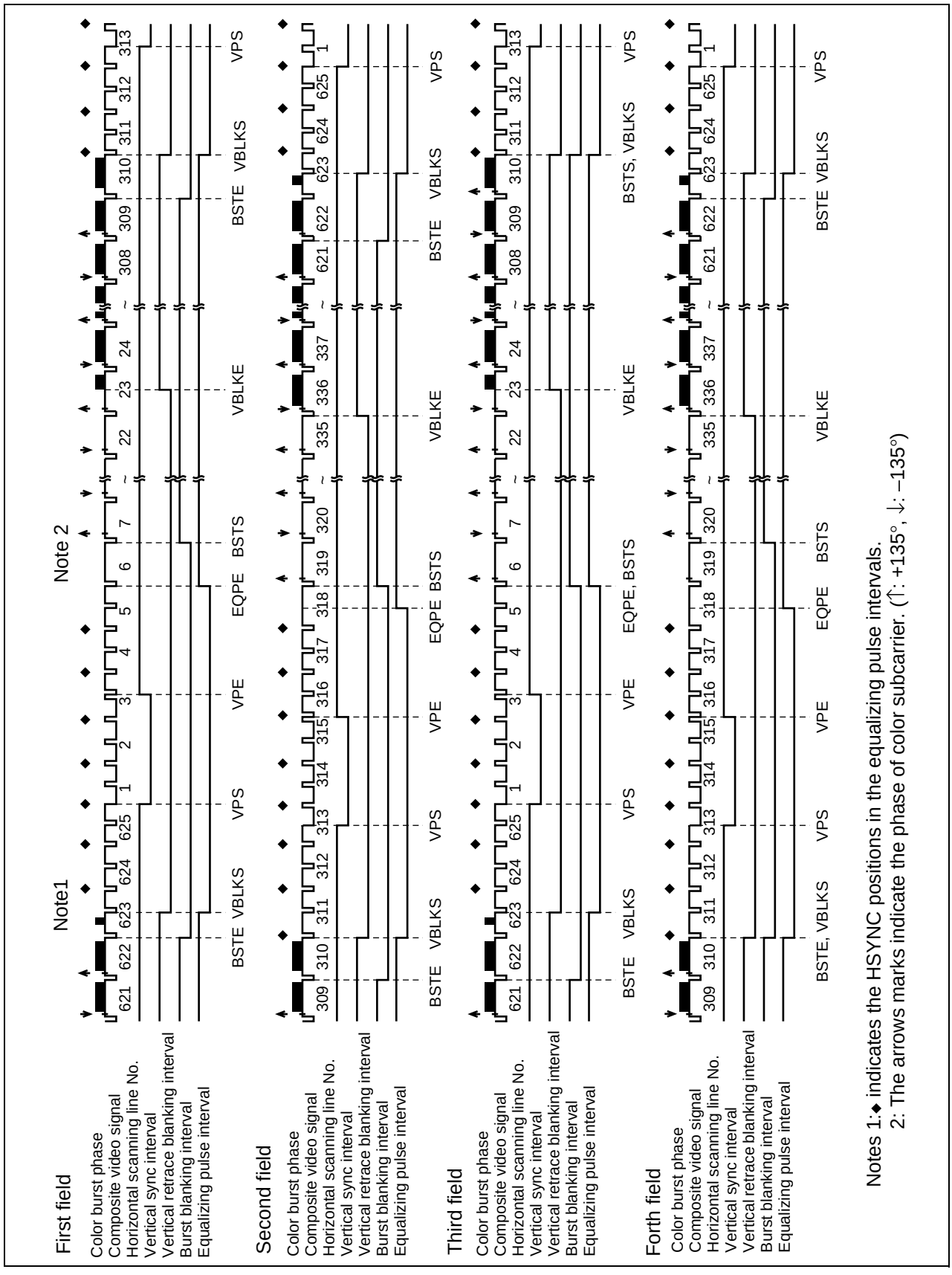
- **NTSC/PAL Horizontal Timings**



- **NTSC Vertical Timings**



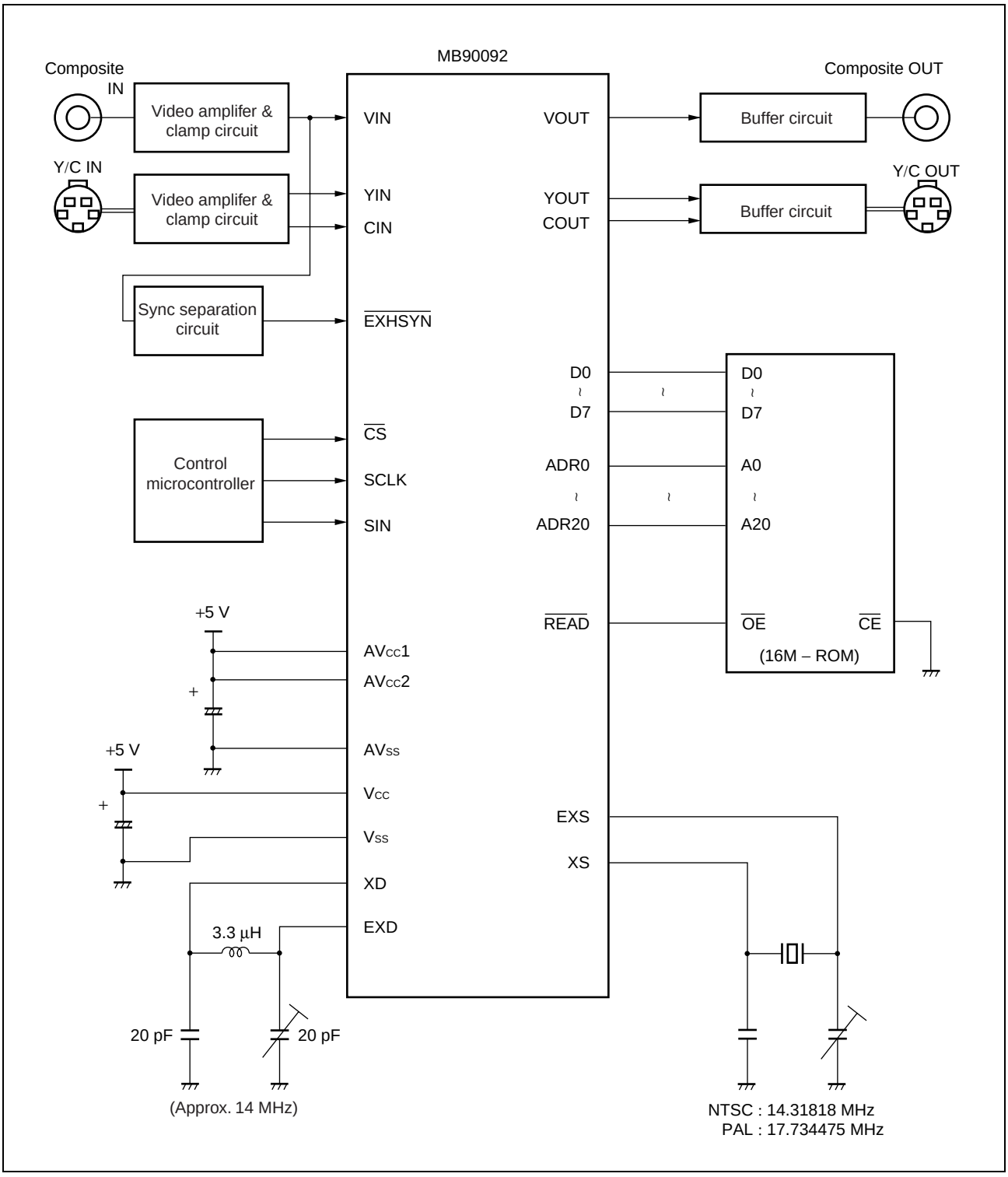
- **PAL Vertical Timings**



Notes 1:◆ indicates the HSYNC positions in the equalizing pulse intervals.
2: The arrows marks indicate the phase of color subcarrier. (↑: +135°, ↓: −135°)

■ SAMPLE CIRCUIT

This is a standard example of the circuit to synthesize the character to input video signal or input internal generation video signal from the outside. Note that composition is different according to the system and parts used.



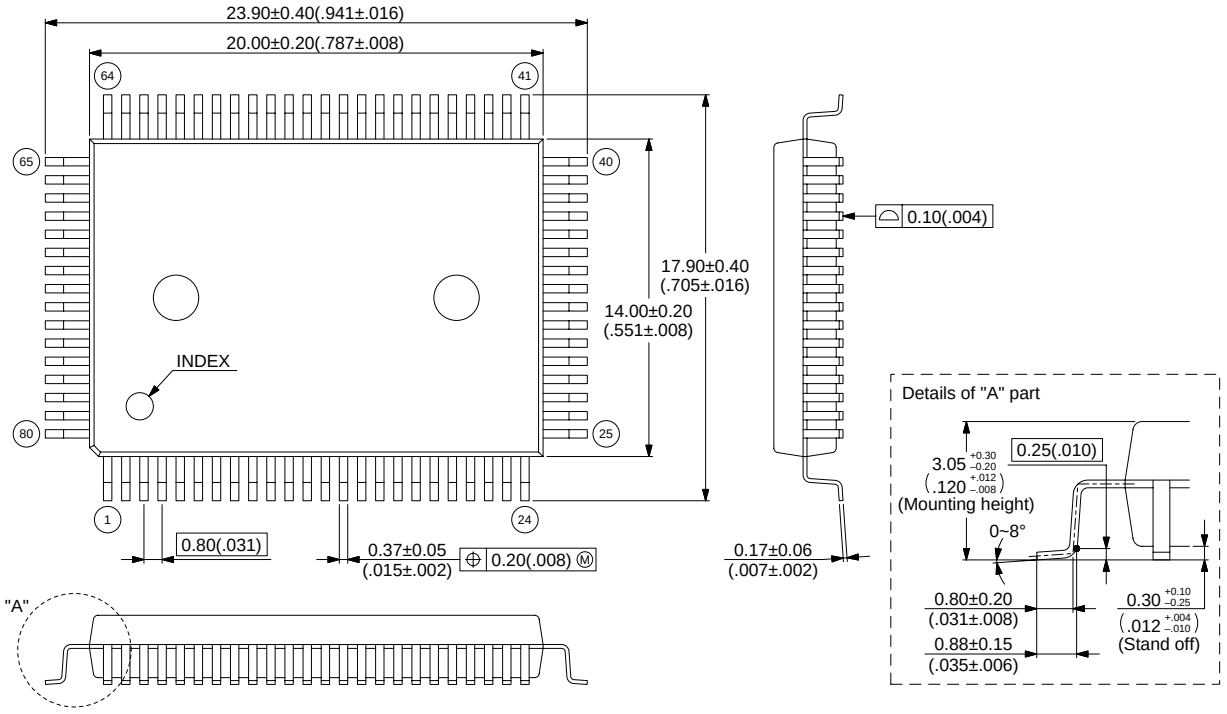
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90092PF	80-pin, plastic QFP (QFP-80P-M06)	

■ PACKAGE DIMENSION

80-pin plastic QFP
(FPT-80P-M06)

Note : Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0108