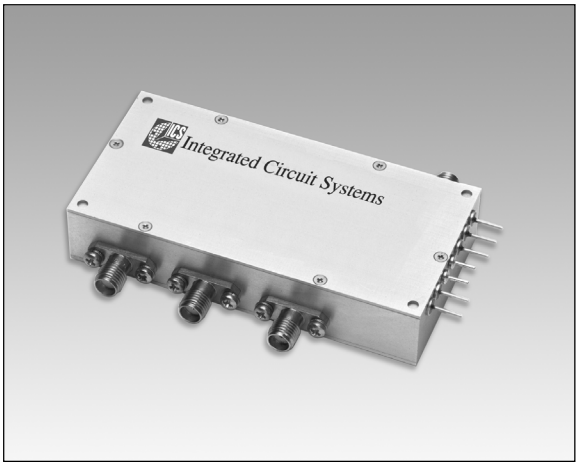
M840 Series

OC-192 MULTI-RATE CLOCK RECOVERY MODULE



FEATURES

- **4 Selectable NRZ or RZ Data Rates: 9.953, 10.3125, 10.664 & 10.709Gb/s**
- **Superior SAW VCO-based PLL Jitter Performance**
- **<2psec RMS Jitter**
- **6mV Peak to Peak Input Sensitivity**
- **Up to 700mV Peak to Peak Un-retimed NRZ or RZ Data Output**
- **Designed and optimized for minimum jitter in accordance with ITU and Bellcore standards for SONET/SDH jitter transfer**

APPLICATIONS

- **SONET OC-192/10GbE Test Equipment**
- **SONET OC-192/SDH STM Physical Layer Clock and Data Recovery**

DESCRIPTION

The M840 Series OC-192 Multi-rate Clock Recovery Module provides low jitter clock recovery from NRZ or RZ input data formats. Four data rates, 9.953, 10.3125, 10.664 or 10.709Gb/s may be selected digitally. The input data is amplified by limiting amplifiers. The amplified data is applied to the clock recovery circuitry and provided as an output at a constant level.

The module incorporates a frequency multiplied high Q SAW VCO in the clock recovery phase-lock loop to minimize the jitter on the recovered clock. The low noise, excellent stability, and low micro-phonic sensitivity of the SAW based VCO to allow operation with a very narrow phase-lock loop bandwidth necessary to minimize pattern dependent clock jitter. The use of micro-strip band pass filters to filter the recovered clock results in a sinusoidal clock output, having low harmonic and sub-harmonic distortion.

The clock recovery circuitry is housed in an easy to interface connectorized module. The discrete circuit design allows for the design to be optimized for various applications and data rates.

ABSOLUTE MAX RATINGS

Operating Temp. Range (Case)	0°C to +70°C
Storage Temp. Range (Ambient)	-40°C to +125°C
Power Supply Voltage	±5.25 Vdc
Control Voltage	+5.0 Vdc

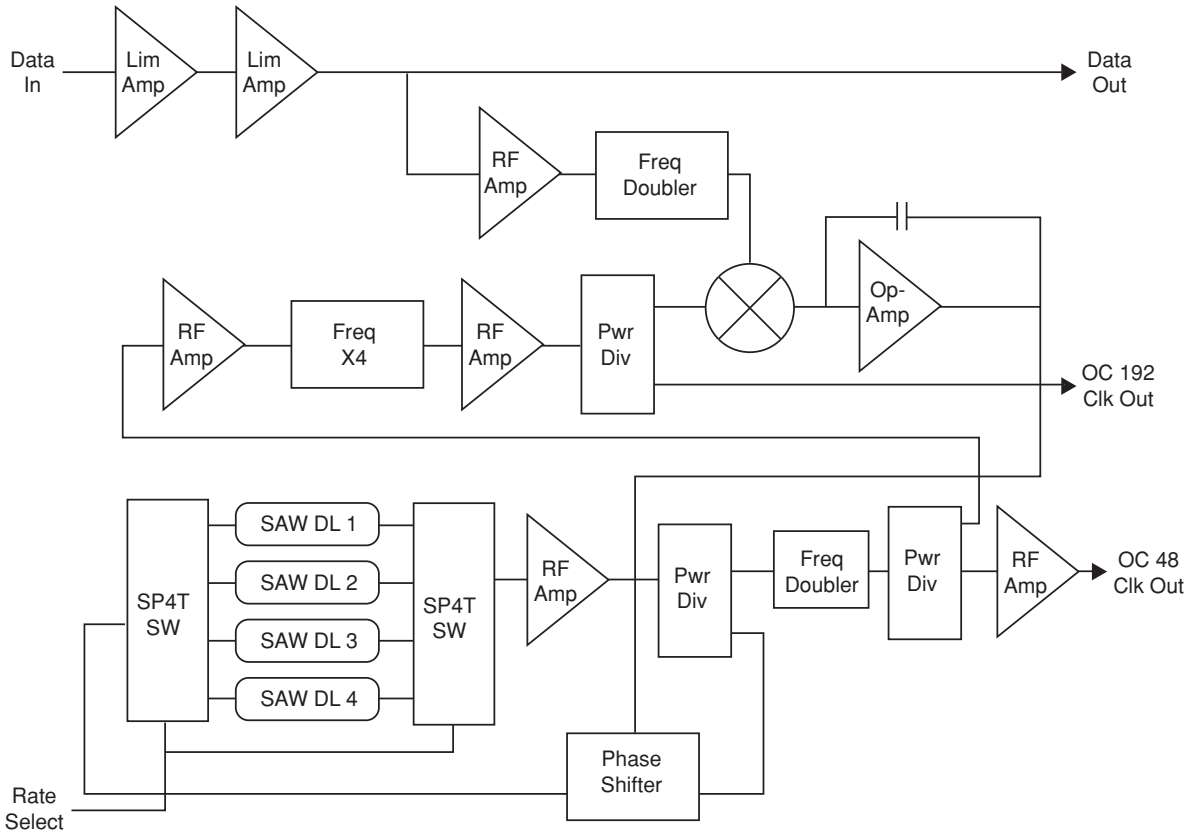
SPECIFICATIONS

Specifications @ Vcc = +5 Volts, Vee = -5 Volts, T_A = +25°C unless otherwise specified

PARAMETER	Min	Max	Units	Conditions
Operating Data Rates	9.953 10.3125 10.664 10.709		Gb/s Gb/s Gb/s Gb/s	
Selectable Operating Data Rates	1	4		Selected by two TTL inputs (00,01,10,11)
Locking Range	-0.3	+0.3	%	Referenced to nominal bit rate.
Data Input Voltage	6	1000	mVp-p	NRZ or RZ
Input Data BER		10^{-12}		
Data Input Return Loss	9		dB	150kHz to 12.5GHz, 10dB typ.
OC-192 Clock Output Frequency	9.953	10.709	GHz	
OC-48 Clock Output Frequency	2.488	2.677	GHz	
Clock Output RMS Jitter		0.02	UI	Wideband measured on oscilloscope. PRBS = 2^{23}-1
Clock Output Peak-to-Peak Jitter		0.12	UI	Wideband measured on oscilloscope. PRBS = 2^{23}-1
Clock Output Voltage	800	1400	mVp-p	
Clock Output Return Loss	10		dB	At output clock frequency ±0.1%
Clock Output Harmonic Level		-30	dBc	
Clock Output Sub-harmonic Level		-40	dBc	
Maximum Number of Bits of Consecutive Ones or Zeros		200	UI	
Data Output Voltage	200	400	mVp-p	Unretimed NRZ or RZ data*
Data Output Return Loss	7		dB	150kHz to 12GHz, 10dB Typ
Jitter Transfer Bandwidth	4		MHz	Set to meet Bellcore jitter transfer requirements while minimizing clock jitter.
Loss of Lock Alarm (unlocked)	2.0	5.0	V	
Loss of Lock Alarm (locked)	0.0	0.8	V	
+5V Power Supply Voltage	4.75	5.25	V	
+5V Power Supply Current		0.70	A	
-5V Power Supply Voltage	-4.75	-5.25	V	
-5V Power Supply Current		0.70	A	
Control Voltage (Low)	0	0.8	V	Standard TTL Levels
Control Voltage (High)	2.4	5.0	V	Standard TTL Levels
Operating Temperature Range	0	+70	°C	(case)
Package Size		3.2 x 1.57 x .625	In	SMA connectors used for Data In, Data Out, OC-192 Clock Out and OC-48 Clock Out

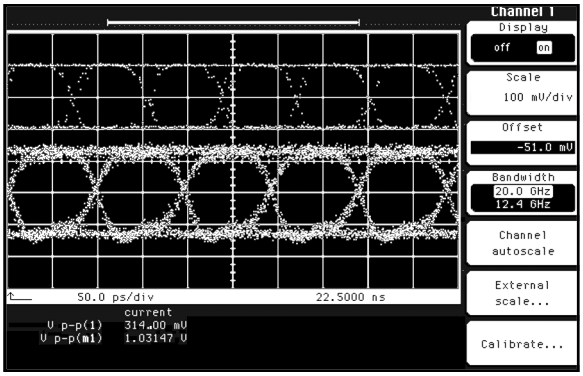
**Higher output level available, contact factory.*

BLOCK DIAGRAM



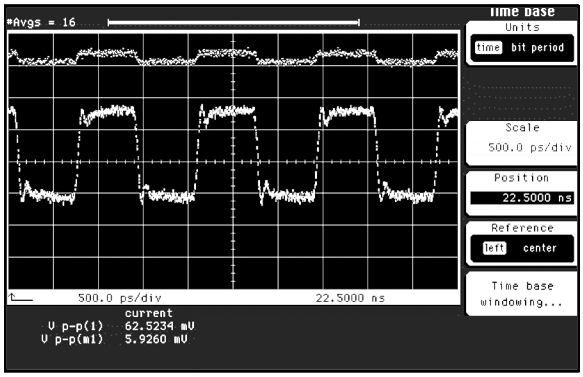
TEST DATA

Single Limiting Amplifier High Level Input Test Data



Conditions: Rate = 12.02Gb/sec, Input Level = 1Vpp

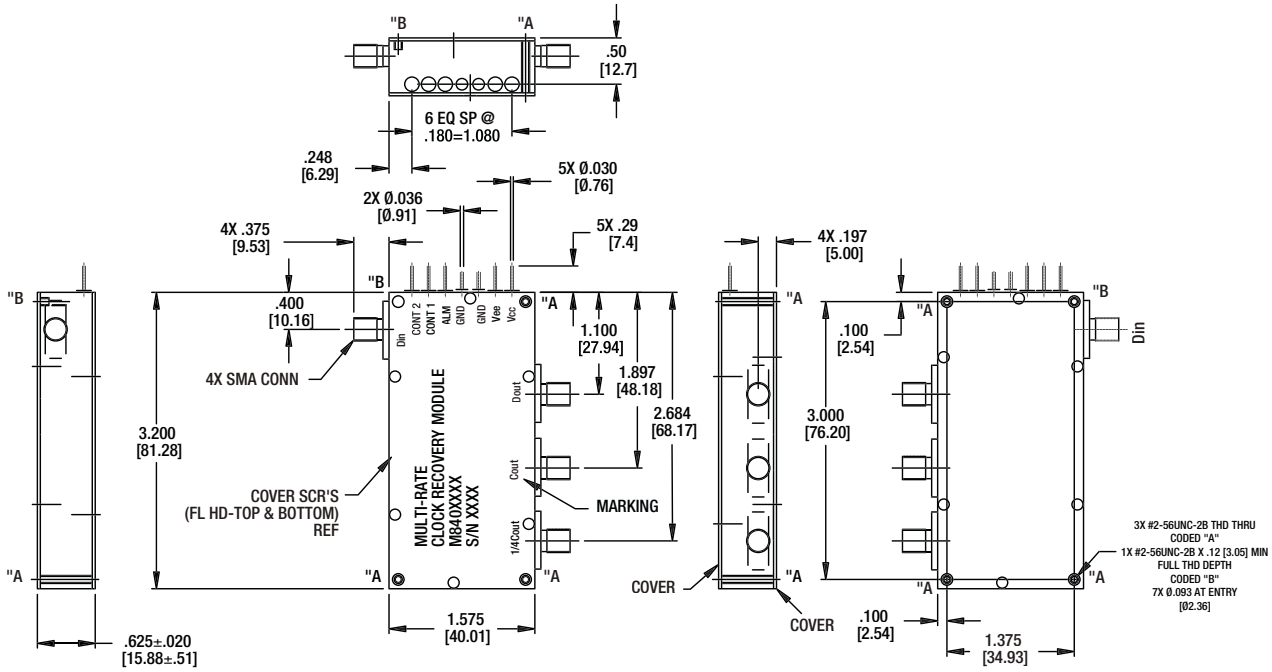
Single Limiting Amplifier Low Level Input Test Data



Conditions: Rate = 12.02Gb/sec, Input Level = 6mVpp

Note: M840 has two limiting amplifiers

MECHANICAL DIMENSIONS & PIN CONFIGURATION



PIN DESIGNATIONS

Symbol	Name	Description
Din	Data Input	AC coupled 50Ω data input
Dout	Data Output	AC coupled 50Ω data output
Cout	OC-192 Clock Output (sinusoidal)	AC coupled 50Ω clock output
1/4 Cout	OC-48 Clock Output (sinusoidal)	AC coupled 50Ω clock output (1/4 freq. of Cout)
Cont1	Frequency Control Line 1	Switch control LSB TTL input signal
Cont2	Frequency Control Line 2	Switch control MSB TTL input signal
ALM	Loss of Lock Alarm	TTL output for PLL lock. "0" is locked; "1" is unlocked
GND	Ground Connection	Pins to connect power and control returns through case
Vee	Negative DC Power Supply	-5VDC Power Supply Input
Vcc	Positive DC Power Supply	+5VDC Power Supply Input

CLOCK FREQUENCY CONTROL MATRIX

	Switch Control	
Clock Frequency	**Cont 2**	**Cont 1**
10.709 GHz	0	0
10.664 GHz	0	1
10.3125 GHz	1	0
9.953 GHz	1	1

ORDERING INFORMATION

Part Number **M844 D XA XB XC XD**

No. of Frequencies (1-4)
Frequency 1
(9.953 GHz)
Frequency 2 (if applicable)
(10.3125 GHz)
Frequency 3 (if applicable)
(10.664 GHz)
Frequency 4 (if applicable)
(10.709 GHz)

VCSO FREQUENCIES AVAILABLE

XA	9.953 GHz
XB	10.3125 GHz
XC	10.664 GHz
XD	10.709 GHz

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