17-STAGE OSCILLATOR/DIVIDER

GENERAL DESCRIPTION

The M58478P is a frequency divider manufactured by aluminum CMOS technology. It produces a frequency of 1/59719 or 1/88672 of the input frequency (3.58MHz to 60Hz or 4.43MHz to 50Hz).

FEATURES

- Makes possible a crystal oscillator circuit
- Capable of handling small-amplitude input signals as low as $0.3V_{PP}$
- Frequency-dividing ratio selected through terminal N
- Reset function
- Produces a shaped-waveform output of the same frequency as the input signal or oscillation output
- Derives a vertical scanning frequency from TV color subcarrier

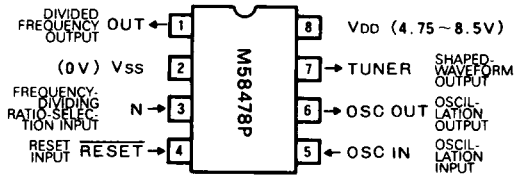
APPLICATIONS

- Frequency divider for VTR

SUMMARY OF FUNCTIONS

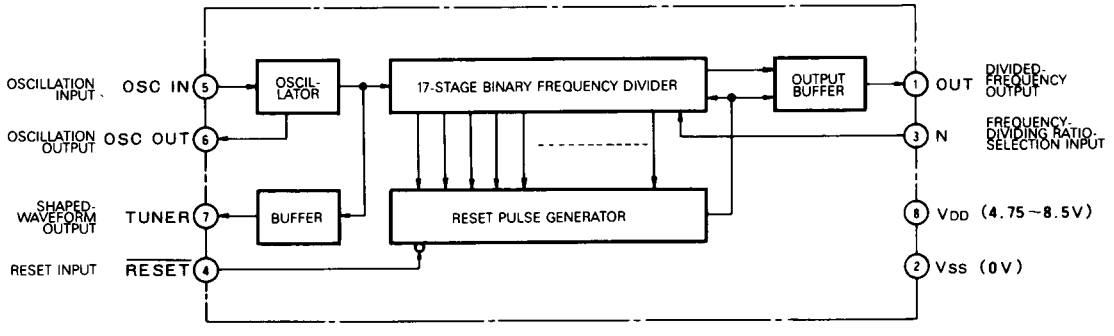
The M58478P has a programmable counter consisting of a 17-stage binary frequency divider, which delivers 60Hz or 50Hz output from an input of 3.58MHz or 4.43MHz, depending on the state of terminal N.

PIN CONFIGURATION (TOP VIEW)



Outline 8P1

BLOCK DIAGRAM



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17-STAGE OSCILLATOR/DIVIDER

FUNCTIONAL DESCRIPTION

Crystal Oscillator

A crystal oscillator is obtained by connecting a quartz resonator element between terminals OSC IN and OSC OUT, and capacitances C_{LI} and C_{LO} between the two terminals and V_{SS}. (A feedback resistor is contained on-chip.) An amplifier is contained in terminal OSC IN, allowing even a small amplitude signal to be input via the coupling capacitor C_C.

Output Frequency

When the input N is open (high), the frequency-dividing ratio is set at 59719, producing a 60Hz output from a 3.58MHz input. When N is low, the ratio is 88672, producing 50Hz from 4.43MHz input. Figure 1 shows the waveform of the divided frequency output.

Shaped-waveform output of the same frequency as the input signal or oscillation frequency is produced on the TUNER output.

Reset Function

When the RESET input is changed from high to low (edge trigger reset of the active low), the output OUT turns low.

Pull-up Resistance

There is a pull-up resistor in both terminals N and $\overline{\text{RESET}}$, eliminating the need for any external resistor. Resistance of the standard pull-up resistor is 20kΩ.

Frequency Dividing Ratio

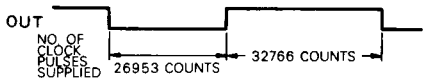
The frequency-dividing ratio is determined by the data contents of the programmable counter.

Change of the Frequency-Dividing Ratio

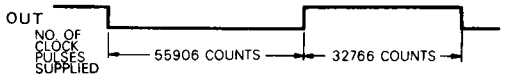
Different frequency-dividing ratios are available. Any frequency-dividing ratio from 5 to 131071 ($=2^{17}-1$) can be provided by changing the data input to the programmable counter.

Fig. 1 Waveform of divided-frequency output

When input N is open (high):



When input N is low:



Note 1 : The frequency-dividing ratio in the following cycle is decided by the state input N just before the output OUT turns from high to low.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3 ~ 9	V
V_I	Input voltage		$V_{SS} \leq V_I \leq V_{DD}$	V
Pd	Maximum power dissipation	Ta = 25°C	250	mW
Topr	Operating free-air temperature range		−30 ~ 70	°C
Tstg	Storage temperature range		−40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −30 ~ 70°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	4.75		8.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	V_{DD}-0.5			V
V_{IL}	Low-level input voltage			0.5	V
V_i	Oscillation input amplitude voltage	0.3			V_{PP}
f	Input frequency, with the terminal N in high-level		3.58	5.5	MHz
	Input frequency, with the terminal N in low-level		4.43	5.5	MHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 6.5V, V_{SS} = 0V, f_{IN} = 4.5MHz, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Operational supply voltage	Ta = −30 ~ 70°C	4.75		8.5	V
I_{DD}	Supply current	N, $\overline{RESET}$ Input/output open			5	mA
V_{IH}	High-level input voltage		V_{DD}-0.5			V
V_{IL}	Low-level input voltage				0.5	V
V_{OH}	High-level output voltage		V_{DD}-0.5			V
V_{OL}	Low-level output voltage				0.5	V
I_{OH}	High-level output current	$V_O = V_{SS}$	−2			mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	2			mA
R_I	Pull-up resistance, N and $\overline{RESET}$ inputs			20		kΩ
v_i	Oscillation input amplitude voltage	V_{DD} = 4.75V	0.3			Vpp
f_{MAX}	Maximum operating frequency	V_{DD} = 4.75V	5.5			MHz

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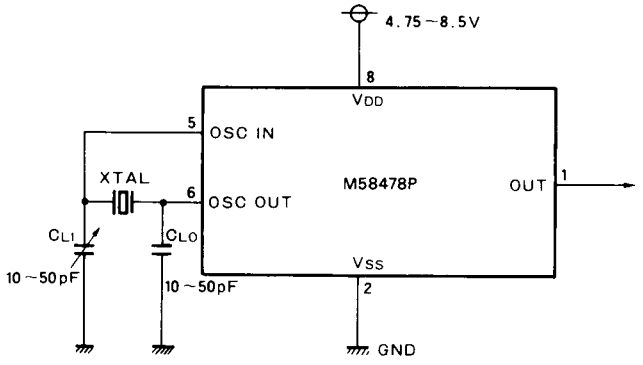
17-STAGE OSCILLATOR/DIVIDER

TYPICAL APPLICATION CIRCUIT

Crystal Oscillator (with Built-In Feedback Resistance)



External Input Signal Connections