Am49PDL640AG

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **30049** Revision **A** Amendment **+5** Issue Date **November 20, 2003**

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PRELIMINARY

Am49PDL640AG

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM

64 Megabit (4 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory and 16 Mbit (1 M x 16-Bit) Pseudo Static RAM

DISTINCTIVE CHARACTERISTICS

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - Access time as fast as 70 ns initial/ 25 ns subsequent
- **Package**
  - 73-Ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **Simultaneous Read/Write operations**
  - Data can be continuously read from one bank while executing erase/program functions in another bank.
  - Zero latency between read and write operations
- **Flex Bank™ architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A: 8 Mbit (4 Kw x 8 and 32Kw x 15)
  - Bank B: 24 Mbit (32 Kw x 48)
  - Bank C: 24 Mbit (32 Kw x 48)
  - Bank D: 8 Mbit (4 Kw x 8 and 32 Kw x 15)
- **Manufactured on 0.17 µm process technology**
- **SecSi™ (Secured Silicon) Sector: Extra 256 Byte sector**
  - *Factory locked and identifiable:* 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function. ExpressFlash option allows entire sector to be available for factory-secured data
  - *Customer lockable:* Sector is one-time programmable. Once sector is locked, data cannot be changed.
- **Zero Power Operation**
  - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- **Boot sectors**
  - Top and bottom boot sectors in the same device
- **Compatible with JEDEC standards**
  - Pinout and software compatible with single-power-supply flash standard

PERFORMANCE CHARACTERISTICS

- **High performance**
  - Access time as fast as 70 ns
  - Program time: 4 µs/word typical utilizing Accelerate function
- **Ultra low power consumption (typical values)**
  - 23 mA active read current
  - 15 mA program/erase current
  - 200 nA in standby or automatic sleep mode
- **Minimum 1 million write cycles guaranteed per sector**
- **20 year data retention at 125°C**
  - Reliable operation for the life of the system

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) complaint**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Any combination of sectors can be erased**
- **Ready/Busy# output (RY/BY#)**
  - Hardware method for detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method of resetting the internal state machine to the read mode
- **WP#/ACC input pin**
  - Write protect (WP#) function protects sectors 0, 1, 140, and 141, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password

Pseudo SRAM Features

- **Power dissipation**
  - Operating: 30 mA maximum
  - Standby: 100 µA maximum
  - Deep Power-down current: 10 µA
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 2.7 to 3.1 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**
- **Multiple pSRAM vendors available**

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GENERAL DESCRIPTION

Am29PDL640G Features

The Am29PDL640G is a 64 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 4 Mwords. The device is offered in 73-ball Fine-pitch BGA packages. The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 25, 30, and 45 ns, with corresponding random access times of 65, 70, 85, and 90 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Bank	Sectors
A	8 Mbit (4 Kw x 8 and 32 Kw x 15)
B	24 Mbit (32 Kw x 48)
C	24 Mbit (32 Kw x 48)
D	8 Mbit (4 Kw x 8 and 32 Kw x 15)

Page Mode Features

The device is AC timing, input/output, and package **compatible with 4 Mbit x16 page mode mask ROM**. The page size is 8 words.

After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.1 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

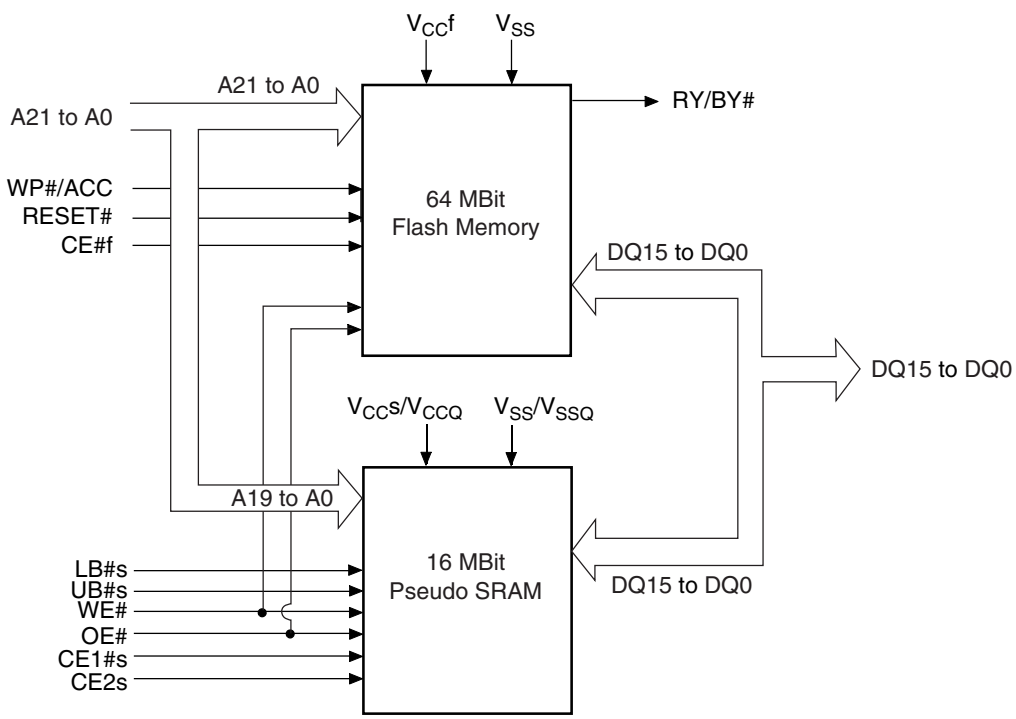
AMD's Flash technology combined years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

TABLE OF CONTENTS

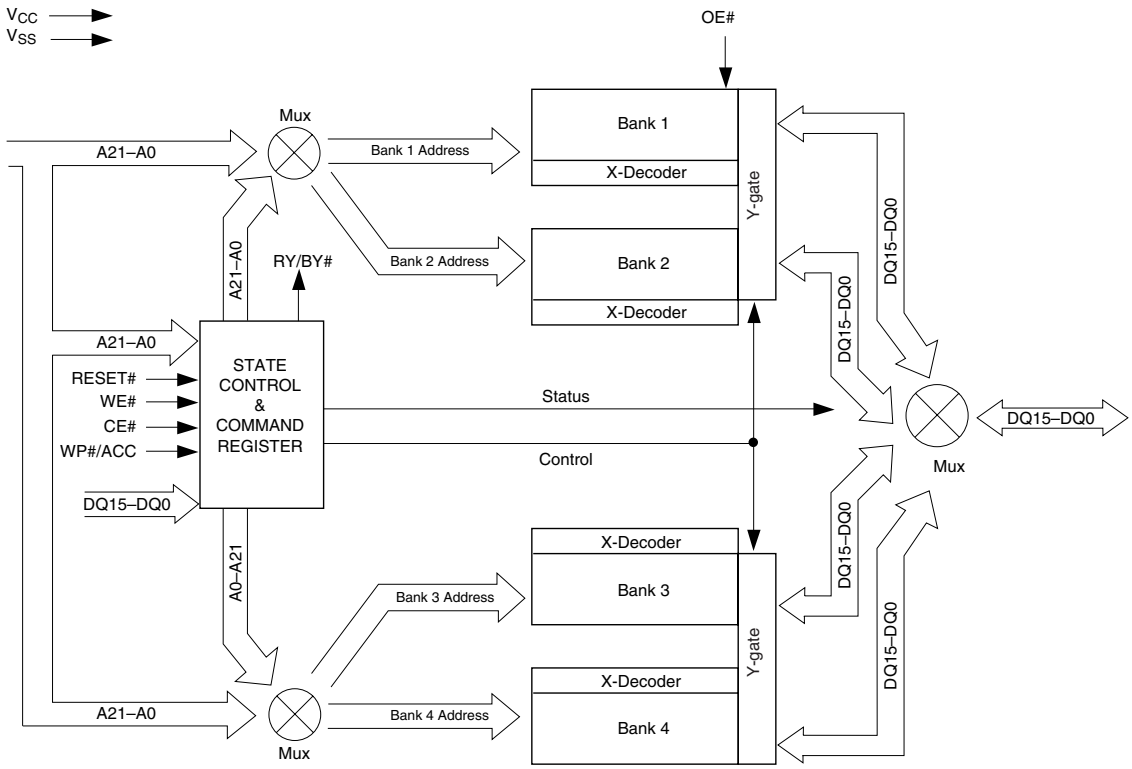
PRODUCT SELECTOR GUIDE

Part Number		Am49PDL640AG			
Speed Options	Standard Voltage Range: V_{CC} = 2.7–3.1 V	Flash Memory		Pseudo SRAM	
		70	85	70	85
Max Access Time (ns) t_{ACC}		70	85	70	85
Max Page Access (ns) t_{PACC}		25	30	N/A	N/A
CE#f Access (ns) t_{CE}		70	85	70	85
OE# Access (ns) t_{OE}		25	30	35	40

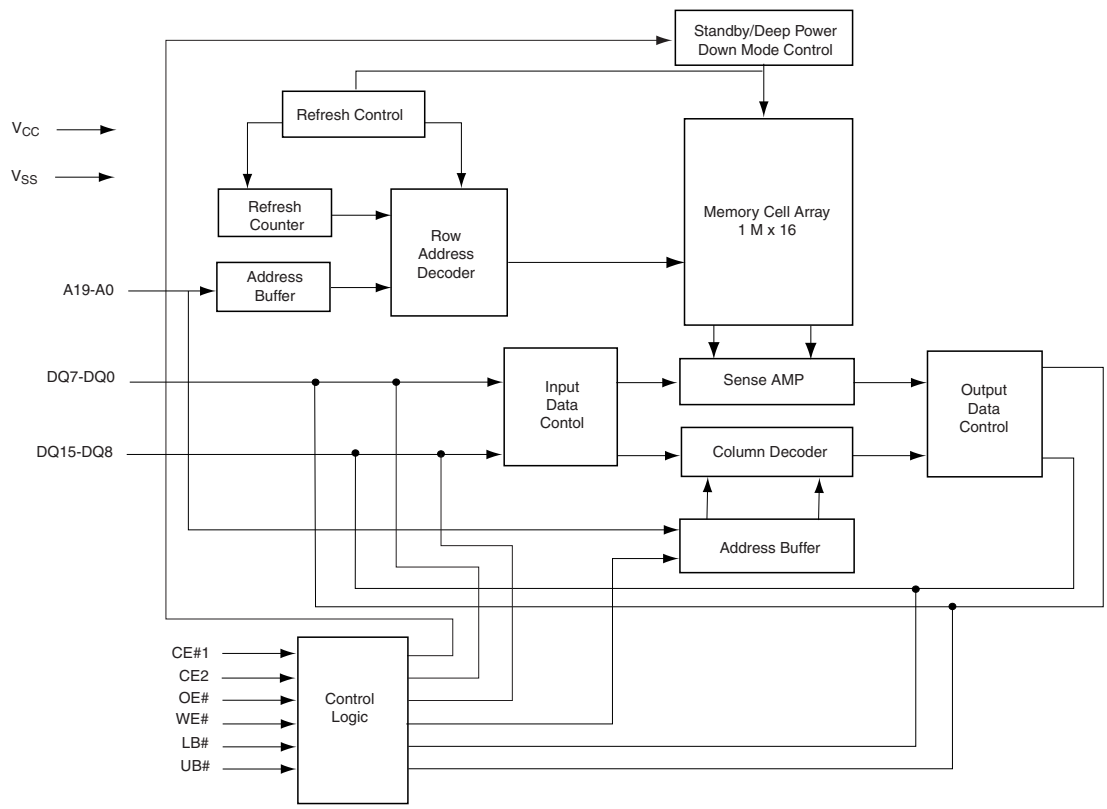
MCP BLOCK DIAGRAM



FLASH MEMORY BLOCK DIAGRAM

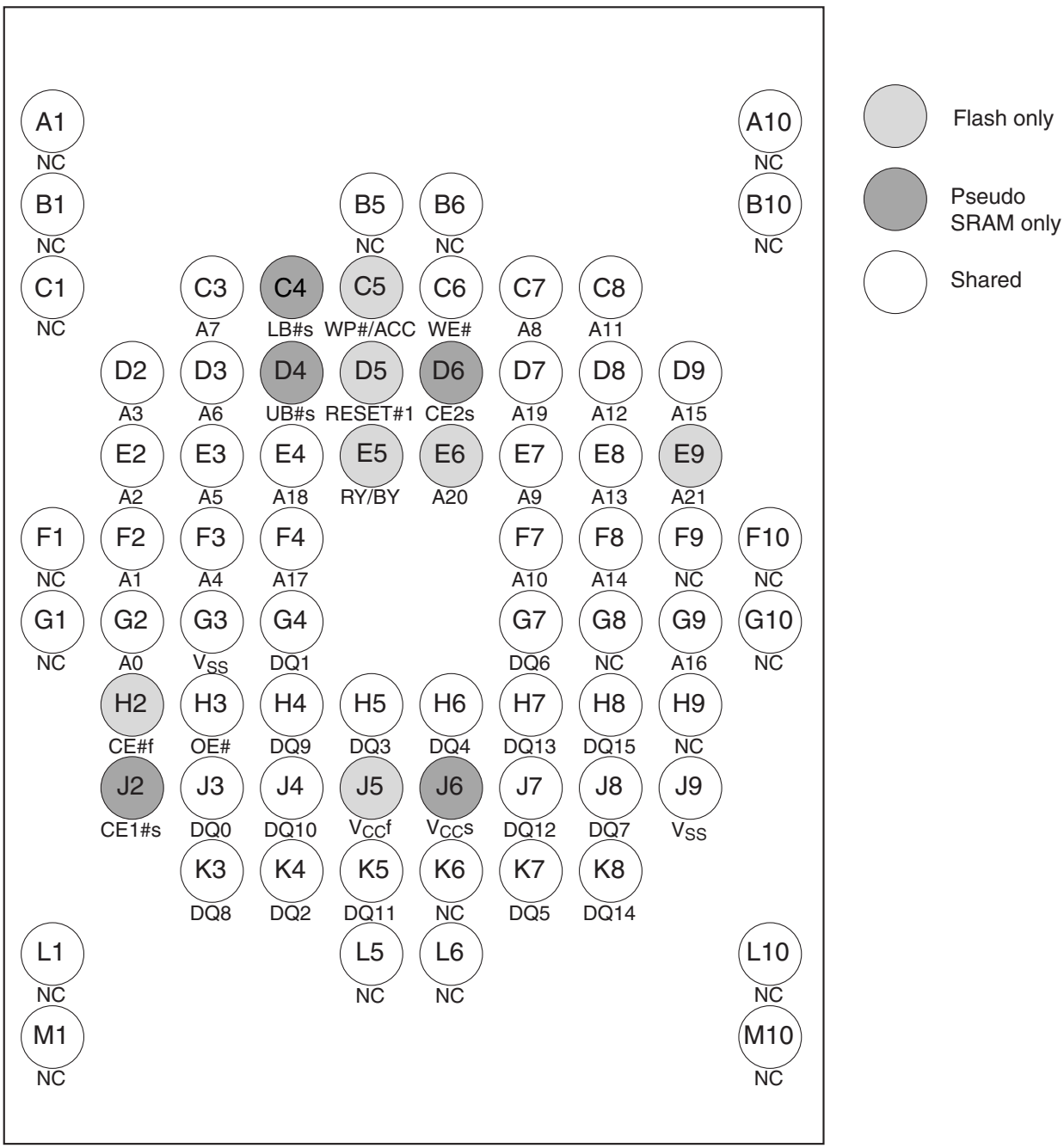


PSRAM BLOCK DIAGRAM



CONNECTION DIAGRAM

73-Ball FBGA
Top View



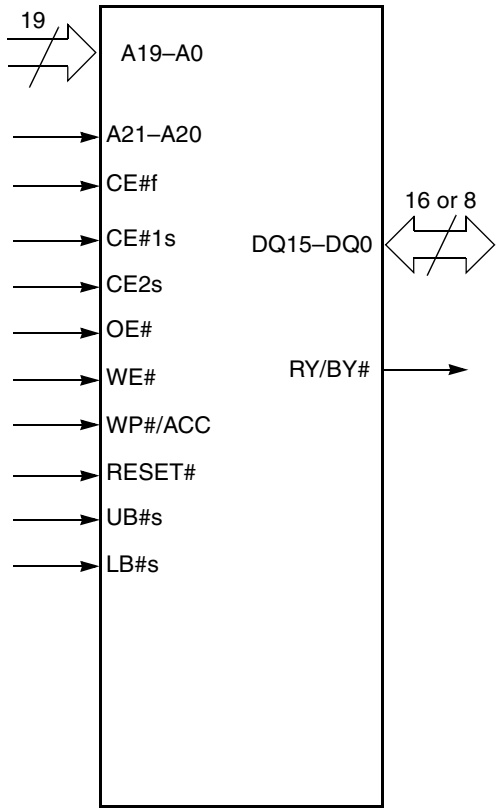
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A19–A0	=	20 Address Inputs (Common)
A21–A20	=	2 Address Inputs (Flash)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE#f	=	Chip Enable (Flash)
CE#1s	=	Chip Enable 1 (pSRAM)
CE2s	=	Chip Enable 2 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output
UB#s	=	Upper Byte Control (pSRAM)
LB#s	=	Lower Byte Control (pSRAM)
RESET#	=	Hardware Reset Pin, Active Low
WP#/ACC	=	Hardware Write Protect/ Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}s$	=	pSRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:

Am49PDL640 A G a 70 N T

TAPE AND REEL
T = 7 inches
S = 13 inches

TEMPERATURE RANGE
N = Light Industrial (–25°C to +85°C)

SPEED OPTION
See Product Selector Guide and Valid Combinations

pSRAM VENDOR
Blank = Etron
a = Si-7

PROCESS TECHNOLOGY
G = 0.17 µm

Pseudo SRAM DEVICE DENSITY
A = 16 Mbits

AMD DEVICE NUMBER/DESCRIPTION

Am49PDL640AG
Stacked Multi-Chip Package (MCP) Flash Memory and SRAM
Am29PDL640G 64 Megabit (4 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory and 16 Mbit (1 M x 16-Bit) Pseudo Static RAM

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations		
Order Number		**Package Marking**
Am49PDL640AG70N	T, S	M49000001Y
Am49PDL640AG85N		M49000001Z
Am49PDL640AGa70N		M49000004F
Am29PDL640AGa85N		M49000004G

MCP DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Tables 1-2 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations—Flash Word Mode, CIOf = V_{IH}

Operation (Notes 1, 2)		CE#f	CE1#s	CE2s	OE#	WE#	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Active Flash	(Note 7)	L	H	H	L	H	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
	(Note 8)		H	L									
Write to Active Flash	(Note 7)	L	H	H	H	L	A_{IN}	X	X	H	(Note 5)	D_{IN}	D_{IN}
	(Note 8)		H	L									
Standby		$V_{CC} \pm 0.3$ V	H	H	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
Deep Power-down Standby (Note 10)		$V_{CC} \pm 0.3$ V	H	L	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
Output Disable (Note 9)		L	L	H	H	H	X	X	X	H	L/H	High-Z	High-Z
					H	H	X	X	X				
Flash Hardware Reset	(Note 7)	X	H	H	X	X	X	X	X	L	L/H	High-Z	High-Z
	(Note 8)		H	L									
Sector Protect (Notes 5, 9)	(Note 7)	L	H	H	H	L	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
	(Note 8)		H	L									
Sector Unprotect (Notes 5, 9)	(Note 7)	L	H	H	H	L	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
	(Note 8)		H	L									
Temporary Sector Unprotect	(Note 7)	X	H	H	X	X	X	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
	(Note 8)		H	L									
Read from pSRAM		H	L	H	L	H	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
								H	L			High-Z	D_{OUT}
								L	H			D_{OUT}	High-Z
Write to pSRAM		H	L	H	X	L	A_{IN}	L	L	H	X	D_{IN}	D_{IN}
								H	L			High-Z	D_{IN}
								L	H			D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f1 = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*
7. *Data will be retained in pSRAM.*
8. *Data will be lost in pSRAM.*
9. *CE# inputs on both flash devices may be held low for this operation*
10. *Deep Power-down Standby is not available.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the AC Read-Only Operations table for timing specifications and to Figure 14 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words, with the appropriate page being selected by the higher address bits A21–A3 and the LSB bits A2–A0 determining the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping A21–A3 constant and changing A2 to A0 to select the specific word within that page.

Table 2. Page Select

Word	A2	A1	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Simultaneous Operation

The device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation), in addition to the conventional features (read, program, erase-suspend read, and erase-suspend program). The bank selected can be selected by bank addresses (A21–A19) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 3. Bank Select

Bank	A21–A19
Bank A	000
Bank B	001, 010, 011
Bank C	100, 101, 110
Bank D	111

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” refers to the address bits

required to uniquely select a sector. The “Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The Flash AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on* WP#/ACC *for operations other than accelerated programming, or device damage may result. In addition, the* WP#/ACC *pin should be raised to V_{CC} when not in use. That is, the* WP#/ACC *pin should not be left floating or unconnected; inconsistent behavior of the device may result*.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3 in the table represents the CMOS standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. ICC5 in the table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (ICC4). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the high impedance state.

Table 4. Am29PDL640G Sector Architecture

Bank	Sector	Sector Address A21–A12	Sector Size (Kwords)	Address Range
Bank A	SA0	0000000000	4	00000h–00FFFh
	SA1	0000000001	4	01000h–01FFFh
	SA2	0000000010	4	02000h–02FFFh
	SA3	0000000011	4	03000h–03FFFh
	SA4	0000000100	4	04000h–04FFFh
	SA5	0000000101	4	05000h–05FFFh
	SA6	0000000110	4	06000h–06FFFh
	SA7	0000000111	4	07000h–07FFFh
	SA8	0000001xxx	32	08000h–0FFFFh
	SA9	0000010xxx	32	10000h–17FFFh
	SA10	0000011xxx	32	18000h–1FFFFh
	SA11	0000100xxx	32	20000h–27FFFh
	SA12	0000101xxx	32	28000h–2FFFFh
	SA13	0000110xxx	32	30000h–37FFFh
	SA14	0000111xxx	32	38000h–3FFFFh
	SA15	0001000xxx	32	40000h–47FFFh
	SA16	0001001xxx	32	48000h–4FFFFh
	SA17	0001010xxx	32	50000h–57FFFh
	SA18	0001011xxx	32	58000h–5FFFFh
	SA19	0001100xxx	32	60000h–67FFFh
	SA20	0001101xxx	32	68000h–6FFFFh
	SA21	0001101xxx	32	70000h–77FFFh
	SA22	0001111xxx	32	78000h–7FFFFh

Table 4. Am29PDL640G Sector Architecture

Bank	Sector	Sector Address A21–A12	Sector Size (Kwords)	Address Range
Bank B	SA23	0010000xxx	32	80000h–87FFFh
	SA24	0010001xxx	32	88000h–8FFFFh
	SA25	0010010xxx	32	90000h–97FFFh
	SA26	0010011xxx	32	98000h–9FFFFh
	SA27	0010100xxx	32	A0000h–A7FFFh
	SA28	0010101xxx	32	A8000h–AFFFFh
	SA29	0010110xxx	32	B0000h–B7FFFh
	SA30	0010111xxx	32	B8000h–BFFFFh
	SA31	0011000xxx	32	C0000h–C7FFFh
	SA32	0011001xxx	32	C8000h–CFFFFh
	SA33	0011010xxx	32	D0000h–D7FFFh
	SA34	0011011xxx	32	D8000h–DFFFFh
	SA35	0011000xxx	32	E0000h–E7FFFh
	SA36	0011101xxx	32	E8000h–EFFFFh
	SA37	0011110xxx	32	F0000h–F7FFFh
	SA38	0011111xxx	32	F8000h–FFFFFh
	SA39	0100000xxx	32	F9000h–107FFFh
	SA40	0100001xxx	32	108000h–10FFFFh
	SA41	0100010xxx	32	110000h–117FFFh
	SA42	0101011xxx	32	118000h–11FFFFh
	SA43	0100100xxx	32	120000h–127FFFh
	SA44	0100101xxx	32	128000h–12FFFFh
	SA45	0100110xxx	32	130000h–137FFFh
	SA46	0100111xxx	32	138000h–13FFFFh
	SA47	0101000xxx	32	140000h–147FFFh
	SA48	0101001xxx	32	148000h–14FFFFh
	SA49	0101010xxx	32	150000h–157FFFh
	SA50	0101011xxx	32	158000h–15FFFFh
	SA51	0101100xxx	32	160000h–167FFFh
	SA52	0101101xxx	32	168000h–16FFFFh
	SA53	0101110xxx	32	170000h–177FFFh
	SA54	0101111xxx	32	178000h–17FFFFh
	SA55	0110000xxx	32	180000h–187FFFh
	SA56	0110001xxx	32	188000h–18FFFFh
	SA57	0110010xxx	32	190000h–197FFFh
	SA58	0110011xxx	32	198000h–19FFFFh
	SA59	0100100xxx	32	1A0000h–1A7FFFh
	SA60	0110101xxx	32	1A8000h–1AFFFFh
	SA61	0110110xxx	32	1B0000h–1B7FFFh
	SA62	0110111xxx	32	1B8000h–1BFFFFh
	SA63	0111000xxx	32	1C0000h–1C7FFFh
	SA64	0111001xxx	32	1C8000h–1CFFFFh
	SA65	0111010xxx	32	1D0000h–1D7FFFh
	SA66	0111011xxx	32	1D8000h–1DFFFFh
	SA67	0111100xxx	32	1E0000h–1E7FFFh
	SA68	0111101xxx	32	1E8000h–1EFFFFh
	SA69	0111110xxx	32	1F0000h–1F7FFFh
	SA70	0111111xxx	32	1F8000h–1FFFFFh

Table 4. Am29PDL640G Sector Architecture

Bank	Sector	Sector Address A21–A12	Sector Size (Kwords)	Address Range
Bank C	SA71	1000000xxx	32	200000h–207FFFh
	SA72	1000001xxx	32	208000h–20FFFFh
	SA73	1000010xxx	32	210000h–217FFFh
	SA74	1000011xxx	32	218000h–21FFFFh
	SA75	1000100xxx	32	220000h–227FFFh
	SA76	1000101xxx	32	228000h–22FFFFh
	SA77	1000110xxx	32	230000h–237FFFh
	SA78	1000111xxx	32	238000h–23FFFFh
	SA79	1001000xxx	32	240000h–247FFFh
	SA80	1001001xxx	32	248000h–24FFFFh
	SA81	1001010xxx	32	250000h–257FFFh
	SA82	1001011xxx	32	258000h–25FFFFh
	SA83	1001100xxx	32	260000h–267FFFh
	SA84	1001101xxx	32	268000h–26FFFFh
	SA85	1001110xxx	32	270000h–277FFFh
	SA86	1001111xxx	32	278000h–27FFFFh
	SA87	1010000xxx	32	280000h–28FFFFh
	SA88	1010001xxx	32	288000h–28FFFFh
	SA89	1010010xxx	32	290000h–297FFFh
	SA90	1010011xxx	32	298000h–29FFFFh
	SA91	1010100xxx	32	2A0000h–2A7FFFh
	SA92	1010101xxx	32	2A8000h–2AFFFFh
	SA93	1010110xxx	32	2B0000h–2B7FFFh
	SA94	1010111xxx	32	2B8000h–2BFFFFh
	SA95	1011000xxx	32	2C0000h–2C7FFFh
	SA96	1011001xxx	32	2C8000h–2CFFFFh
	SA97	1011010xxx	32	2D0000h–2D7FFFh
	SA98	1011011xxx	32	2D8000h–2DFFFFh
	SA99	1011100xxx	32	2E0000h–2E7FFFh
	SA100	1011101xxx	32	2E8000h–2EFFFFh
	SA101	1011110xxx	32	2F0000h–2FFFFFh
	SA102	1011111xxx	32	2F8000h–2FFFFFh
	SA103	1100000xxx	32	300000h–307FFFh
	SA104	1100001xxx	32	308000h–30FFFFh
	SA105	1100010xxx	32	310000h–317FFFh
	SA106	1100011xxx	32	318000h–31FFFFh
	SA107	1100100xxx	32	320000h–327FFFh
	SA108	1100101xxx	32	328000h–32FFFFh
	SA109	1100110xxx	32	330000h–337FFFh
	SA110	1100111xxx	32	338000h–33FFFFh

Table 4. Am29PDL640G Sector Architecture

Bank	Sector	Sector Address A21–A12	Sector Size (Kwords)	Address Range
Bank D	SA119	1110000xxx	32	380000h–387FFFh
	SA120	1110001xxx	32	388000h–38FFFFh
	SA121	1110010xxx	32	390000h–397FFFh
	SA122	1110011xxx	32	398000h–39FFFFh
	SA123	1110100xxx	32	3A0000h–3A7FFFh
	SA124	1110101xxx	32	3A8000h–3AFFFFh
	SA125	1110110xxx	32	3B0000h–3B7FFFh
	SA126	1110111xxx	32	3B8000h–3BFFFFh
	SA127	1111000xxx	32	3C0000h–3C7FFFh
	SA128	1111001xxx	32	3C8000h–3CFFFFh
	SA129	1111010xxx	32	3D0000h–3D7FFFh
	SA130	1111011xxx	32	3D8000h–3DFFFFh
	SA131	1111100xxx	32	3E0000h–3E7FFFh
	SA132	1111101xxx	32	3E8000h–3EFFFFh
	SA133	1111110xxx	32	3F0000h–3F7FFFh
	SA134	1111111000	4	3F8000h–3F8FFFh
	SA135	1111111001	4	3F9000h–3F9FFFh
	SA136	1111111010	4	3FA000h–3FAFFFh
	SA137	1111111011	4	3FB000h–3FBFFFh
	SA138	1111111100	4	3FC000h–3FCFFFh
	SA139	1111111101	4	3FD000h–3FDFFFh
	SA140	1111111110	4	3FE000h–3FEFFFh
	SA141	1111111111	4	3FF000h–3FFFFFh

Table 5. Bank Address

Bank	A21–A19
A	000
B	001, 010, 011
C	100, 101, 110
D	111

Table 6. SecSi™ Sector Secure Sector **Addresses**

Device	Sector Size	Address Range
Am29PDL640G	128 words	00000h–0007Fh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 7. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 4). Table 7 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 14. *Note that if a Bank Address (BA) on address bits A21, A20, and A19 is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 14. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 7. Am29PDL640G Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	4 Kwords
SA1	0000000001	4 Kwords
SA2	0000000010	4 Kwords
SA3	0000000011	4 Kwords
SA4	0000000100	4 Kwords
SA5	0000000101	4 Kwords
SA6	0000000110	4 Kwords
SA7	0000000111	4 Kwords
SA8–SA10	0000001XXX, 0000010XXX, 0000011XXX	96 (3x32) Kwords
SA11–SA14	00001XXXXX	128 (4x32) Kwords
SA15–SA18	00010XXXXX	128 (4x32) Kwords
SA19–SA22	00011XXXXX	128 (4x32) Kwords
SA23–SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51-SA54	01011XXXXX	128 (4x32) Kwords
SA55–SA58	01100XXXXX	128 (4x32) Kwords
SA59–SA62	01101XXXXX	128 (4x32) Kwords
SA63–SA66	01110XXXXX	128 (4x32) Kwords
SA67–SA70	01111XXXXX	128 (4x32) Kwords
SA71–SA74	10000XXXXX	128 (4x32) Kwords
SA75–SA78	10001XXXXX	128 (4x32) Kwords
SA79–SA82	10010XXXXX	128 (4x32) Kwords
SA83–SA86	10011XXXXX	128 (4x32) Kwords
SA87–SA90	10100XXXXX	128 (4x32) Kwords
SA91–SA94	10101XXXXX	128 (4x32) Kwords
SA95–SA98	10110XXXXX	128 (4x32) Kwords
SA99–SA102	10111XXXXX	128 (4x32) Kwords
SA103–SA106	11000XXXXX	128 (4x32) Kwords
SA107–SA110	11001XXXXX	128 (4x32) Kwords
SA111–SA114	11010XXXXX	128 (4x32) Kwords
SA115–SA118	11011XXXXX	128 (4x32) Kwords
SA119–SA122	11100XXXXX	128 (4x32) Kwords
SA123–SA126	11101XXXXX	128 (4x32) Kwords
SA127–SA130	11110XXXXX	128 (4x32) Kwords
SA131–SA133	1111100XXX, 1111101XXX, 1111110XXX	96 (3x32) Kwords
SA134	1111111000	4 Kwords
SA135	1111111001	4 Kwords
SA136	1111111010	4 Kwords
SA137	1111111011	4 Kwords
SA138	1111111100	4 Kwords
SA139	1111111101	4 Kwords
SA140	1111111101	4 Kwords
SA141	1111111111	4 Kwords

SECTOR PROTECTION

The Am29PDL640G features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors 0, 1, 140, and 141.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the Persistent Sector Protection method is desired, programming the **Persistent Sector Protection Mode Locking Bit** permanently sets the device to the Persistent Sector Protection mode. If the Password Sector Protection method is desired, programming the **Password Mode Locking Bit** permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set. **One of the two modes must be selected when the device is first programmed.** This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at the factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous AMD flash devices. This new method provides three different sector protection states:

- **Persistently Locked**—The sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command.
- **Unlocked**—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of "bits" are used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Write Command**.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. **The flash device does not have a built-in means of preventing sector PPBs over-erasure**.

Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to

switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors 0, 1, 140, and 141. When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = V_{IL}.

Table 8. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

Table 9 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **one-time programmable (OTP)** region of the flash memory. Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. Disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting sectors 0, 1, 140, and 141 without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed High Voltage Sector Protection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether sectors 0, 1, 140, and 141 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in High Voltage Sector Protection.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

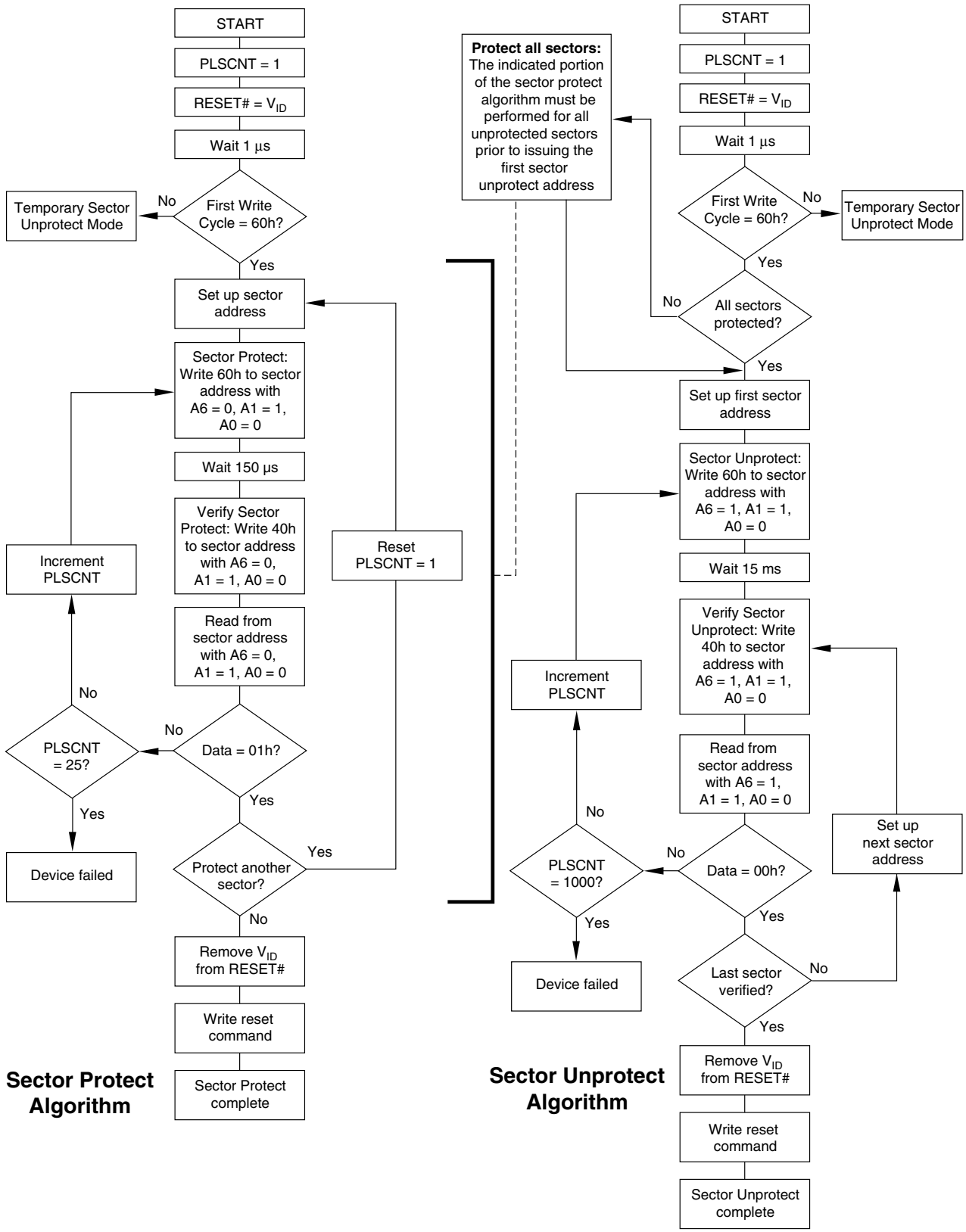
Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure Note: for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

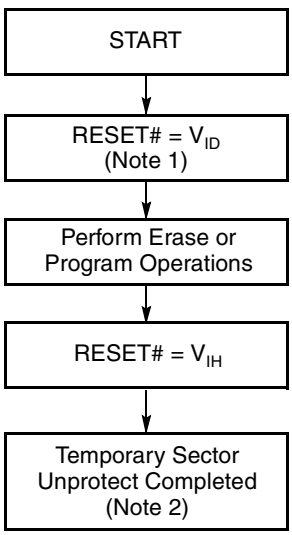


Note: *These algorithms are valid only in Persistent Sector Protection Mode. They are not valid in Password Protection Mode.*

Figure 1. In-System Sector Protection/ Sector Unprotection Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected (If* WP#/ACC *= V_{IL}, sectors 0, 1, 140, 141 will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

SecSi™ (Secured Silicon) Sector SectorFlash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is up to 128 words in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize the sector in any manner they choose. The customer-lockable version has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi™ Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In a factory locked device, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The SecSi Sector is located at addresses 000000h–00007Fh in Persistent Protection mode, and at addresses 000005h–00007Fh in Password Protection mode. The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through the ExpressFlash service
- Both a random, secure ESN and customer code through the ExpressFlash service.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. AMD programs the customer's code, with or without the random ESN. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

If the security feature is not required, the SecSi SectorSecure Sector can be treated as an additional Flash memory space. The SecSi Sector can be read any

number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure Note:, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

SecSi Sector Protection Bit

The SecSi Sector Protection Bit prevents programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

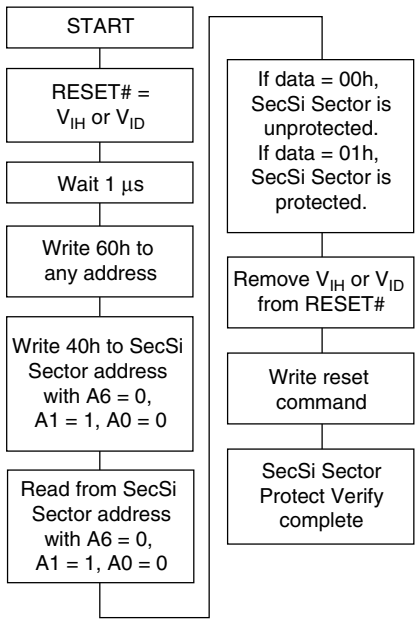


Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 10–13. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 10–13. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 9. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0031h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses	Data	Description
27h	0017h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	007Dh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 12. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	0004h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	0077h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0017h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0030h	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0030h	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0017h	Bank 4 Region Information X = Number of Sectors in Bank 4

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 14 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to return the device to reading array data.*

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

See also Requirements for Reading Array Data in the section for more information. The Read-Only Operations table provides the read parameters, and Figure 14 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 14 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 4 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 14 shows the address and data requirements for both command sequences. See also "SecSi™ (Secured Silicon) Sector SectorFlash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 14 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

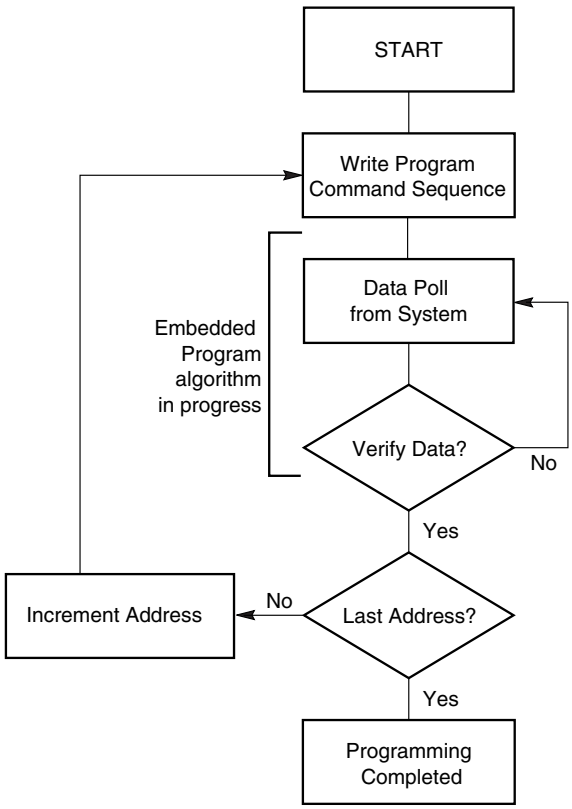
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 14 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/ACC *pin must not be at* V_{HH} *any operation other than accelerated programming, or device damage may result. In addition, the* WP#/ACC *pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 4 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 for timing diagrams.



Note: *See Table 14 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 14 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command.Table 14 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 80 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 80 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read

data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

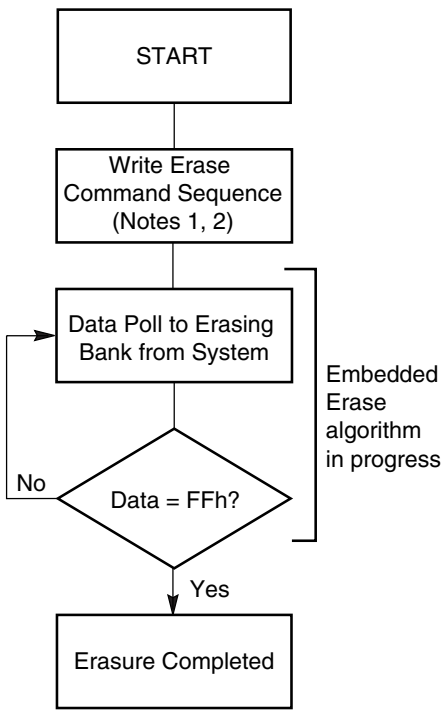
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don’t care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 14 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Four Password Program commands are required to program the password. The system must enter the unlock cycle, password program command (38h) and the program address/data for each portion

of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all ones when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

The Password Verify command is permitted if the SecSi sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1-A0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. *If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin.* By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. *If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin.* Exiting the V_{CC}-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command (only in the Persistent Protection Mode).

DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits (A21–A12) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset.Exiting the DYB Write command is accomplished by writing the Read/Reset command.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

Once the Password Unlock command is entered, the RY/BY# indicates that the device is busy. Approximately 2 µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/BY# is not low or DQ6 does not toggle when read), the Password Unlock command and next part of the password are written. The system must thus monitor RY/BY# or the status bits to confirm when to write the next portion of the password.

Note that immediately following successful unlock, write the SecSi Sector exit command before attempting to verify, program, or erase the PPBs.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A21–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

DYB Write Command

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

PPB Lock Bit Set Command

The PPB Lock Bit set command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

Note that immediately following the PPB Lock Status Command write the SecSi Sector Exit command before attempting to verify, program, or erase the PPBs.

Sector Protection Status Command

The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

Command Definitions Tables

Table 13. Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA)X00	01				
	Device ID (10)	6	555	AA	2AA	55	(BA) 555	90	(BA)X01	7E	(BA)X0E	15	(BA)X0F	01
	SecSi Sector Factory Protect (8)	4	555	AA	2AA	55	(BA) 555	90	X03	(see note 8)				
	Sector Group Protect Verify (9)	4	555	AA	2AA	55	(BA) 555	90	(SA)X02	XX00/ XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (11)		1	BA	B0										
Program/Erase Resume (12)		1	BA	30										
CFI Query (13)		1	55	98										
Accelerated Program (14)		2	XX	A0	PA	PD								
Unlock Bypass Entry (15)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (15)		2	XX	A0	PA	PD								
Unlock Bypass Erase (15)		2	XX	80	XX	10								
Unlock Bypass CFI (13, 15)		1	XX	98										
Unlock Bypass Reset (15)		2	XX	90	XX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by A21:A19, see Tables 4 and 5 for more detail.

PA = Program Address (A21:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (A21:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A21:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.*
8. *The data is 80h for factory locked and 00h for not factory locked.*
9. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Device ID must be read across cycles 4, 5, and 6.*
11. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
12. *Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *WP#/ACC must be at V_{ID} during the entire operation of command.*
15. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.*

Table 14. Sector Protection Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)											
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
SecSi Sector Entry	3	555	AA	2AA	55	555	88						
SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00				
SecSi Protection Bit Program (5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)
SecSi Protection Bit Status	4	555	AA	2AA	55	555	60	OW	RD(0)				
Password Program (5, 7, 8)	4	555	AA	2AA	55	555	38	XX[0-3]	PD[0-3]				
Password Verify (8, 9)	4	555	AA	2AA	55	555	C8	PWA[0-3]	PWD[0-3]				
Password Unlock (7, 10, 11, 17)	4	555	AA	2AA	55	555	28	PWA[0-3]	PWD[0-3]				
PPB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)
All PPB Erase (5, 13, 14)	6	555	AA	2AA	55	555	60	EP	60	(SA)EP	40	(SA)WP	RD(0)
PPB Lock Bit Set	3	555	AA	2AA	55	555	78						
PPB Lock Bit Status (15, 18)	4	555	AA	2AA	55	555	58	SA	RD(1)				
DYB Write (7)	4	555	AA	2AA	55	555	48	SA	X1				
DYB Erase (7)	4	555	AA	2AA	55	555	48	SA	X0				
DYB Status	4	555	AA	2AA	55	555	58	SA	RD(0)				
PPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)
PPMLB Status (5)	4	555	AA	2AA	55	555	60	PL	RD(0)				
SPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)
SPMLB Status (5)	4	555	AA	2AA	55	555	60	SL	RD(0)				

Legend:

DYB = Dynamic Protection Bit
OW = Address (A6:A0) is (0011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A5:A0) is (001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits A21:A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A5:A0) is (010010)
WP = PPB Address (A6:A0) is (0111010) (Note 16)
EP = PPB Erase Address (A6:A0) is (1111010) (Note 16)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns device to reading array.*
6. *Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *Entire command sequence must be entered for each portion of password.*
9. *Command sequence returns FFh if PPMLB is set.*
10. *The password is written over four consecutive cycles, at addresses 0-3.*
11. *A 2 µs timeout is required between any two portions of password.*
12. *A 100 µs timeout is required between cycles 4 and 5.*
13. *A 1.2 ms timeout is required between cycles 4 and 5.*
14. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.*
15. *DQ1 = 1 if PPB locked, 0 if unlocked.*
16. *For all other parts that use the Persistent Protection Bit (excluding PDL128G), the WP and EP addresses are 00000010.*
17. *Immediately following successful unlock, write the SecSi Sector Exit command before attempting to verify, program, or erase the PPBs.*
18. *Immediately following the PPB Lock Status command write the SecSi Sector Exit command before attempting to verify, program, or erase the PPBs.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 16 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

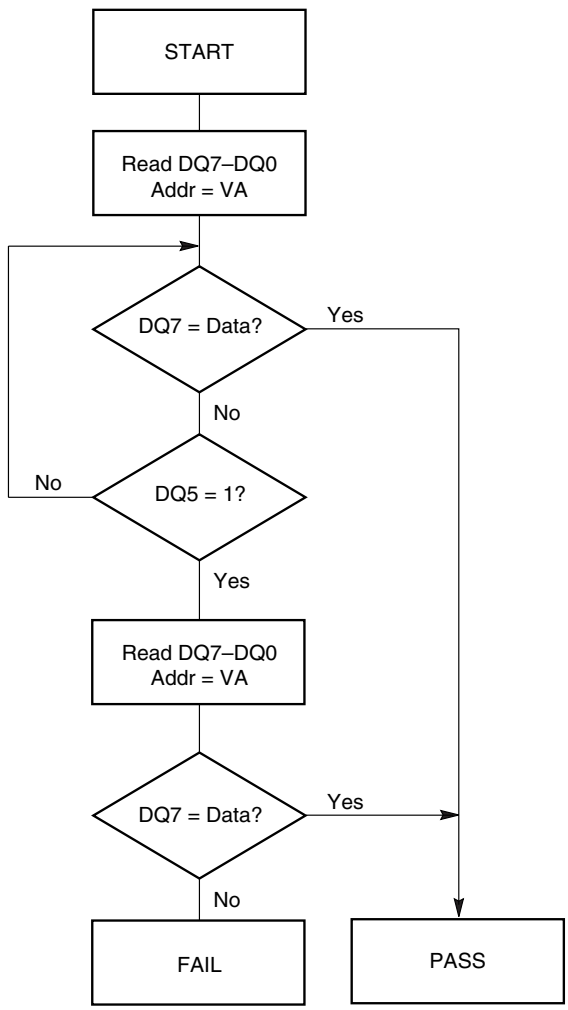
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 16 shows the outputs for Data# Polling on DQ7. Figure 6 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 16 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

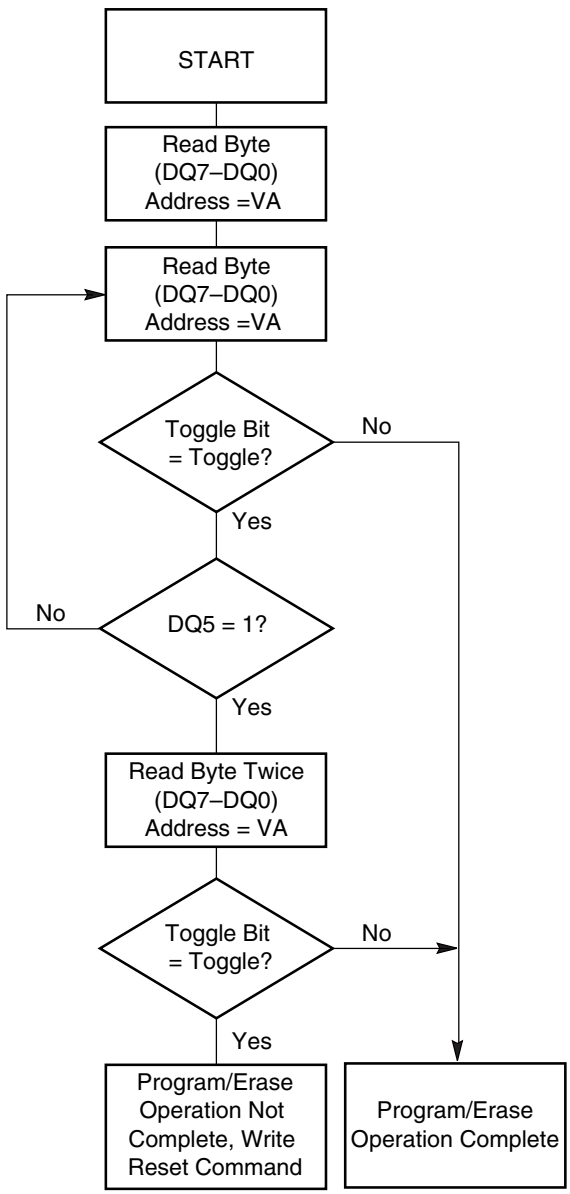
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 16 shows the outputs for Toggle Bit I on DQ6. Figure 7 shows the toggle bit algorithm. Figure 21 in the “Flash AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 16 to compare outputs for DQ2 and DQ6.

Figure 7 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ15–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ15–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 16 shows the status of DQ3 relative to the other status bits.

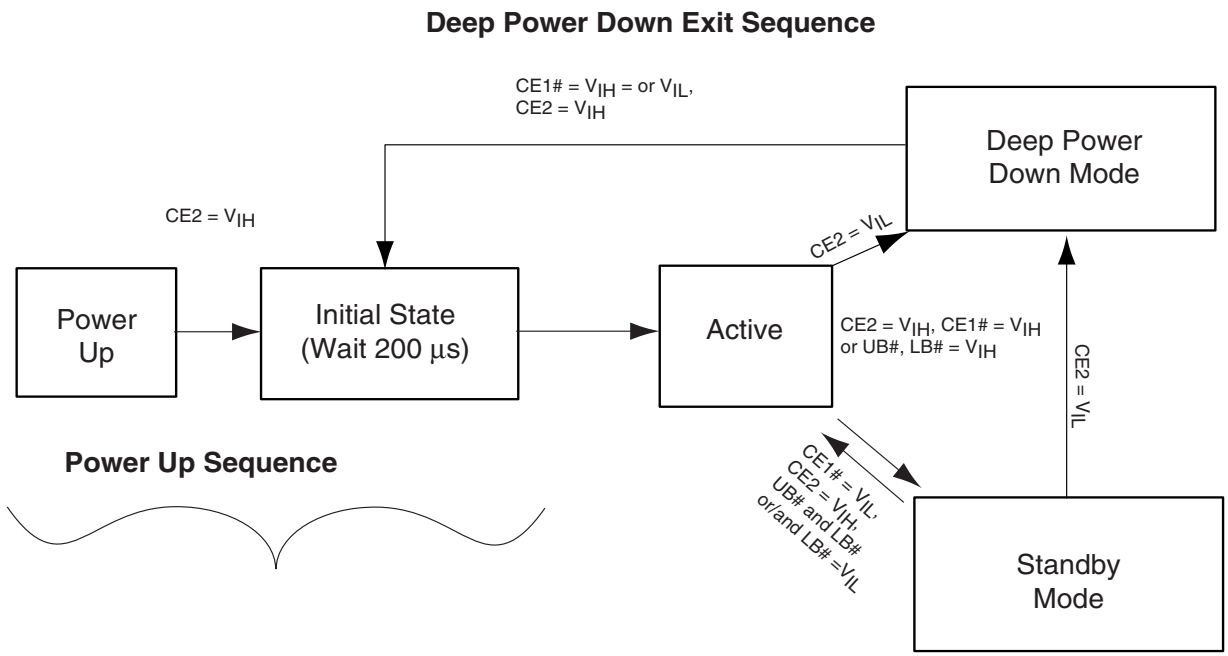
Table 15. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

PSRAM POWER DOWN



Note:*For Si-7 pSRAM, Deep Power-Down Standby is not available.*

Figure 8. State Diagram

Table 16. Standby Mode Characteristics

Power Mode	Memory Cell Data	Standby Current (µA)	Wait Time (µs)
Standby	Valid	100	0
Deep Power Down	Invalid	10	200

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –55°C to +125°C

Ambient Temperature
with Power Applied. . . . . –25°C to +85°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

RESET# (Note 2) . . . . . –0.5 V to +12.5 V

WP#/ACC . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 9. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins RESET#, and WP#/ACC is –0.5 V. During voltage transitions, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

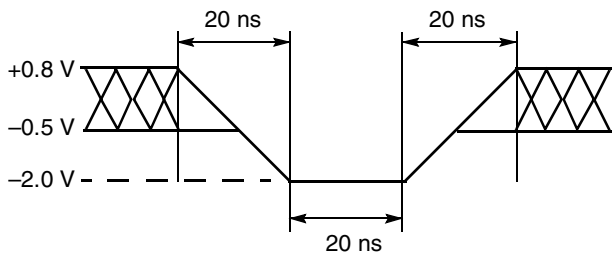


Figure 9. Maximum Negative Overshoot Waveform

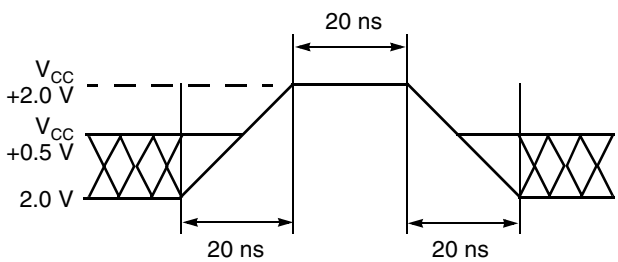


Figure 10. Maximum Positive Overshoot Waveform

OPERATING RANGES

Light Industrial (L) Devices

Ambient Temperature (T_A) . . . . . –25°C to +85°C

V_{CC}f/V_{CC}s Supply Voltages

V_{CC}f/V_{CC}s for standard voltage range . . 2.7 V to 3.1 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = $V_{CC\ max}$	5 MHz		10	20	mA
			10 MHz		25	45	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET#, WP#/ACC = V_{IO} ± 0.3 V			1	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			1	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{IO}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			1	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	Word		21	45	mA
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	Word		21	45	mA
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	CE# = V_{IL}, OE# = V_{IH}			17	35	mA
V_{IL}	Input Low Voltage						
				–0.5		0.8	V
V_{IH}	Input High Voltage						
				2		V_{CC}+0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage						
		I_{OL} = 4.0 mA, $V_{CC} = V_{CCS}$				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CCf} = V_{CCS}$		V_{IO}–0.1			V
		I_{OH} = –2.0 mA, $V_{CC} = V_{CCS}$		2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *Not 100% tested.*

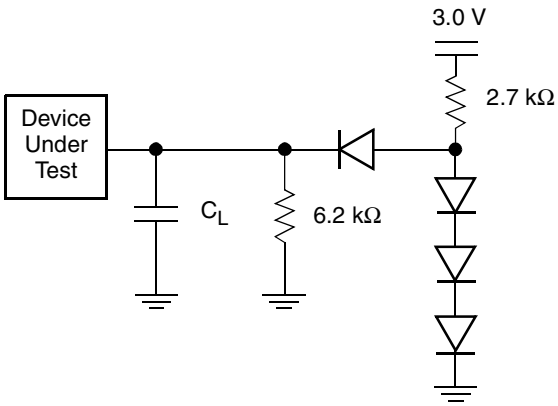
pSRAM DC AND OPERATING CHARACTERISTICS (NOTE 1)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE#1s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
$I_{CC1}s$	Operating Current at Minimum Cycle Time	Cycle time = Min., 100% duty I_{IO} = 0 mA, CE#1 ≤ 0.2 V, CE2 ≥ V_{DD} -0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{DD} -0.2 V			30	
$I_{CC2}s$	Operating Current at Maximum Cycle Time	Cycle time = 1 µs, 100% duty I_{IO} = 0 mA, CE#1 = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}			3	
V_{IL}	Input Low Voltage		–0.2 (Note 2)		0.6	V
V_{IH}	Input High Voltage		2.2		V_{CC}+0.2 (Note 1)	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA	2.4			V
I_{SB}	Standby Current (TTL)	CE#1s = V_{IH}, CE2 = V_{IL}, Other inputs = V_{IH} or V_{IL}			0.3	mA
I_{SB1}	Standby Current (CMOS)	CE1# = V_{DD} -0.2 V and CE2 = V_{DD} -0.2 V, Other inputs = V_{SS} ~ V_{CC}			100	µA
I_{SBD}	Deep Power Down (Note 4)	CE2 ≤ 0.2 V, Other Inputs = V_{SS} ~ V_{CC}			10	µA

Notes:

1. *Overshoot: VCC + 2.0 V in case of pulse width* ≤ 20 ns.
2. *Undershoot: -2.0 V in case of pulse width* ≤ 20 ns.
3. *Not 100% Tested*
4. *For Si-7 pSRAM, Deep Power-down Standby is not available.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 17. Test Specifications

Test Condition	70, 85	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

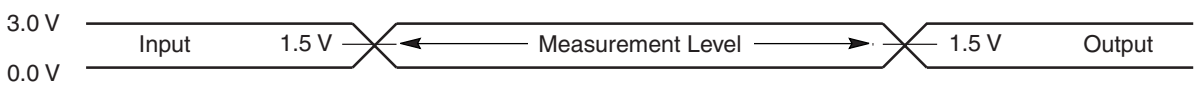


Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

pSRAM CE#s Timing

Parameter		Description	Test Setup		All Speeds	Unit
JEDEC	Std					
—	t_{CCR}	CE#s Recover Time	—	Min	0	ns

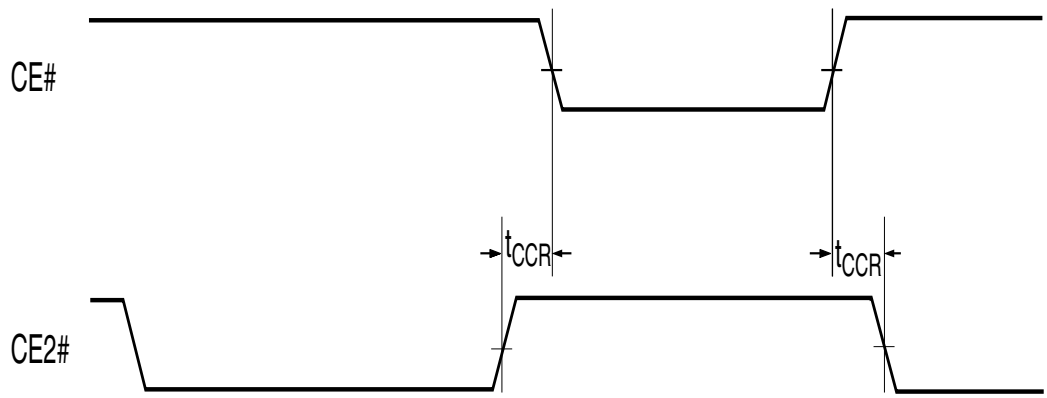


Figure 13. Timing Diagram for Alternating Between pSRAM to Flash

AC CHARACTERISTICS

Flash Read-Only Operations

Parameter		Description		Test Setup	Speed Options			Unit
JEDEC	Std.					70	85	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	85	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	70	85	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	85	ns
	t_{PACC}	Page Access Time			Max	25	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 3)			Max	25	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	25	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	4	5	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 18 for test specifications*
3. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}*

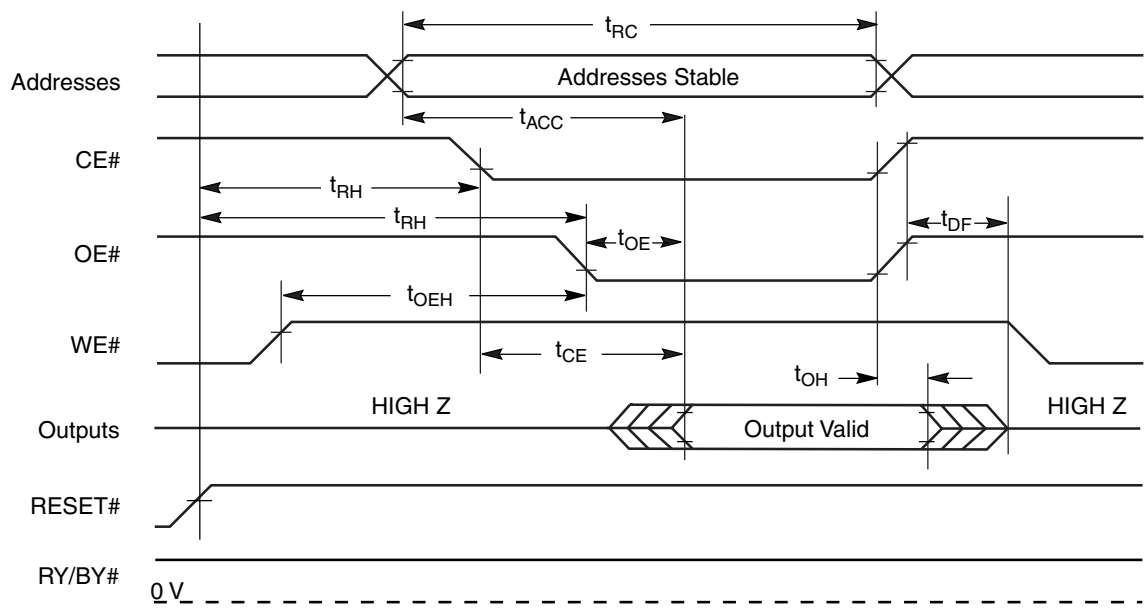


Figure 14. Read Operation Timings

AC CHARACTERISTICS

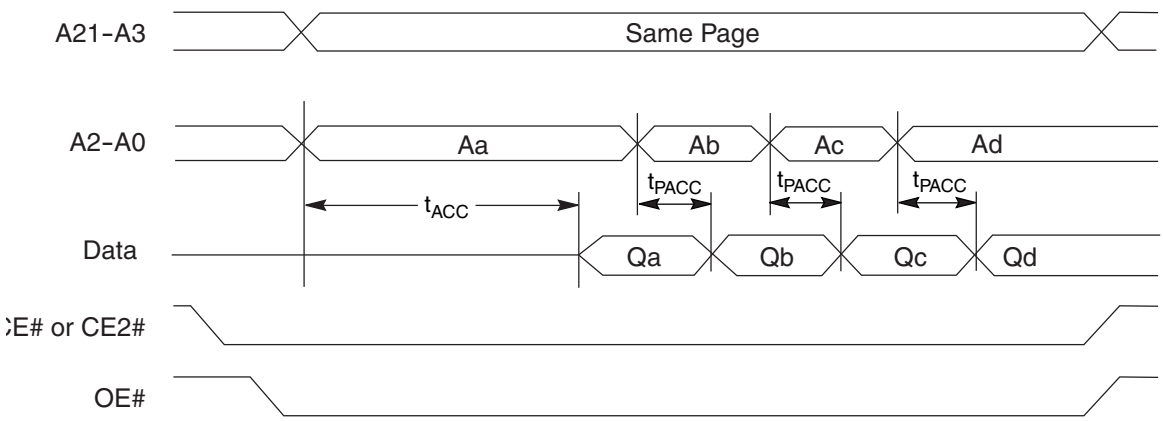


Figure 15. Page Read Operation Timings

FLASH AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

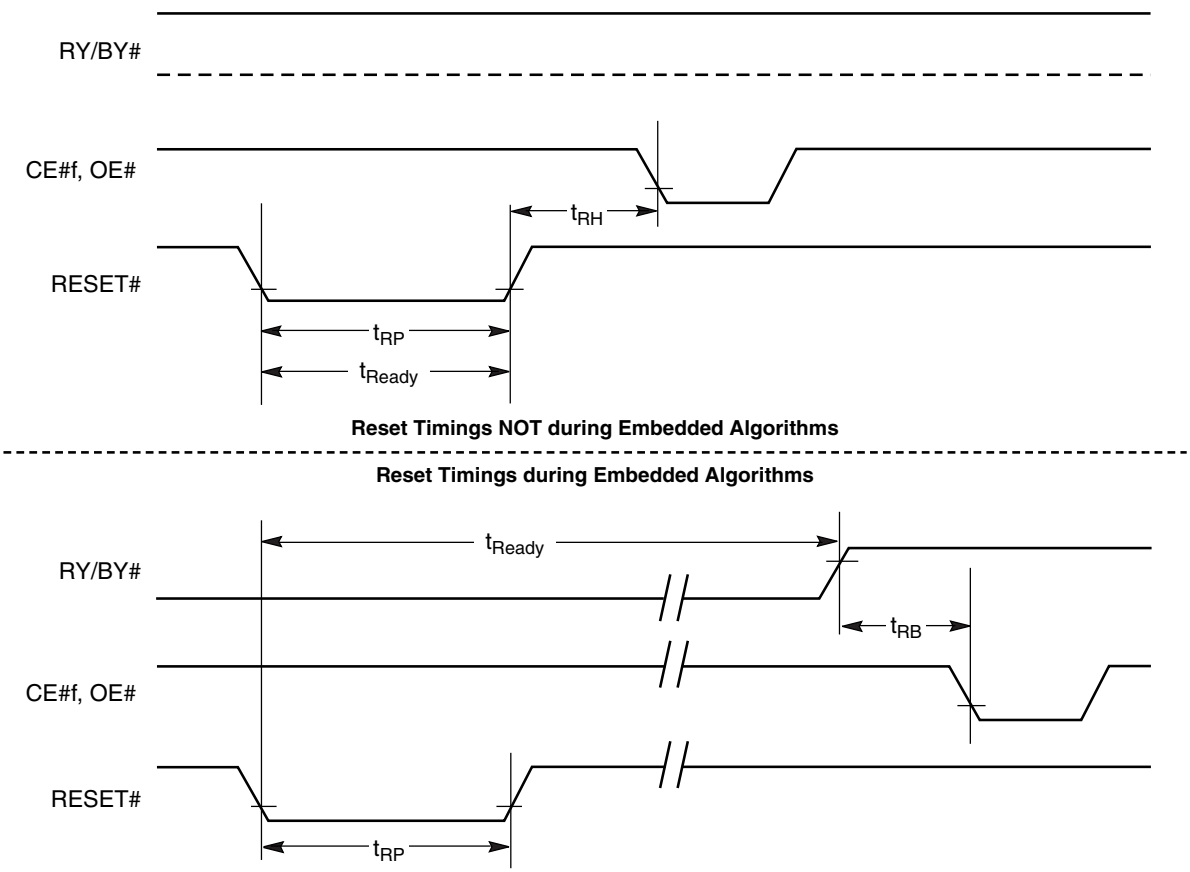


Figure 16. Reset Timings

AC CHARACTERISTICS

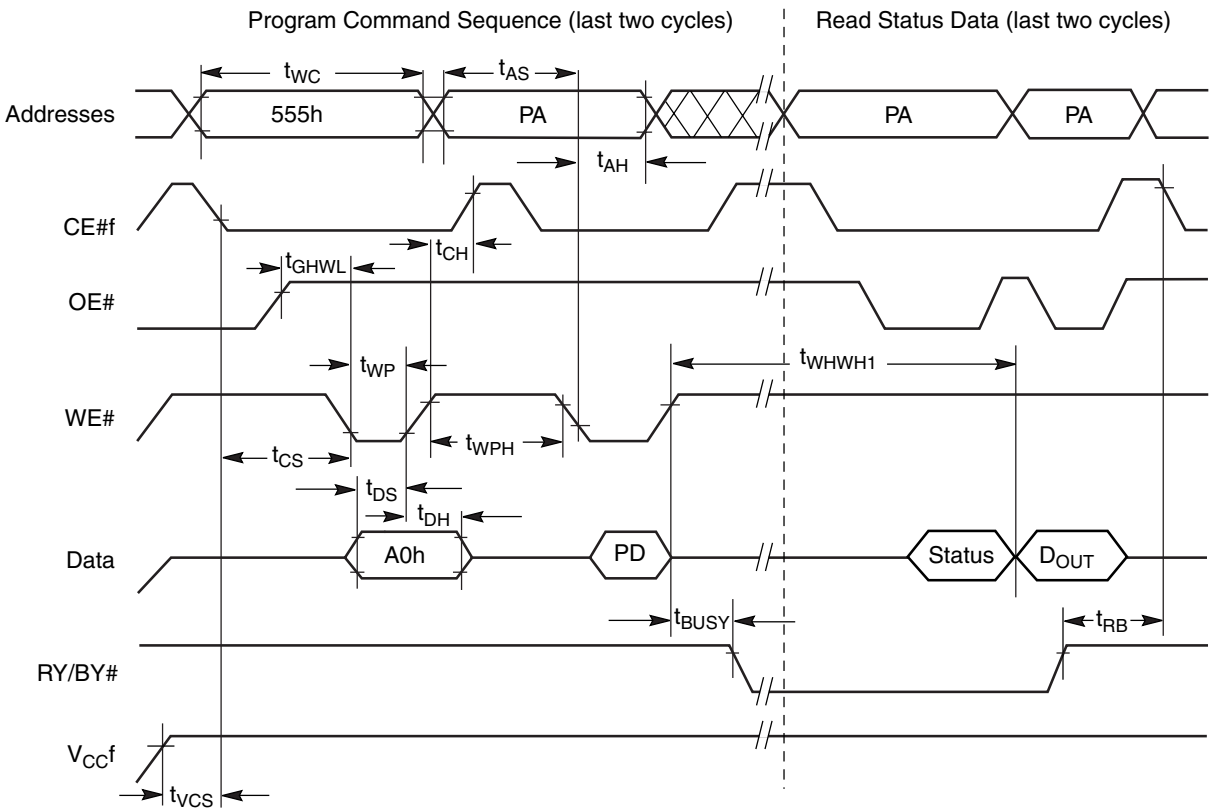
Flash Erase and Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std			70	85	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	85	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45		ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35		ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35		ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.2		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50		µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90		ns

Notes:

1. *Not 100% tested.*
2. *See the "Deep Power Down Mode" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, D_{OUT} is the true data at the program address..

Figure 17. Program Operation Timings

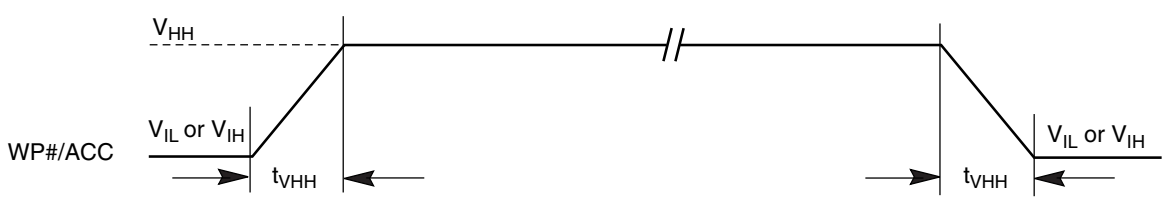
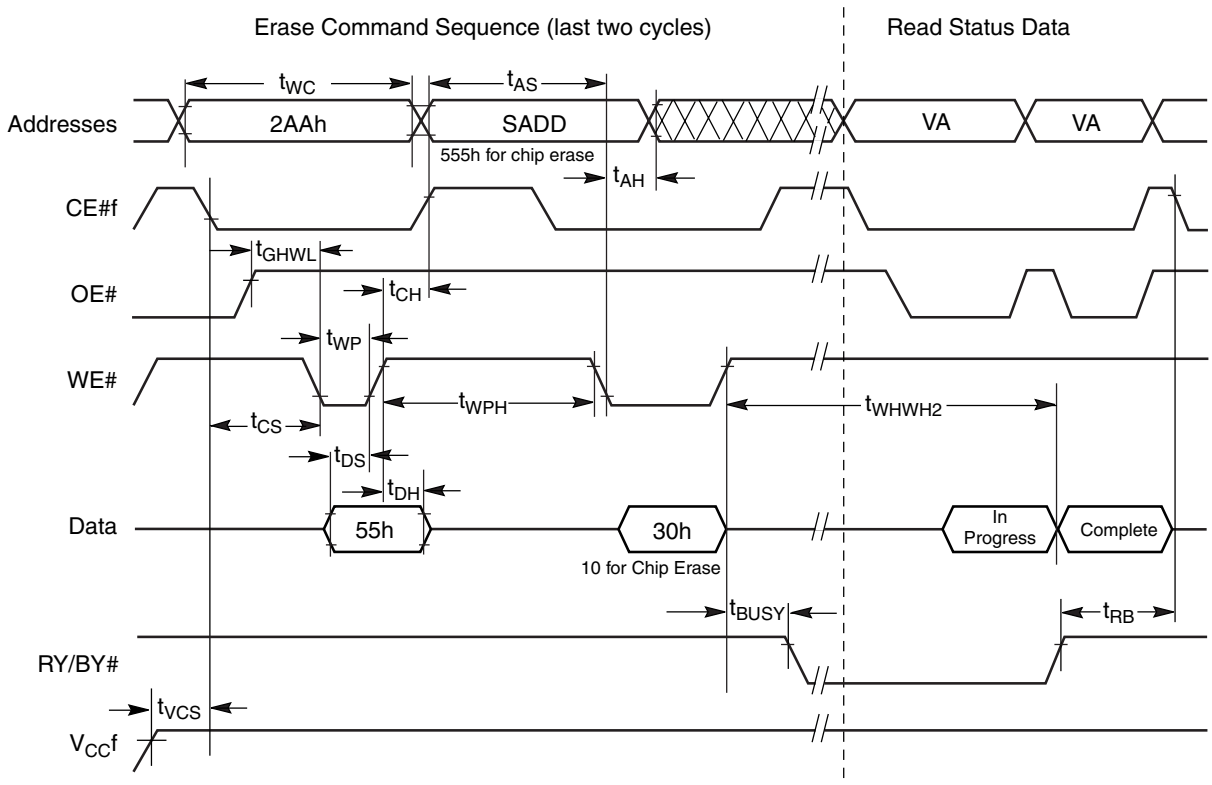


Figure 18. Accelerated Program Timing Diagram

FLASH AC CHARACTERISTICS



Notes:

1. SADD = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").

Figure 19. Chip/Sector Erase Operation Timings

FLASH AC CHARACTERISTICS

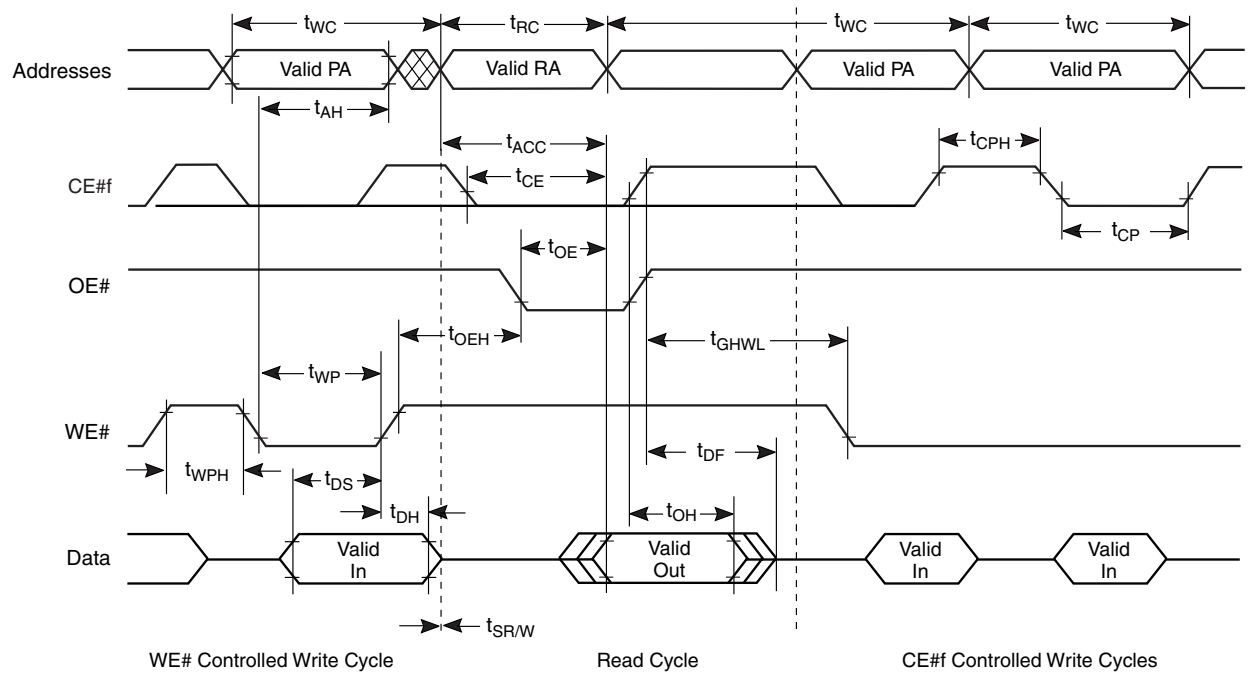
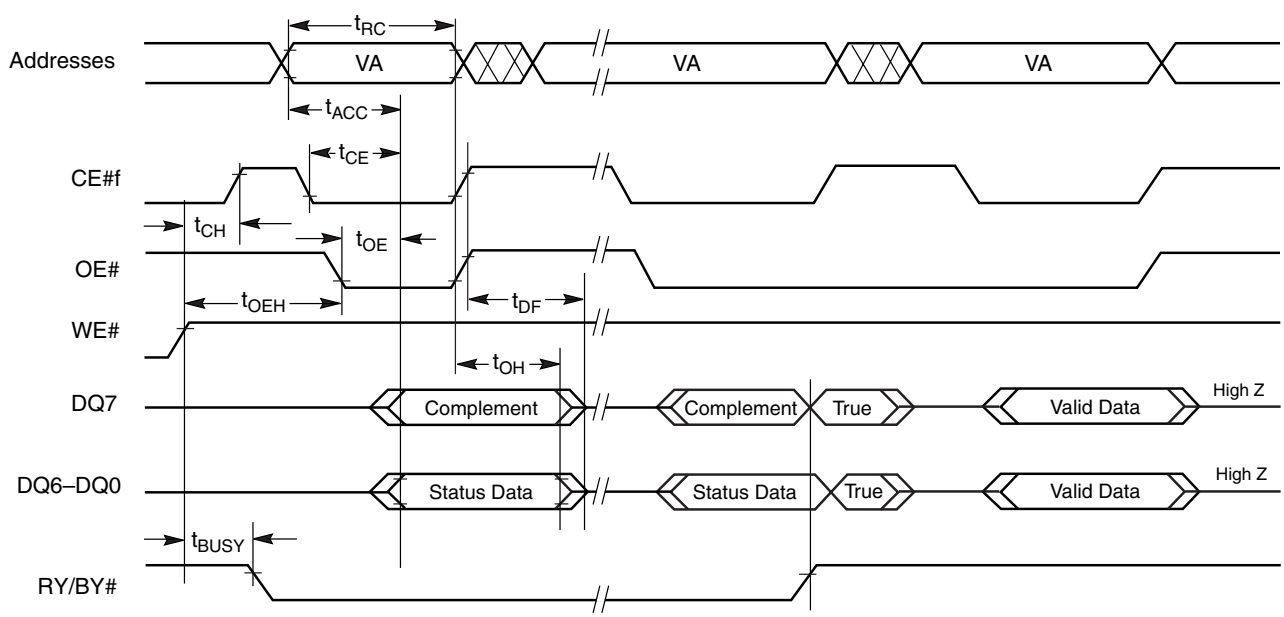


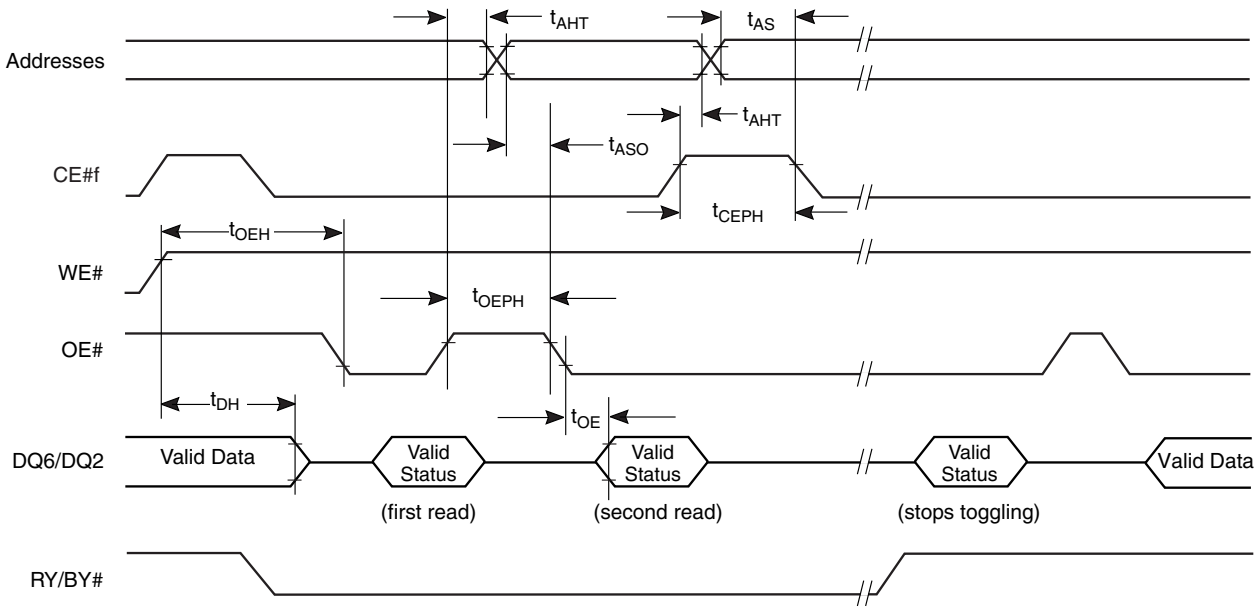
Figure 20. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

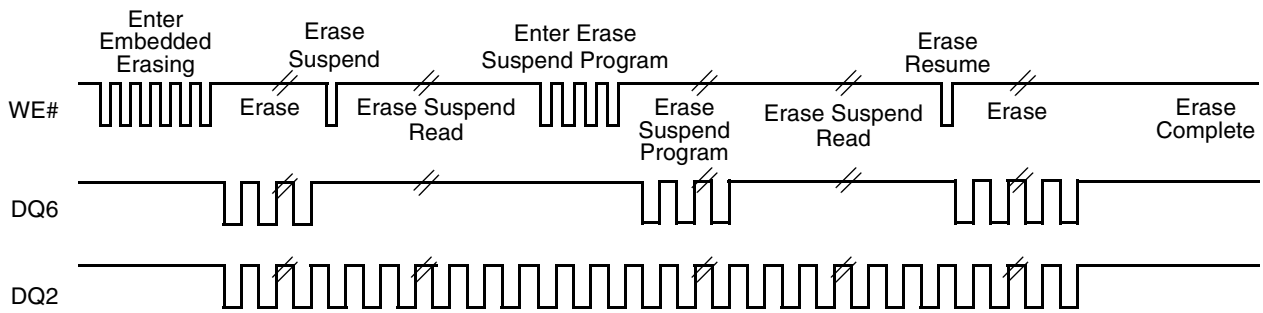
Figure 21. Data# Polling Timings (During Embedded Algorithms)

FLASH AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 22. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE#f to toggle DQ2 and DQ6.*

Figure 23. DQ2 vs. DQ6

FLASH AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

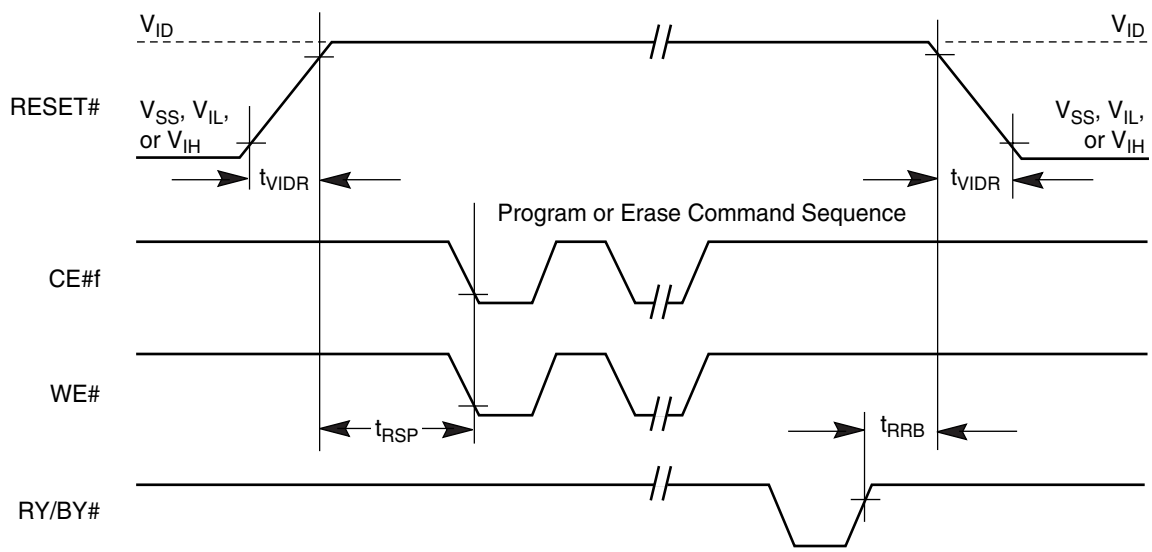
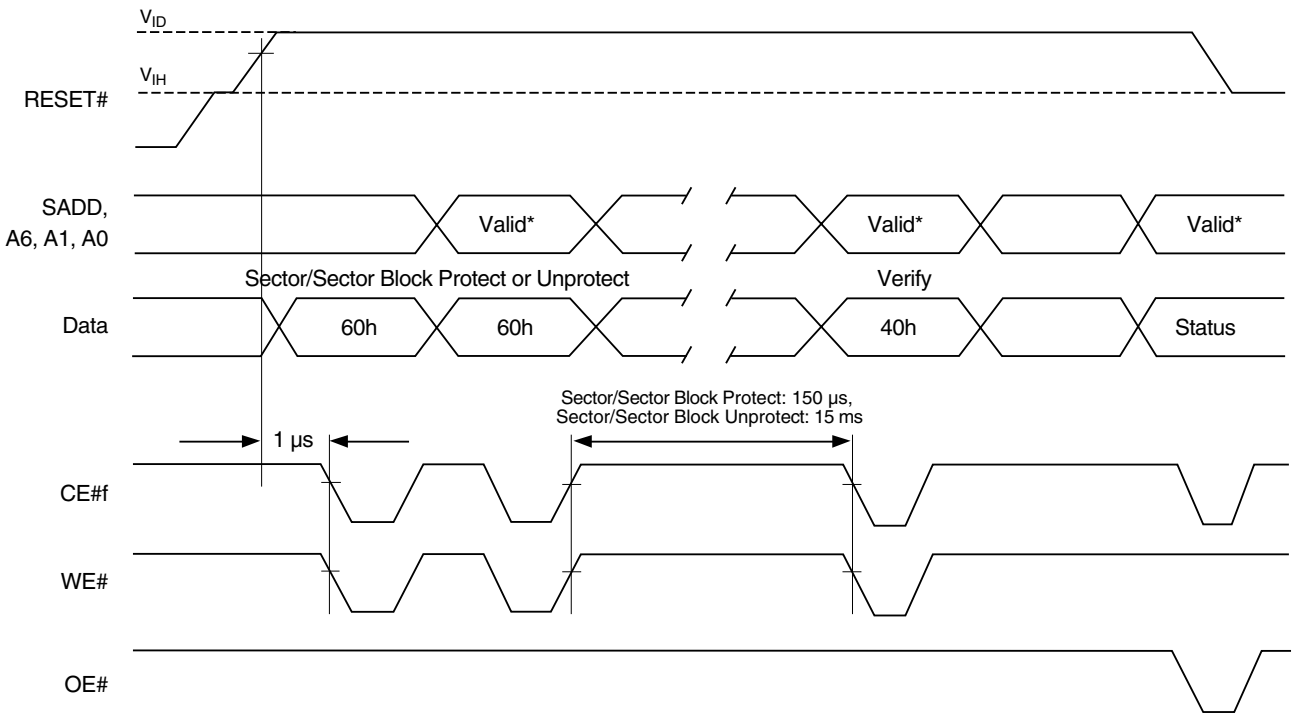


Figure 24. Temporary Sector Unprotect Timing Diagram

FLASH AC CHARACTERISTICS



** For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0, SADD = Sector Address.*

Figure 25. Sector/Sector Block Protect and Unprotect Timing Diagram

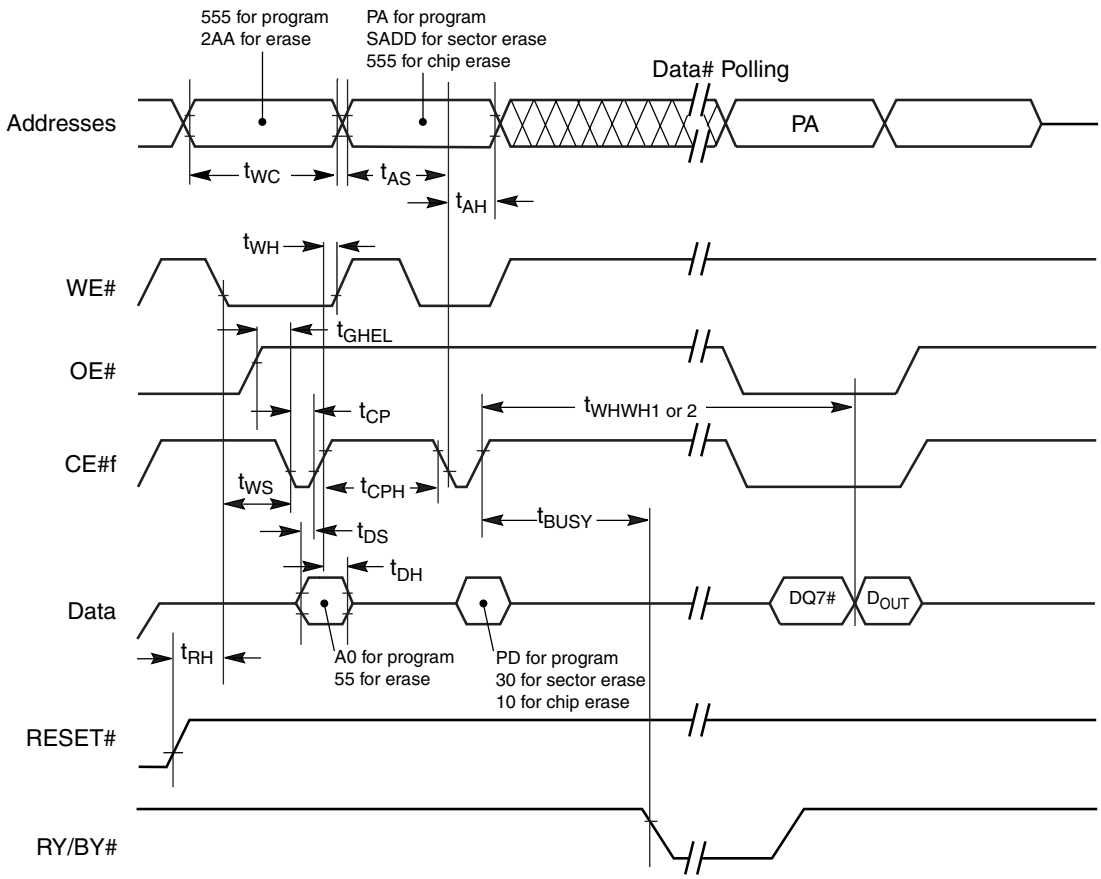
FLASH AC CHARACTERISTICS

Flash Alternate CE#f Controlled Erase and Program Operations

Parameter				Speed Options		
JEDEC	Std.	Description		70	85	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	85	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45		ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35		ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.2		sec

1. *Not 100% tested.*
2. *See the "Deep Power Down Mode" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SADD = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device..*

Figure 26. Flash Alternate CE#f Controlled Write (Erase/Program) Operation Timings

pSRAM AC CHARACTERISTICS

Power Up Time (Etron pSRAM only)

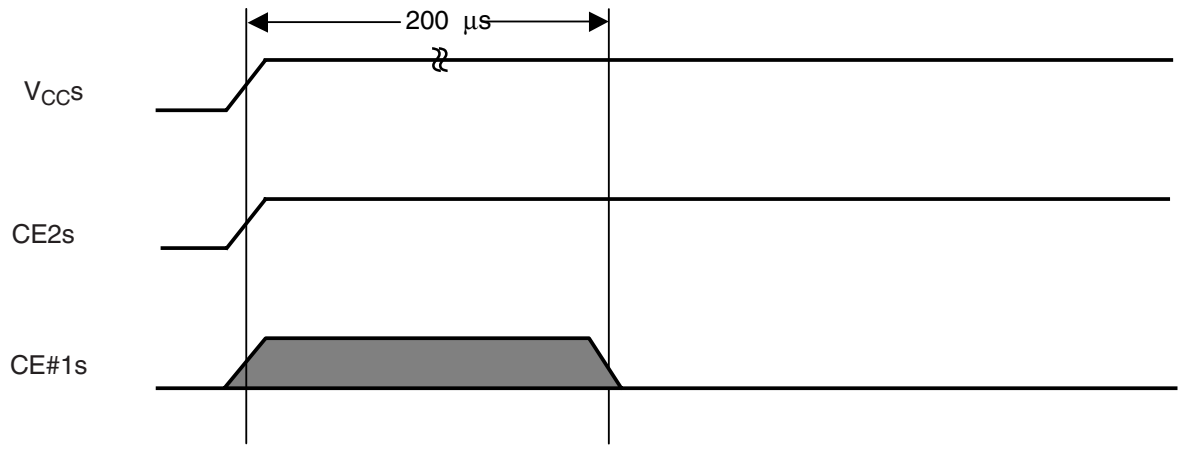
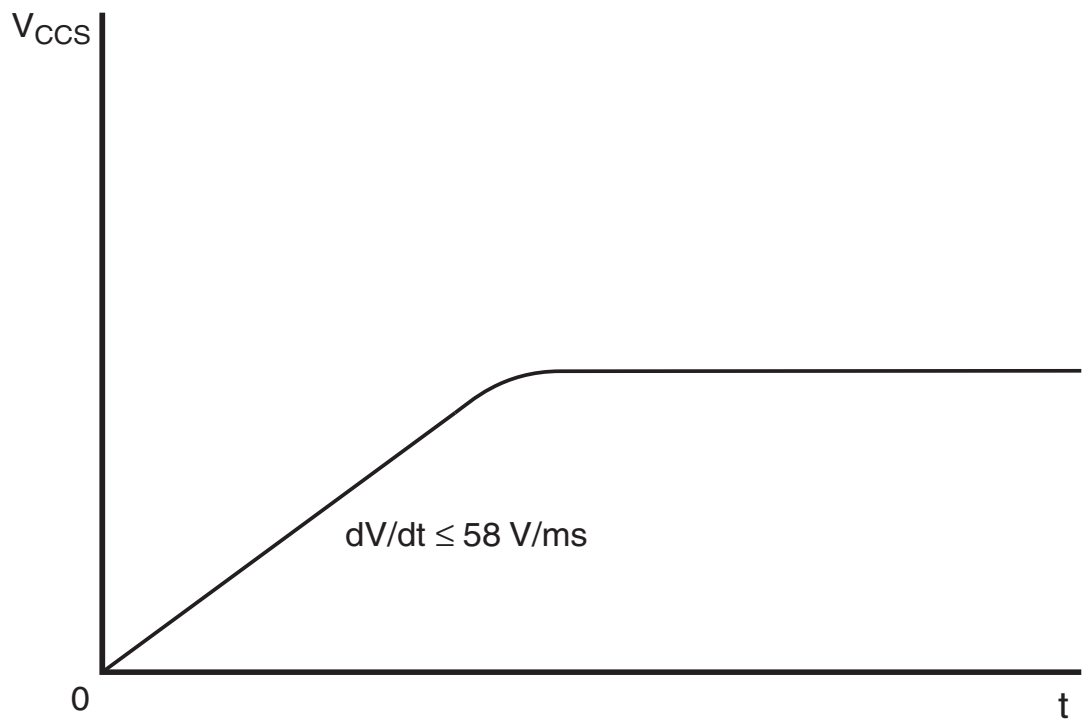


Figure 27. Power Up

V_{CCS} Slew Rate (Etron pSRAM only)



Notes:

1. *At any time during Power Up, the V_{CCS} slew rate (i.e. rate of change) must not exceed 58 V/ms (alternately, it must exceed 17 µs/V).*
2. *Power up and Slew Rate requirements apply to Etron pSRAM only.*

Figure 28. V_{CCS} Slew Rate

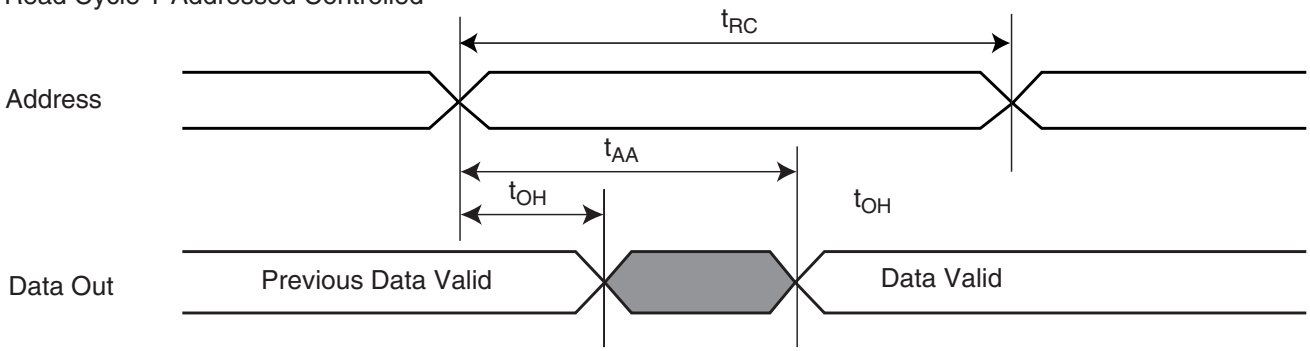
pSRAM Read Cycle

Parameter Symbol	Description		Speed		Unit
			70	85	
t_{RC}	Read Cycle Time	Min	70	85	ns
t_{AA}	Address Access Time	Max	70	85	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	70	85	ns
t_{OE}	Output Enable Access Time	Max	35	40	ns
t_{BA}	LB#s, UB#s to Access Time	Max	70	85	ns
t_{LZ12}	Chip Enable Low to Low-Z Output	Min	10		ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10		ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5		ns
t_{HZ1}	Chip Disable to High-Z Output	Max	25	35	ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25	35	ns
t_{OHZ}	Output Disable to High-Z Output	Max	25	35	ns
t_{OH}	Output Data Hold from Address Change	Min	10		ns

pSRAM AC CHARACTERISTICS

Read Cycle

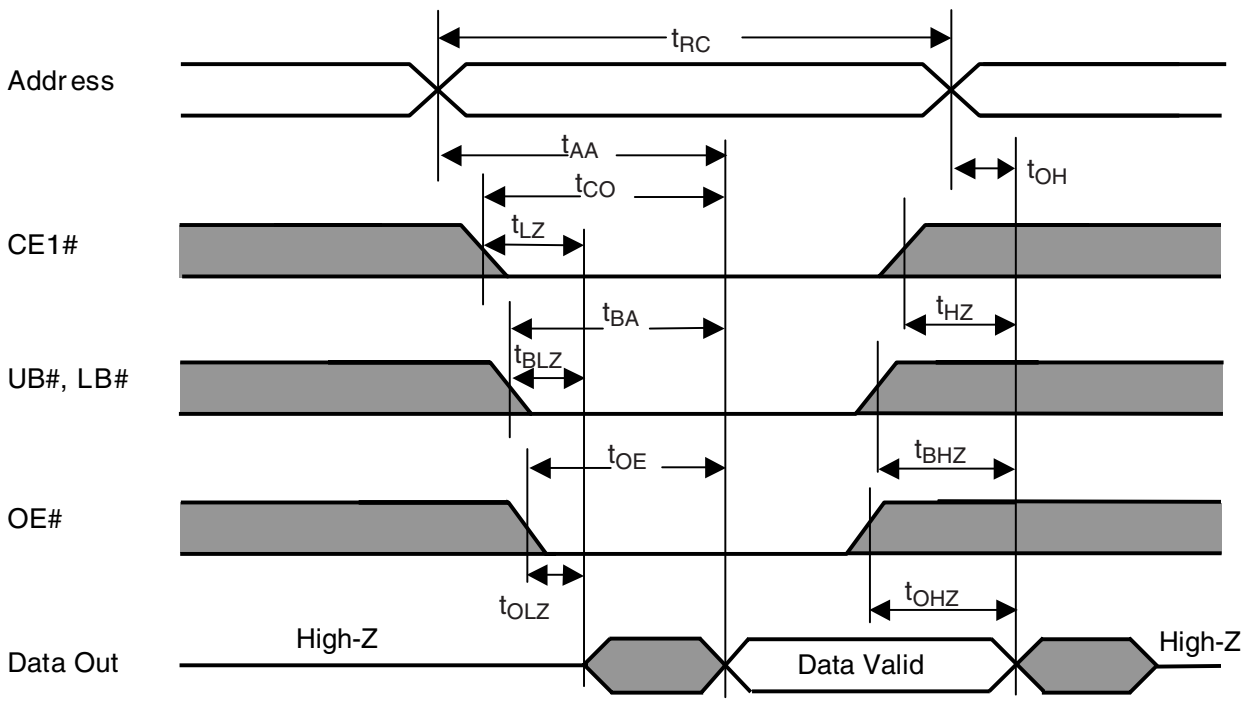
Read Cycle 1-Addressed Controlled



Note:

1. CE1# = OE# = V_{IL}, CE2 = WE# = V_{IH}, UB# or/and LB# = V_{IL}

Figure 29. pSRAM Read Cycle–Address Controlled



Note:

1. CE2 = WE# = V_{IH}

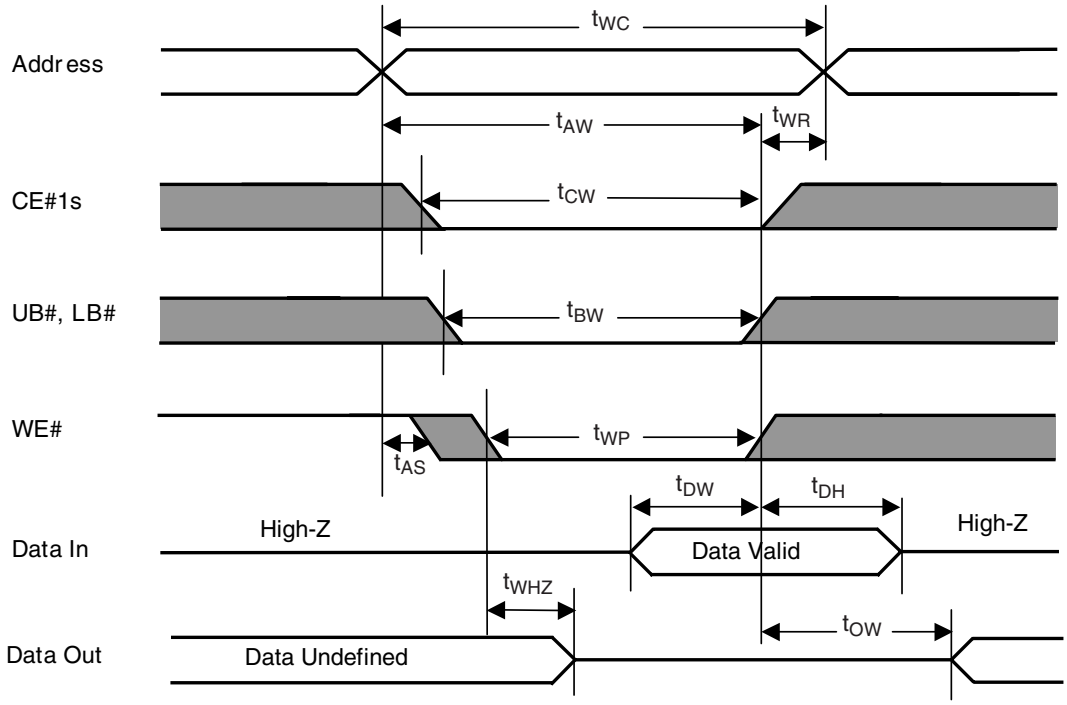
Figure 30. pSRAM Read Cycle–CS1# Controlled

pSRAM AC CHARACTERISTICS

Write Cycle

Parameter Symbol	Description		Speed		Unit
			70	85	
t_{WC}	Write Cycle Time	Min	70	85	ns
t_{Cw}	Chip Enable to End of Write	Min	60	70	ns
t_{AS}	Address Setup Time	Min	0		ns
t_{AW}	Address Valid to End of Write	Min	60	70	ns
t_{BW}	UB#s, LB#s to End of Write	Min	60	70	ns
t_{WP}	Write Pulse Time	Min	50	60	ns
t_{WR}	Write Recovery Time	Min	0		ns
t_{WHZ}	Write to Output High-Z	Min	0		ns
		Max	20	30	
t_{DW}	Data to Write Time Overlap	Min	30	30	ns
t_{DH}	Data Hold from Write Time	Min	0		ns
t_{OW}	End Write to Output Low-Z	min	5		ns

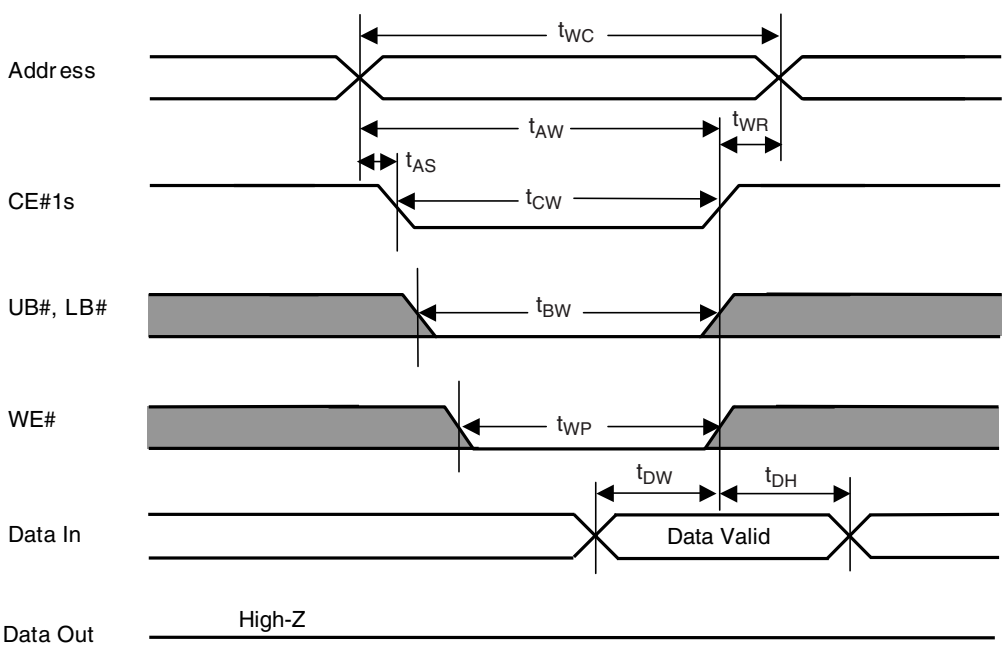
pSRAM AC CHARACTERISTICS



Note:

1. *CE2s = V_{IH}*
2. *CE2s = WE# = V_{IH}*

Figure 31. pSRAM Write Cycle–WE# Controlled

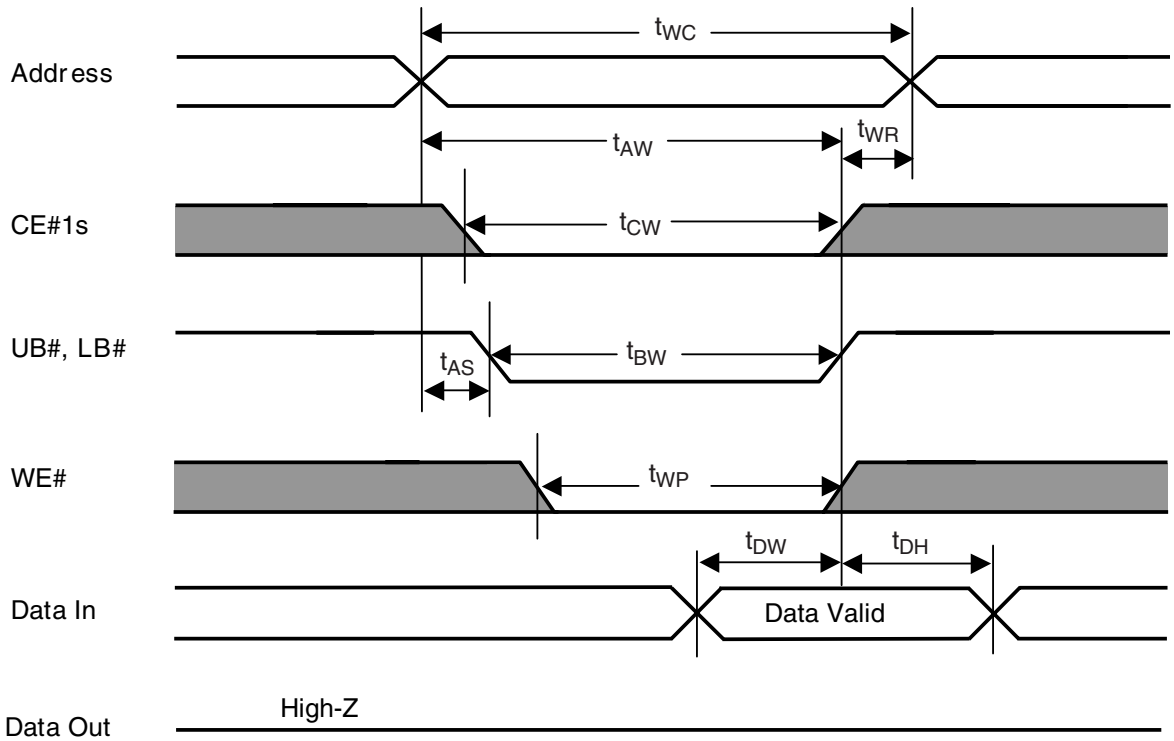


Note:

1. *CE2s = V_{IH}*
2. *CE2s = WE# = V_{IH}*

Figure 32. pSRAM Write Cycle–CS1# Controlled

PSRAM AC CHARACTERISTICS



Note:

1. *CE2s = V_{IH}*
2. *CE2s = WE# = V_{IH}*

Figure 33. pSRAM Write Cycle–UB#, LB# Controlled

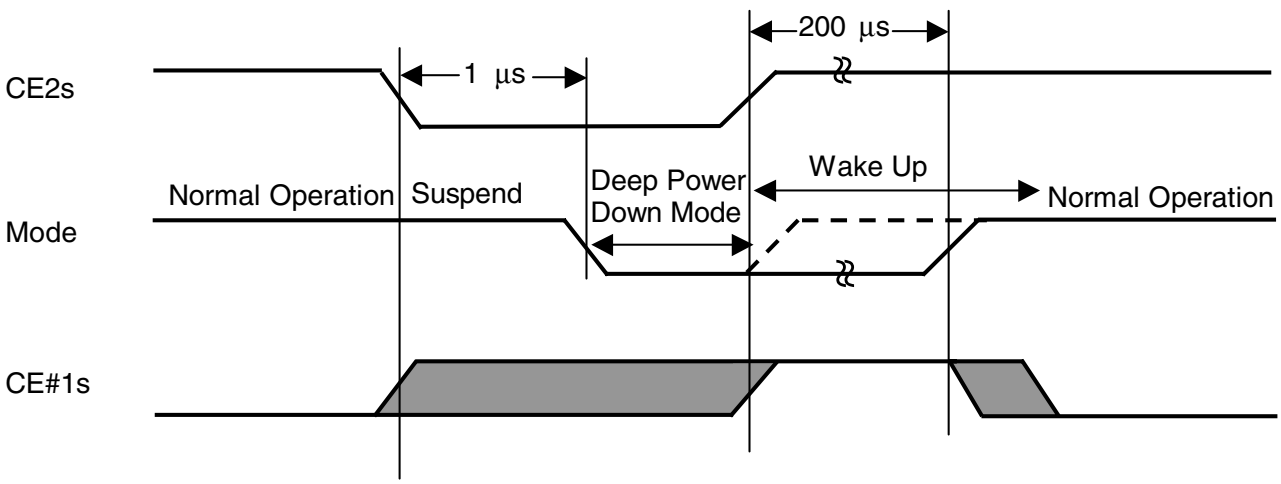
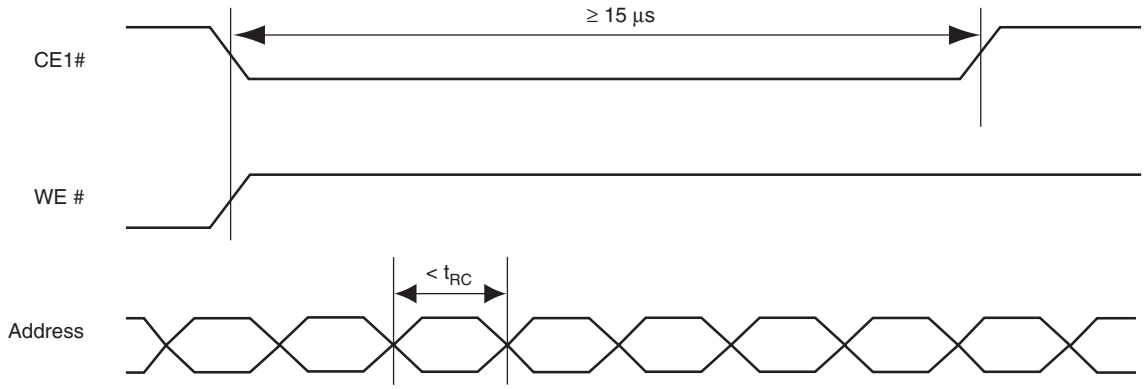


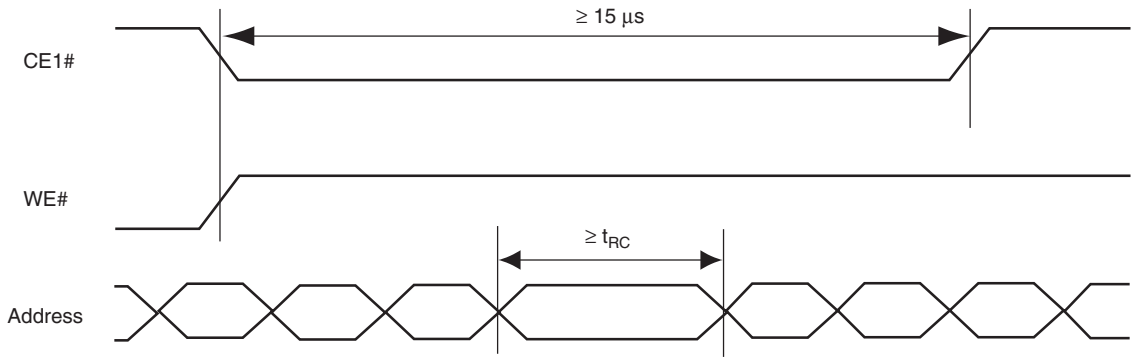
Figure 34. Deep Power Down Mode

PSRAM AC CHARACTERISTICS



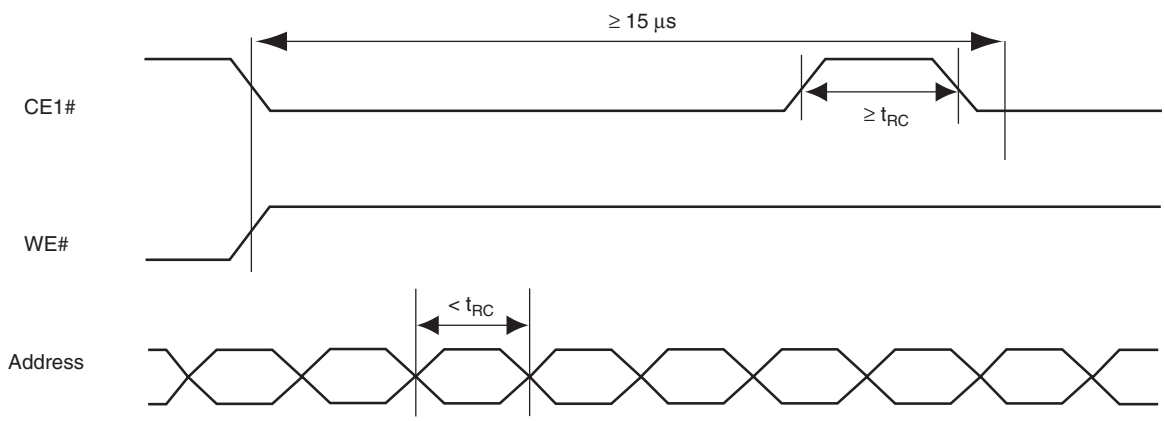
Note: *Applies to Etron pSRAM only.*

Figure 35. Abnormal Timing



Note: *Applies to Etron pSRAM only.*

Figure 36. Avoidable Timing 1



Note: *Applies to Etron pSRAM only.*

Figure 37. Avoidable Timing 2

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.4	5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	56		sec	
Word Program Time	7	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time	4	120	µs	
Chip Program Time (Note 3)	28	84	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables Table 14 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including RESET#)	–1.0 V	13 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

PACKAGE PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	14	16	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	17	20	pF

Notes:

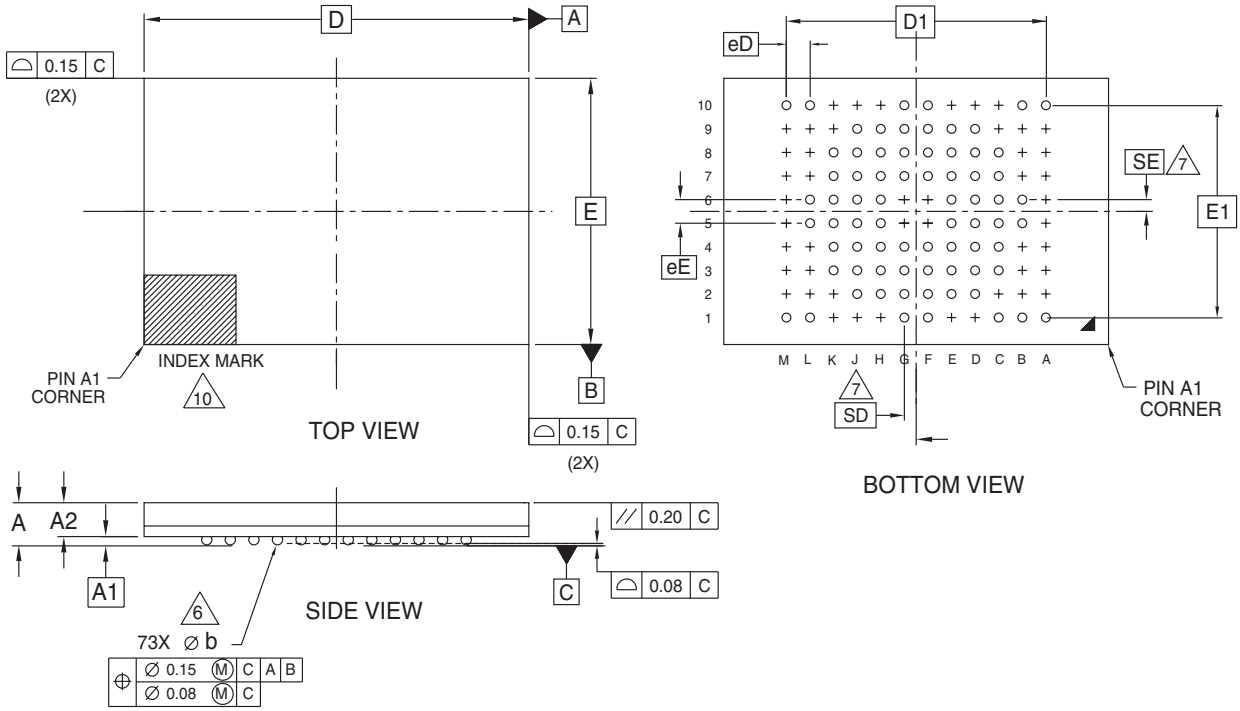
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

FLASH DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

FLK073—73-Ball Fine-Pitch Grid Array 13 x 9 mm



PACKAGE	FLK 073			
JEDEC	N/A			
	13.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.25	---	---	BALL HEIGHT
A2	0.98	---	1.08	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		9.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		72		BALL COUNT
ϕb	0.30	0.35	0.40	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9, B2,B3,B4,B7,B8,B9 C2,C9,C10,D1,D10,E1,E10, F5,F6,G5,G6,H1,H10 J1,J10,K1,K2,K9,K10, L2,L3,L4,L7,L8,L9 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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REVISION SUMMARY

Revision A (February 21, 2003)

Initial Release

Revision A+1 (March 14, 2003)

Ordering Information

Corrected typo in temperature range.

Revision A+2 (April 4, 2003)

Ordering Information

Corrected typo in temperature range.

Corrected OPNs

Revision A+3 (April 7, 2003)

Ordering Information

Corrected typo in temperature range.

Revision A+4 (August 5, 2003)

Figure 28. V_{CCS} Slew Rate

Added Figure.

Revision A+5 (November 20, 2003)

Distinctive Characteristics, Pseudo SRAM Features

Added bullet regarding pSRAM vendors.

Ordering Information

Added Si-7 pSRAM option.

Device Bus Operations

Added Note 10.

pSRAM Power Down

Added Note.

pSRAM DC and Operating Characteristics

Added Note 4.

pSRAM AC Characteristics

Added Note to diagrams.