

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J16FS

High Speed Switching Applications

Analog Switch Applications

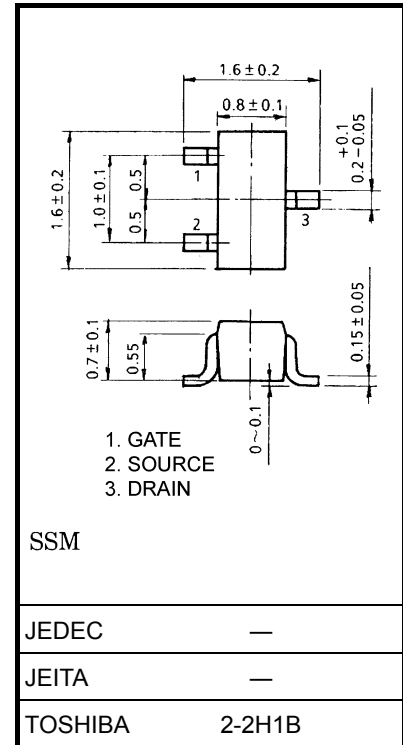
- Small package
- Low on-resistance : $R_{on} = 8 \Omega$ (max) (@ $V_{GS} = -4$ V)
: $R_{on} = 12 \Omega$ (max) (@ $V_{GS} = -2.5$ V)
: $R_{on} = 45 \Omega$ (max) (@ $V_{GS} = -1.5$ V)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

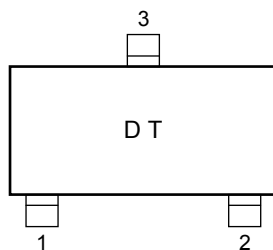
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-20	V
Gate-Source voltage		V_{GSS}	± 10	V
Drain current	DC	I_D	-100	mA
	Pulse	I_{DP}	-200	
Drain power dissipation ($T_a = 25^\circ\text{C}$)		P_D	100	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

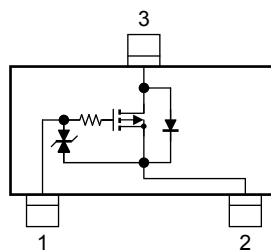
Unit: mm



Marking



Equivalent Circuit (top view)



Handling Precaution

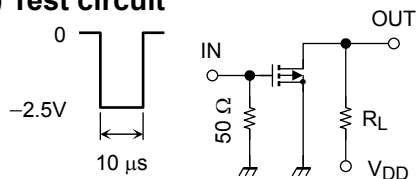
When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Gate leakage current	I_{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage	$V_{(BR) DSS}$	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-20	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-0.6	—	-1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$	25	—	—	mS
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$	—	6	8	Ω
		$I_D = -10 \text{ mA}, V_{GS} = -2.5 \text{ V}$	—	8	12	
		$I_D = -1 \text{ mA}, V_{GS} = -1.5 \text{ V}$	—	18	45	
Input capacitance	C_{iss}	$V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	11	—	pF
Reverse transfer capacitance	C_{rss}		—	3.7	—	pF
Output capacitance	C_{oss}		—	10	—	pF
Switching time	Turn-on time	$V_{DD} = -3 \text{ V}, I_D = -10 \text{ mA}, V_{GS} = 0 \sim -2.5 \text{ V}$	—	130	—	ns
	Turn-off time		—	190	—	

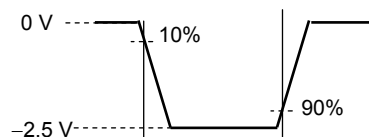
Switching Time Test Circuit

(a) Test circuit

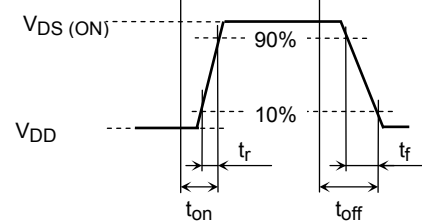


$V_{DD} = -3 \text{ V}$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



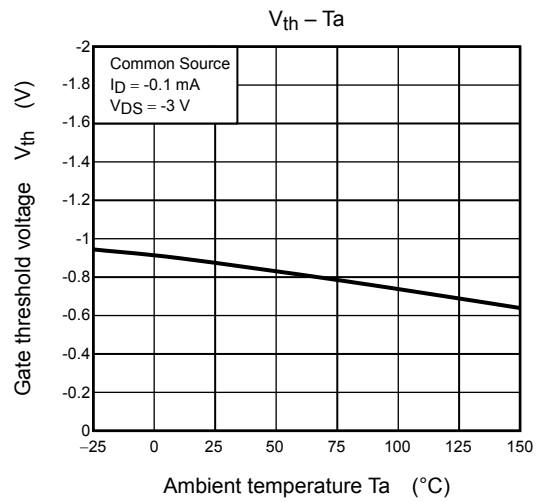
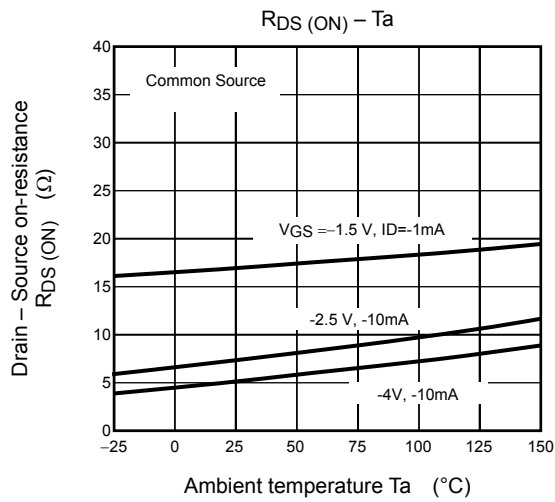
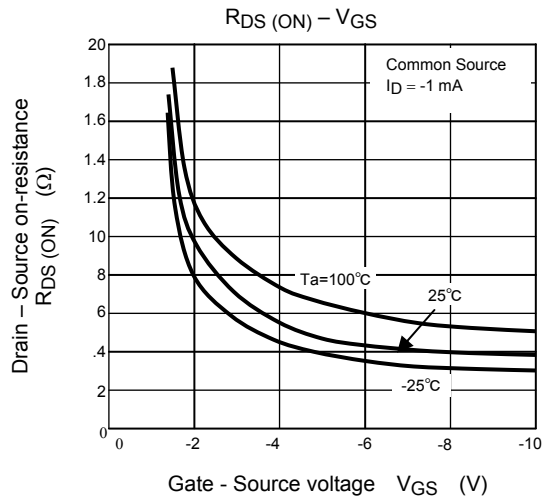
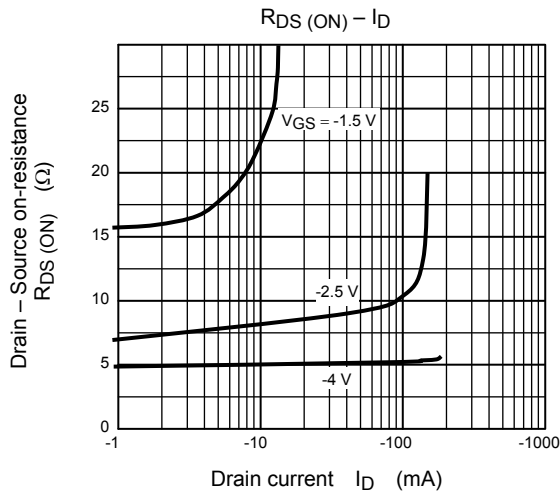
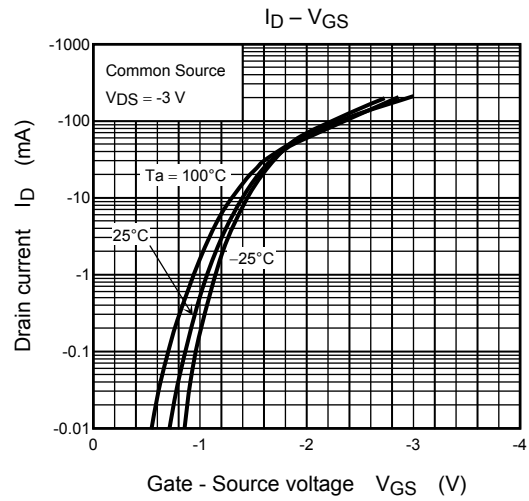
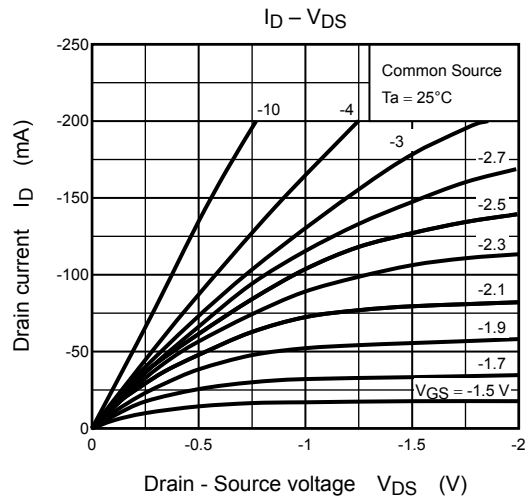
(c) V_{OUT}

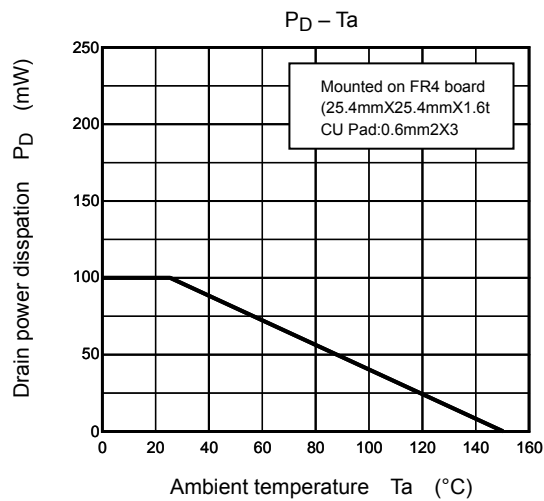
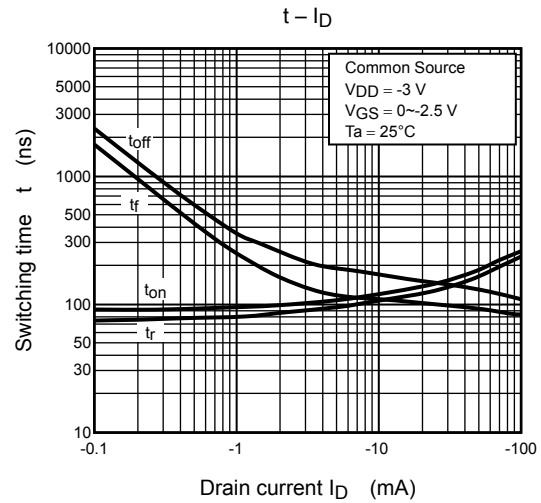
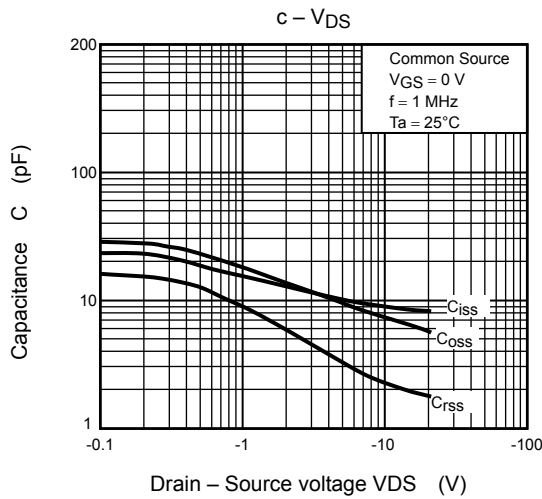
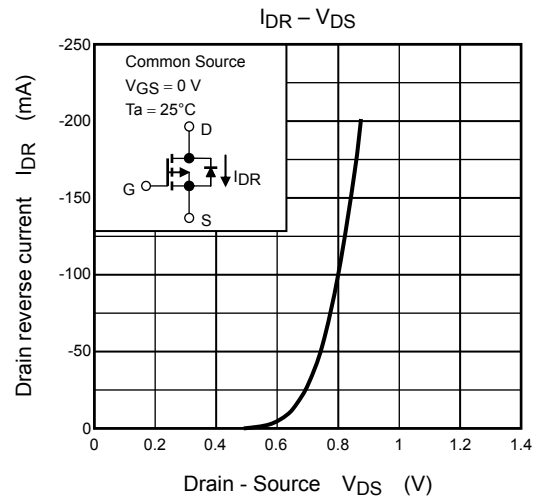
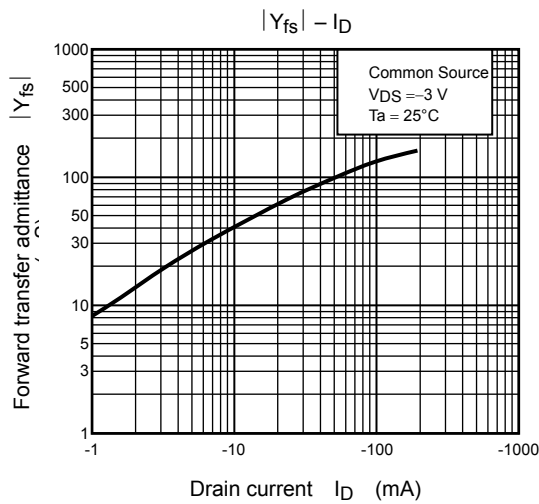


Precaution

V_{th} can be expressed as the voltage between the gate and source when the low operating current value is $I_D = 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} and $V_{GS(OFF)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

Be sure to take this into consideration when using the device.





RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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