

FEATURES

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75K Ω input pull-down resistors
- Available in 16-pin SOIC package



Precision Edge®

DESCRIPTION

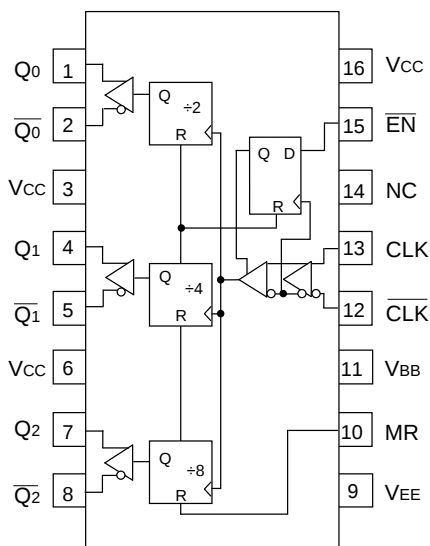
The SY10/100EL34/L are low skew $\div 2$, $\div 4$, $\div 8$ clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01 μ F capacitor. The VBB output is designed to act as the switching reference for the input of the EL34/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34/Ls in a system.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q0	Differential $\div 2$ Outputs
Q1	Differential $\div 4$ Outputs
Q2	Differential $\div 8$ Outputs

PACKAGE/ORDERING INFORMATION**16-Pin Narrow SOIC (Z16-2)****Ordering Information⁽¹⁾**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10EL34LZC	Z16-2	Commercial	SY10EL34LZC	Sn-Pb
SY10EL34LZCTR ⁽²⁾	Z16-2	Commercial	SY10EL34LZC	Sn-Pb
SY100EL34LZC	Z16-2	Commercial	SY100EL34LZC	Sn-Pb
SY100EL34LZCTR ⁽²⁾	Z16-2	Commercial	SY100EL34LZC	Sn-Pb
SY10EL34LZI	Z16-2	Industrial	SY10EL34LZI	Sn-Pb
SY10EL34LZITR ⁽²⁾	Z16-2	Industrial	SY10EL34LZI	Sn-Pb
SY100EL34LZI	Z16-2	Industrial	SY100EL34LZI	Sn-Pb
SY100EL34LZITR ⁽²⁾	Z16-2	Industrial	SY100EL34LZI	Sn-Pb
SY10EL34LZG ⁽³⁾	Z16-2	Industrial	SY10EL34LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY10EL34LZGTR ^(2, 3)	Z16-2	Industrial	SY10EL34LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL34LZG ⁽³⁾	Z16-2	Industrial	SY100EL34LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL34LZGTR ^(2, 3)	Z16-2	Industrial	SY100EL34LZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

CLK	$\overline{EN}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q ₀₋₂
X	X	H	Reset Q ₀₋₂

NOTE:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

DC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply	—	—	49	—	—	49	—	—	49	—	—	49	mA
	Current	—	—	49	—	—	49	—	—	49	—	—	54	
V _{BB}	Output Reference	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	V
	Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	
I _{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

NOTE:

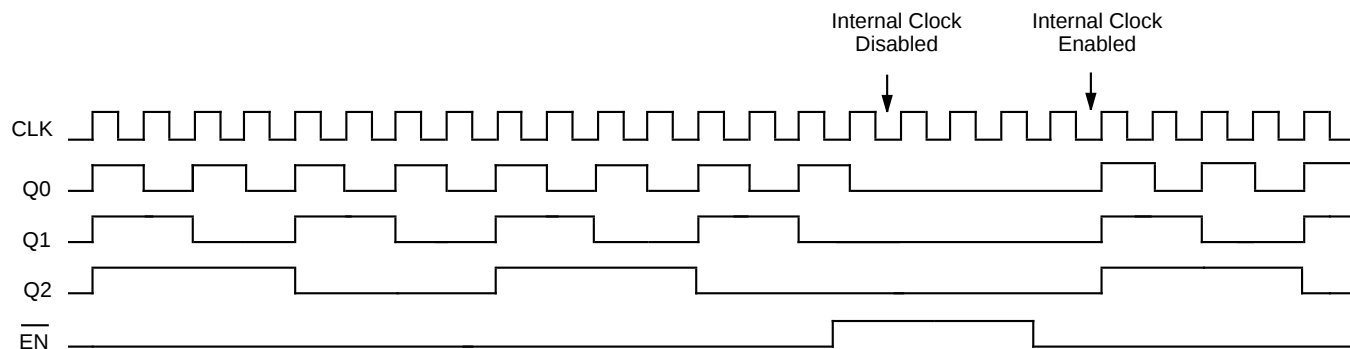
1. Parametric values specified at:
- | | | |
|---------------------------|---------------------|------------------|
| 5 volt Power Supply Range | 100EL34 Series: | -4.2V to -5.5V. |
| | 10EL34 Series | -4.75V to -5.5V. |
| 3 volt Power Supply Range | 10/100EL34L Series: | -3.0V to -3.8V. |

AC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

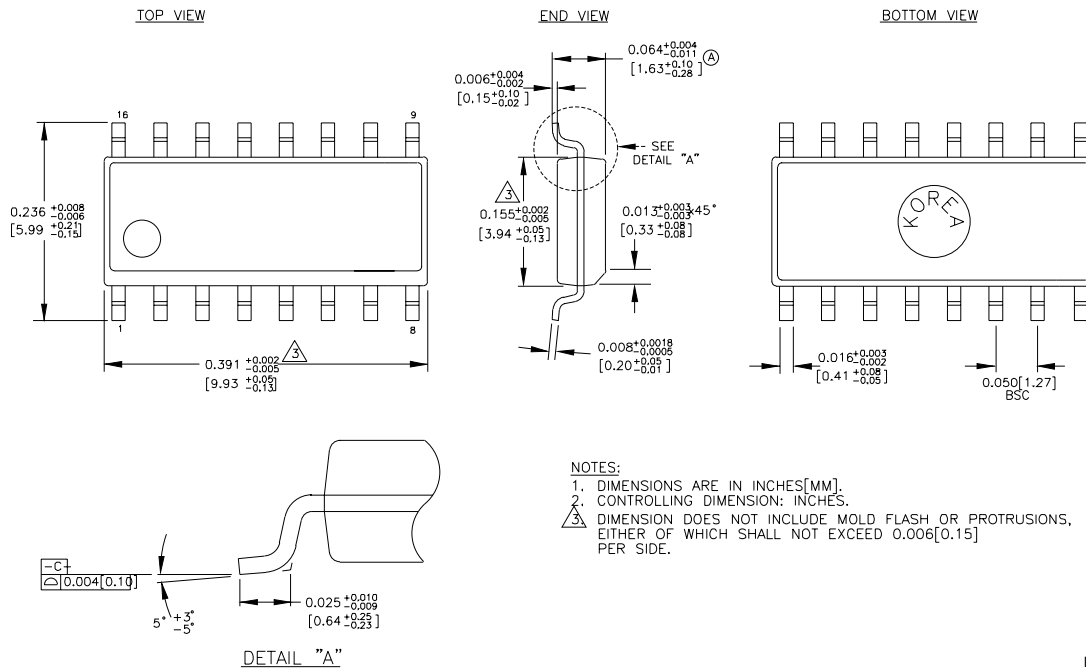
Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PD}	Propagation Delay to Output	960	1100	1200	960	1100	1200	960	1100	1200	960	1100	1200	ps
	CLK	650	800	1010	650	800	1010	650	800	1010	650	800	1010	
	MR	650	800	1010	650	800	1010	650	800	1010	650	800	1010	ps
t _{skew}	Within-Device Skew ⁽²⁾	—	—	50	—	—	50	—	—	50	—	—	50	
t _s	Set-up Time $\overline{EN}$	400	—	—	400	—	—	400	—	—	400	—	—	ps
t _H	Hold Time $\overline{EN}$	200	—	—	200	—	—	200	—	—	200	—	—	ps
V _{PP}	Minimum Input Swing ⁽³⁾	250	—	—	250	—	—	250	—	—	250	—	—	mV
V _{CMR}	Common Mode Range ⁽⁴⁾	-1.3	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	V
t _r	Output Rise/Fall Times	275	400	525	275	400	525	275	400	525	275	400	525	ps
t _f	Q (20% – 80%)	275	400	525	275	400	525	275	400	525	275	400	525	

NOTES:

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- | | | |
|---------------------------|---------------------|------------------|
| 5 volt Power Supply Range | 100EL34 Series: | -4.2V to -5.5V. |
| | 10EL34 Series | -4.75V to -5.5V. |
| 3 volt Power Supply Range | 10/100EL34L Series: | -3.0V to -3.8V. |
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – IV_{CMR} (min)I.

TIMING DIAGRAM

The $\overline{\text{EN}}$ signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{\text{EN}}$ signal not been asserted.

16-PIN SOIC .150" WIDE (Z16-2)

Rev. 02

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