Data Sheet | April 14, 2006 | FN8102.3

2-Wire™ RTC Real Time Clock/Calendar/CPU Supervisor with EEPROM

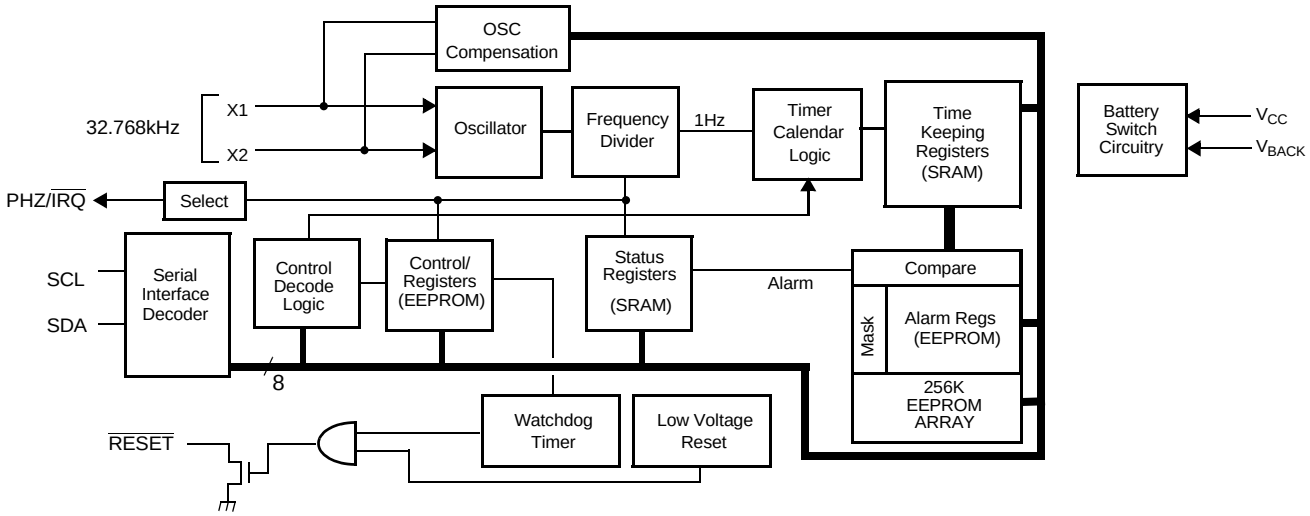
FEATURES

- Real Time Clock/Calendar
  - —Tracks time in Hours, Minutes, Seconds and Hundredths of a Second
  - —Day of the Week, Day, Month, and Year
- 2 Polled Alarms (Non-volatile)
  - —Settable on the Second, Minute, Hour, Day of the Week, Day, or Month
  - —Repeat Mode (periodic interrupts)
- Oscillator Compensation on Chip
  - —Internal feedback resistor and compensation capacitors
  - —64 position Digitally Controlled Trim Capacitor
  - —6 digital-frequency adjustment setting to ±30ppm
- CPU Supervisor Functions
  - —Power-on Reset, Low Voltage Sense
  - —Watchdog Timer (SW Selectable: 0.25s, 0.75s, 1.75s, off)
- Battery Switch or Super Cap Input
- 32K x 8 Bits of EEPROM
  - —128-Byte Page Write Mode
  - —8 modes of Block Lock™ Protection
  - —Single Byte Write Capability
- High Reliability
  - —Data Retention: 100 years
  - —Endurance: 100,000 cycles per byte
- 2-Wire™ Interface interoperable with I2C*
  - —400kHz data transfer rate
- Frequency Output (SW Selectable: Off, 1Hz, 100Hz, or 32.768kHz)
- Low Power CMOS
  - —1.25µA Operating Current (Typical)
- Small Package Options
  - —16-Lead SOIC and 14-Lead TSSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

APPLICATIONS

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

BLOCK DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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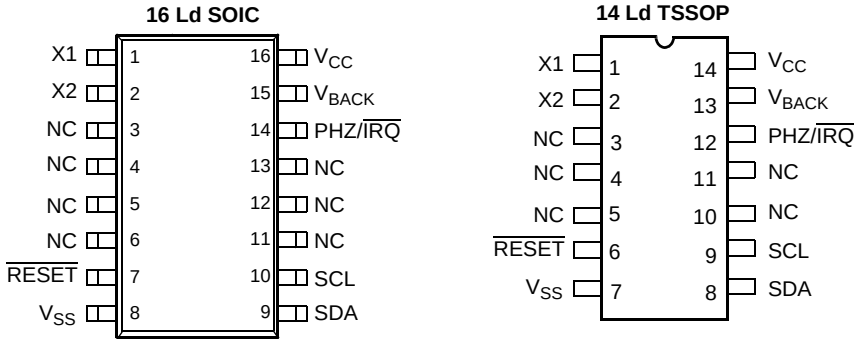
PIN DESCRIPTIONS



NC = No internal connection

Ordering Information

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE	OPERATING TEMP RANGE (°C)	PACKAGE
X1288S16-4.5A*	X1288S AL	4.5 to 5.5	4.63V±112mV	0 to 70	16 Ld SOIC
X1288S16I-4.5A*	X1288S AM			-40 to +85	16 Ld SOIC
X1288V14-4.5A*	X1288V AL			0 to 70	14 Ld TSSOP
X1288V14Z-4.5A* (Note)	X1288V ZAL			0 to 70	14 Ld TSSOP (Pb-free)
X1288V14I-4.5A*	X1288V AM			-40 to +85	14 Ld TSSOP
X1288V14IZ-4.5A* (Note)	X1288V ZAM			-40 to +85	14 Ld TSSOP (Pb-free)
X1288S16*	X1288S		4.38V±112mV	0 to 70	16 Ld SOIC
X1288S16I*	X1288S I			-40 to +85	16 Ld SOIC
X1288V14*	X1288V			0 to 70	14 Ld TSSOP
X1288V14Z* (Note)	X1288V Z			0 to 70	14 Ld TSSOP (Pb-free)
X1288V14I*	X1288V I			-40 to +85	14 Ld TSSOP
X1288V14IZ* (Note)	X1288V ZI			-40 to +85	14 Ld TSSOP (Pb-free)
X1288S16-2.7A*	X1288S AN	2.7 to 5.5	2.85V±100mV	0 to 70	16 Ld SOIC
X1288S16I-2.7A*	X1288S AP			-40 to +85	16 Ld SOIC
X1288V14-2.7A*	X1288V AN			0 to 70	14 Ld TSSOP
X1288V14Z-2.7A* (Note)	X1288V ZAN			0 to 70	14 Ld TSSOP (Pb-free)
X1288V14I-2.7A*	X1288V AP			-40 to +85	14 Ld TSSOP
X1288V14IZ-2.7A* (Note)	X1288V ZAP			-40 to +85	14 Ld TSSOP (Pb-free)
X1288S16-2.7*	X1288S F		2.65V±100mV	0 to 70	16 Ld SOIC
X1288S16I-2.7*	X1288S G			-40 to +85	16 Ld SOIC
X1288V14-2.7*	X1288V F			0 to 70	14 Ld TSSOP
X1288V14Z-2.7* (Note)	X1288V ZF			0 to 70	14 Ld TSSOP (Pb-free)
X1288V14I-2.7*	X1288V G			-40 to +85	14 Ld TSSOP
X1288V14IZ-2.7* (Note)	X1288V ZG			-40 to +85	14 Ld TSSOP (Pb-free)

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN ASSIGNMENTS

Pin Number		Symbol	Brief Description
SOIC	TSSOP		
1	1	X1	**X1.** The X1 pin is the input of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1288 to supply a timebase for the real time clock. The recommended crystal is a Citizen CFS206-32.768KDZF. Internal compensation circuitry is included to form a complete oscillator circuit. Care should be taken in the placement of the crystal and the layout of the circuit. Plenty of ground plane around the device and short traces to X1 are highly recommended. See Application section for more information.
2	2	X2	**X2.** The X2 pin is the output of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1288 to supply a timebase for the real time clock. The recommended crystal is a Citizen CFS206-32.768KDZF. Internal compensation circuitry is included to form a complete oscillator circuit. Care should be taken in the placement of the crystal and the layout of the circuit. Plenty of ground plane around the device and short traces to X2 are highly recommended. See Application section for more information.
7	6	$\overline{\text{RESET}}$	**RESET Output – $\overline{\text{RESET}}$.** This is a reset signal output. This signal notifies a host processor that the watchdog time period has expired or that the voltage has dropped below a fixed V_{TRIP} threshold. It is an open drain active LOW output. Recommended value for the pullup resistor is 5kΩ. If unused, tie to ground.
8	7	V_{SS}	**V_{SS}.**
9	8	SDA	**Serial Data (SDA).** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated). An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire interface speed.
10	9	SCL	**Serial Clock (SCL).** The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated).
14	12	PHZ/$\overline{\text{IRQ}}$	**Programmable Frequency/Interrupt Output – PHZ/$\overline{\text{IRQ}}$.** This is either an output from the internal oscillator or an interrupt signal output. It is a CMOS output. When used as frequency output, this signal has a frequency of 32.768kHz, 100Hz, 1Hz or inactive. When used as interrupt output, this signal notifies a host processor that an alarm has occurred and an action is required. It is an active LOW output. The control bits for this function are FO1 and FO0 and are found in address 0011h of the Clock Control Memory map. See “Programmable Frequency Output Bits - FO1, FO0” on page 13.
15	13	V_{BACK}	**V_{BACK}.** This input provides a backup supply voltage to the device. V_{BACK} supplies power to the device in the event the V_{CC} supply fails. This pin can be connected to a battery, a Supercap or tied to ground if not used.
16	14	V_{CC}	**V_{CC}.**

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on V_{CC}, V_{BACK} and PHZ/$\overline{IRQ}$ pin (respect to ground) .....-0.5V to 7.0V
Voltage on SCL, SDA, X1 and X2 pin (respect to ground) ..... -0.5V to 7.0V or 0.5V above V_{CC} or V_{BACK} (whichever is higher)
DC Output Current .....5 mA
Lead Temperature (Soldering, 10 sec)..... 300°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS (Temperature = -40°C to +85°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{CC}	Main Power Supply		2.7		5.5	V	
V_{BACK}	Backup Power Supply		1.8		5.5	V	
V_{CB}	Switch to Backup Supply		V_{BACK} -0.2		V_{BACK} -0.1	V	
V_{BC}	Switch to Main Supply		V_{BACK}		V_{BACK} +0.2	V	

OPERATING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
I_{CC1}	Read Active Supply Current	V_{CC} = 2.7V			400	µA	1, 5, 7, 14
		V_{CC} = 5.0V			800	µA	
I_{CC2}	Program Supply Current (nonvolatile)	V_{CC} = 2.7V			2.5	mA	2, 5, 7, 14
		V_{CC} = 5.0V			3.0	mA	
I_{CC3}	Main Timekeeping Current	V_{CC} = 2.7V			10	µA	3, 7, 8, 14, 15
		V_{CC} = 5.0V			20	µA	
I_{BACK}	Timekeeping Current – (Low Voltage Sense and Watchdog Timer disabled	V_{BACK} = 1.8V		1.25		µA	3, 6, 9, 14, 15 “See Performance Data”
		V_{BACK} = 3.3V		1.5		µA	
I_{LI}	Input Leakage Current				10	µA	10
I_{LO}	Output Leakage Current				10	µA	10
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.2 or V_{BACK} x 0.2	V	13
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7 or V_{BACK} x 0.7		V_{CC} + 0.5 or V_{BACK} + 0.5	V	13
V_{HYS}	Schmitt Trigger Input Hysteresis	V_{CC} related level	.05 x V_{CC} or .05 x V_{BACK}			V	13
V_{OL1}	Output LOW Voltage for SDA and $\overline{RESET}$	V_{CC} = 2.7V			0.4	V	11
		V_{CC} = 5.5V			0.4		
V_{OL2}	Output LOW Voltage for PHZ/$\overline{IRQ}$	V_{CC} = 2.7V			V_{CC} x 0.3	V	11
		V_{CC} = 5.5V			V_{CC} x 0.3		
V_{OH2}	Output HIGH Voltage for PHZ/$\overline{IRQ}$	V_{CC} = 2.7V	V_{CC} x 0.7			V	12
		V_{CC} = 5.5V	V_{CC} x 0.7				

Notes: (1) The device enters the Active state after any start, and remains active: for 9 clock cycles if the Device Select Bits in the Slave Address Byte are incorrect or until 200nS after a stop ending a read or write operation.
(2) The device enters the Program state 200nS after a stop ending a write operation and continues for t_{WC}.

(3) The device goes into the Timekeeping state 200nS after any stop, except those that initiate a nonvolatile write cycle; t_{WC} after a stop that initiates a nonvolatile write cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(4) For reference only and not tested.
(5) $V_{IL} = V_{CC} \times 0.1$, $V_{IH} = V_{CC} \times 0.9$, $f_{SCL} = 400KHz$
(6) $V_{CC} = 0V$
(7) $V_{BACK} = 0V$
(8) $V_{SDA} = V_{SCL} = V_{CC}$, Others = GND or V_{CC}
(9) $V_{SDA} = V_{SCL} = V_{BACK}$, Others = GND or V_{BACK}
(10) V_{SDA} = GND or V_{CC}, V_{SCL} = GND or V_{CC}, $V_{\overline{RESET}}$ = GND or V_{CC}
(11) $I_{OL} = 3.0mA$ at 5.5V, 1.5mA at 2.7V
(12) $I_{OH} = -1.0mA$ at 5.5V, -0.4mA at 2.7V
(13) Threshold voltages based on the higher of Vcc or Vback.
(14) Using recommended crystal and oscillator network applied to X1 and X2 (25°C).
(15) Typical values are for $T_A = 25°C$

Capacitance $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
C_{OUT}(1)	Output Capacitance (SDA, PHZ/$\overline{IRQ}$, $\overline{RESET}$)	10	pF	$V_{OUT} = 0V$
C_{IN}(1)	Input Capacitance (SCL)	10	pF	$V_{IN} = 0V$

Notes: (1) This parameter is not 100% tested.
(2) The input capacitance between x1 and x2 pins can be varied between 5pF and 19.75pF by using analog trimming registers

AC CHARACTERISTICS

AC Test Conditions

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	Standard Output Load

Equivalent AC Output Load Circuit for $V_{CC} = 5V$

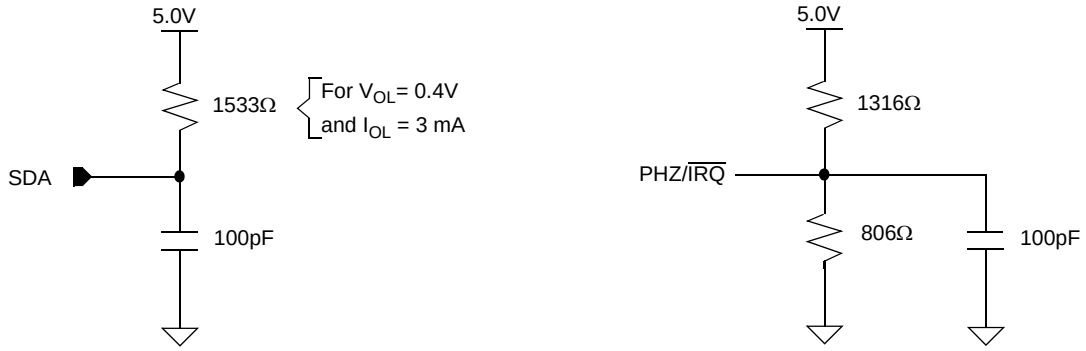


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH $V_{CC} = 5.0V$

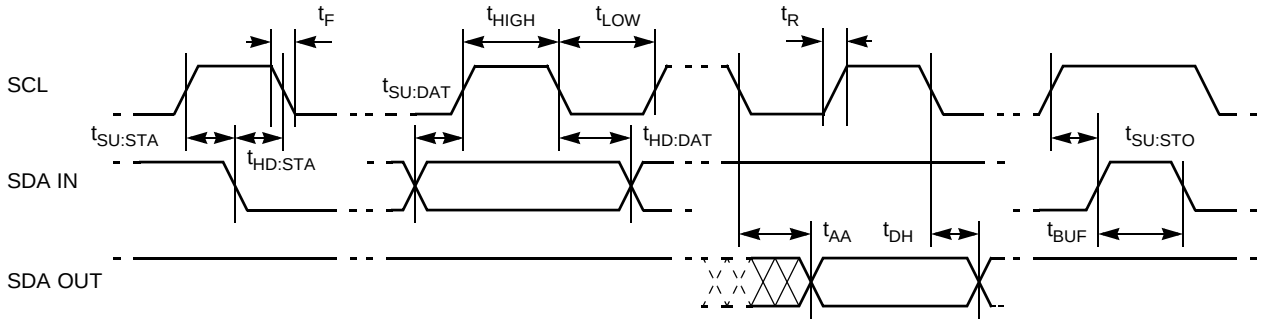
AC Specifications (T_A = -40°C to +85°C, VCC = +2.7V to +5.5V, unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency		400	kHz
t_{IN}	Pulse width Suppression Time at inputs	50(1)		ns
t_{AA}	SCL LOW to SDA Data Out Valid		0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Output Hold Time	50		ns
t_R	SDA and SCL Rise Time	20 +.1Cb(1)(2)	300	ns
t_F	SDA and SCL Fall Time	20 +.1Cb(1)(2)	300	ns
Cb	Capacitive load for each bus line		400	pF

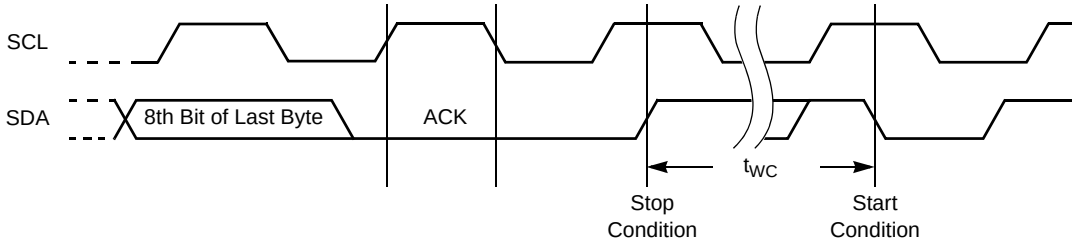
Notes: (1) This parameter is not 100% tested.
(2) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

Bus Timing



Write Cycle Timing



Power-up Timing

Symbol	Parameter	Min.	Typ.(2)	Max.	Units
t_{PUR}(1)	Time from Power-up to Read			1	ms
t_{PUW}(1)	Time from Power-up to Write			5	ms

Notes: (1) Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are not 100% tested. V_{CC} slew rate should be between 0.2mV/µsec and 50mV/µsec.
(2) Typical values are for T_A = 25°C and V_{CC} = 5.0V

Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(1)	Write Cycle Time		5	10	ms

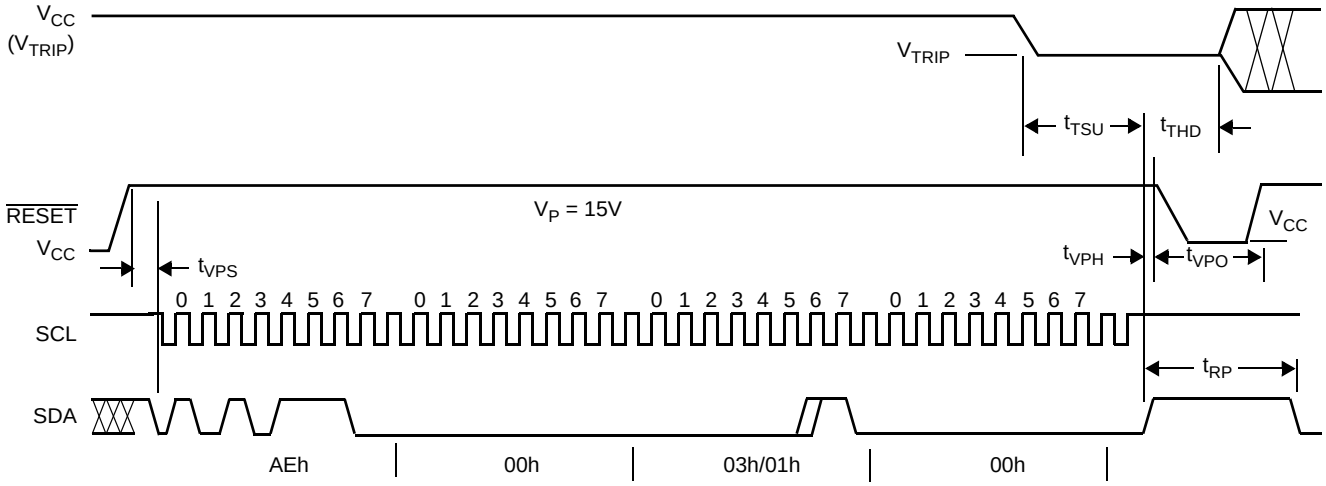
Note: (1) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

WATCHDOG TIMER/LOW VOLTAGE RESET OPERATING CHARACTERISTICS

Watchdog/Low Voltage Reset Parameters (See Figures 3 and 4)

Symbols	Parameters	Min.	Typ.	Max.	Unit
V_{PTRIP}	Programmed Reset Trip Voltage X1288-4.5A X1288 X1288-2.7A X1288-2.7	 4.50 4.25 2.75 2.55	 4.63 4.38 2.85 2.65	 4.75 4.50 2.95 2.75	V
t_{RPD}	V_{CC} Detect to $\overline{RESET}$ LOW			500	ns
t_{PURST}	Power-up Reset Time-out Delay	100	250	400	ms
t_F	V_{CC} Fall Time	10			µs
t_R	V_{CC} Rise Time	10			µs
t_{WDO}	Watchdog Timer Period (Crystal=32.768kHz): WD1=0, WD0=0, (default) WD1=0, WD0=1 WD1=1, WD0=0	 1.7 725 225	 1.75 750 250	 1.8 775 275	 s ms ms
t_{RST}	Watchdog Reset Time-out Delay (Crystal=32.768kHz)	225	250	275	ms
t_{RSP}	2-Wire interface	1			µs
V_{RVALID}	Reset Valid V_{CC}	1.0			V

V_{TRIP} Programming Timing Diagram



V_{TRIP} Programming Parameters

Parameter	Description	Min.	Max.	Units
t_{VPS}	V_{TRIP} Program Enable Voltage Setup time	1		µs
t_{VPH}	V_{TRIP} Program Enable Voltage Hold time	1		µs
t_{TSU}	V_{TRIP} Setup time	1		µs
t_{THD}	V_{TRIP} Hold (stable) time	10		ms
t_{VPO}	V_{TRIP} Program Enable Voltage Off time (Between successive adjustments)	0		µs
t_{RP}	V_{TRIP} Program Recovery Period (Between successive adjustments)	10		ms
V_P	Programming Voltage	14	16	V
V_{TRAN}	V_{TRIP} Programmed Voltage Range	1.7	5.0	V
V_{tv}	V_{TRIP} Program variation after programming (Programmed at 25°C)	-25	+25	mV

V_{TRIP} programming parameters are not 100% Tested.

DESCRIPTION

The X1288 device is a Real Time Clock with clock/calendar, two polled alarms with integrated 32kx8 EEPROM, oscillator compensation, CPU Supervisor (POR/LVS and WDT) and battery backup switch.

The oscillator uses an external, low-cost 32.768kHz crystal. All compensation and trim components are integrated on the chip. This eliminates several external discrete components and a trim capacitor, saving board area and component cost.

The Real-Time Clock keeps track of time with separate registers for Hours, Minutes, Seconds and 1/100 of a second. The Calendar has separate registers for Date, Month, Year and Day-of-week. The calendar is correct through 2099, with automatic leap year correction.

The powerful Dual Alarms can be set to any Clock/Calendar value for a match. For instance, every minute, every Tuesday, or 5:23 AM on March 21. The alarms can be polled in the Status Register or provide a hardware interrupt ($\overline{IRQ}$ Pin). There is a repeat mode for the alarms allowing a periodic interrupt.

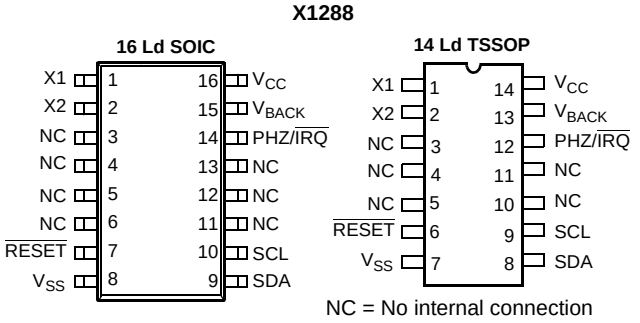
The PHZ/$\overline{IRQ}$ pin may be software selected to provide a frequency output of 1 Hz, 100 Hz, or 32,768 Hz.

The X1288 device integrates CPU Supervisor func-tions and a Battery Switch. There is a Power-On Reset (RESET output) with typically 250 ms delay from power-on. It will also assert RESET when Vcc goes below the specified threshold. The Vtrip threshold is user repro-grammable. There is a WatchDog Timer (WDT) with 3 selectable time-out periods (0.25s, 0.75s, 1.75s) and a disabled setting. The watchdog activates the $\overline{RESET}$ pin when it expires.

The device offers a backup power input pin. This V_{BACK} pin allows the device to be backed up by battery or SuperCap. The entire X1288 device is fully operational from 2.7 to 5.5 volts and the clock/calendar portion of the X1288 device remains fully operational down to 1.8 volts (Standby Mode).

The X1288 device provides 256K bits of EEPROM with 8 modes of BlockLock™ control. The BlockLock allows a safe, secure memory for critical user and configuration data, while allowing a large user storage area.

PIN DESCRIPTIONS



NC = No internal connection

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated).

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated).

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire interface speed.

V_{BACK}

This input provides a backup supply voltage to the device. V_{BACK} supplies power to the device in the event the V_{CC} supply fails. This pin can be connected to a battery, a Supercap or tied to ground if not used.

RESET Output – $\overline{RESET}$

This is a reset signal output. This signal notifies a host processor that the watchdog time period has expired or that the voltage has dropped below a fixed V_{TRIP} threshold. It is an open drain active LOW output. Recommended value for the pullup resistor is 5kΩ. If unused, tie to ground.

Programmable Frequency/Interrupt Output – PHZ/$\overline{IRQ}$

This is either an output from the internal oscillator or an interrupt signal output. It is a CMOS output.

When used as frequency output, this signal has a frequency of 32.768kHz, 100Hz, 1Hz or inactive.

When used as interrupt output, this signal notifies a host processor that an alarm has occurred and an action is required. It is an active LOW output.

The control bits for this function are FO1 and FO0 and are found in address 0011h of the Clock Control Memory map. See “Programmable Frequency Output Bits - FO1, FO0” on page 13.

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the X1288 to supply a timebase for the real time clock. The recommended crystal is a Citizen CFS206-32.768KDZF. Internal compensation circuitry is included to form a complete oscillator circuit. Care should be taken in the placement of the crystal and the layout of the circuit. Plenty of ground plane around the device and short traces to X1 and X2 are highly recommended. See Application section for more information.

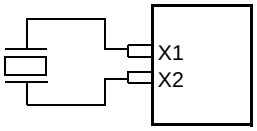


FIGURE 2. RECOMMENDED CRYSTAL CONNECTION

POWER CONTROL OPERATION

The power control circuit accepts a V_{CC} and a V_{BACK} input. The power control circuit powers the clock from V_{BACK} when $V_{CC} < V_{BACK}$ - 0.2V. It will switch back to power the device from V_{CC} when V_{CC} exceeds V_{BACK}.

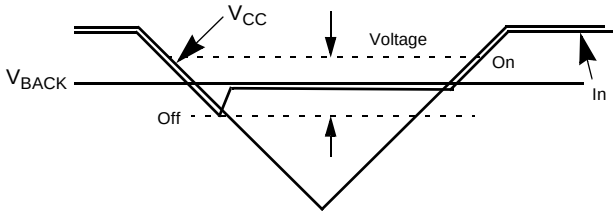


FIGURE 3. POWER CONTROL

REAL TIME CLOCK OPERATION

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of the 1/100 of a second, second, minute, hour, day, date, month, and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the X1288 powers up after the loss of both V_{CC} and V_{BACK}, the clock will not operate until at least one byte is written to the clock register.

Reading the Real Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the Real Time Clock. The RTC Registers can then be read in a Sequential Read Mode. Since the clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock could change during the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

Writing to the Real Time Clock

The time and date may be set by writing to the RTC registers. To avoid changing the current time by an uncompleted write operation, the current time value is loaded into a separate buffer at the falling edge of the clock on the ACK bit before the RTC data input bytes, the clock continues to run. The new serial input data replaces the values in the buffer. This new RTC value is loaded back into the RTC Register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation the RTC will reflect the newly loaded data beginning with the SSEC register reset to “0” at the next sub-second update after the stop bit is written. The 1Hz frequency output from the PHZ/$\overline{IRQ}$ pin will be reset to restart after the stop bit is written. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any nonvolatile write sequences. A single byte may be written to the RTC without affecting the other bytes.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal’s nominal frequency. For example, a >20ppm frequency deviation translates into an accuracy of >1 minute per month. these parameters are available from the crystal manufacturer. Intersil’s RTC family provides on-chip crystal compensation networks to adjust load-capacitance to tune oscillator frequency from +116 ppm to –37 ppm when using a 12.5 pF load crystal. For more detail information see the Application section.

CLOCK/CONTROL REGISTERS (CCR)

The Control/Clock Registers are located in an area separate from the EEPROM array and are only accessible following a slave byte of “1101111x” and reads or writes to addresses [0000h:003Fh]. The clock/control memory map has memory addresses from 0000h to 003Fh. The defined addresses are described in the Table 1. Writing to and reading from the undefined addresses are not recommended.

CCR Access

The contents of the CCR can be modified by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register), however, the WEL and RWEL bits must be set using a two step process (See section “Writing to the Clock/Control Registers.”)

The CCR is divided into 5 sections. These are:

1. Alarm 0 (8 bytes; non-volatile)
2. Alarm 1 (8 bytes; non-volatile)
3. Control (4 bytes; non-volatile)
4. Real Time Clock (8 bytes; volatile)
5. Status (1 byte; volatile)

Each register is read and written through buffers. The non-volatile portion (or the counter portion of the RTC) is updated only if RWEL is set and only after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. Continued reads or writes, once reaching the end of a section, will wrap around to the start of the section. A read or write can begin at any address in the CCR.

It is not necessary to set the RWEL bit prior to writing the status register. Section 5 supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

The state of the CCR can be read by performing a random read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all Clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read of the CCR will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

Table 1. Clock/Control Memory Map

Addr.	Type	Reg Name	Bit 7	6	5	4	3	2	1	0 (optional)	Range	Default
003F	Status	SR	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF		01h
0037	RTC (SRAM)	SSEC	SS23	SS22	SS21	SS20	SS13	SS12	SS11	SS10	0-99	xxh
0036		DW	0	0	0	0	0	DY2	DY1	DY0	0-6	xxh
0035		YR	Y23	Y22	Y21	Y20	Y13	Y12	Y11	Y10	0-99	xxh
0034		MO	0	0	0	G20	G13	G12	G11	G10	1-12	xxh
0033		DT	0	0	D21	D20	D13	D12	D11	D10	1-31	xxh
0032		HR	MIL	0	H21	H20	H13	H12	H11	H10	0-23	xxh
0031		MN	0	M22	M21	M20	M13	M12	M11	M10	0-59	xxh
0030		SC	0	S22	S21	S20	S13	S12	S11	S10	0-59	xxh
0013	Control (EE-PROM)	DTR	0	0	0	0	0	DTR2	DTR1	DTR0		00h
0012		ATR	0	0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0		00h
0011		INT	IM	AL1E	AL0E	FO1	FO0	Read Only	Read Only	Read Only		00h
0010		BL	BP2	BP1	BP0	WD1	WD0	Read Only	Read Only	Read Only		18h
000F	Alarm1 (EEPROM)	Y2K1	Read-only - Default = 20h								20	20h
000E		DWA1	EDW1	0	0	0	0	DY2	DY1	DY0	0-6	00h
000D		YRA1	Unused - Default = RTC Year value (No EEPROM) - Future expansion									
000C		MOA1	EMO1	0	0	A1G20	A1G13	A1G12	A1G11	A1G10	1-12	00h
000B		DTA1	EDT1	0	A1D21	A1D20	A1D13	A1D12	A1D11	A1D10	1-31	00h
000A		HRA1	EHR1	0	A1H21	A1H20	A1H13	A1H12	A1H11	A1H10	0-23	00h
0009		MNA1	EMN1	A1M22	A1M21	A1M20	A1M13	A1M12	A1M11	A1M10	0-59	00h
0008		SCA1	ESC1	A1S22	A1S21	A1S20	A1S13	A1S12	A1S11	A1S10	0-59	00h
0007	Alarm0 (EEPROM)	Y2K0	Read-only - Default = 20h								20	20h
0006		DWA0	EDW0	0	0	0	0	DY2	DY1	DY0	0-6	00h
0005		YRA0	Unused - Default = RTC Year value (No EEPROM) – Future expansion									
0004		MOA0	EMO0	0	0	A0G20	A0G13	A0G12	A0G11	A0G10	1-12	00h
0003		DTA0	EDT0	0	A0D21	A0D20	A0D13	A0D12	A0D11	A0D10	1-31	00h
0002		HRA0	EHR0	0	A0H21	A0H20	A0H13	A0H12	A0H11	A0H10	0-23	00h
0001		MNA0	EMN0	A0M22	A0M21	A0M20	A0M13	A0M12	A0M11	A0M10	0-59	00h
0000		SCA0	ESC0	A0S22	A0S21	A0S20	A0S13	A0S12	A0S11	A0S10	0-59	00h

ALARM REGISTERS

There are two alarm registers whose contents mimic the contents of the RTC register, but add enable bits and exclude the 24 hour time selection bit. The enable bits specify which registers to use in the comparison between the Alarm and Real Time Registers. For example:

– Setting the Enable Month bit (EMOn*) bit in combination with other enable bits and a specific alarm time, the user can establish an alarm that triggers at the same time once a year.

*n = 0 for Alarm 0: N = 1 for Alarm 1

When there is a match, an alarm flag is set. The occurrence of an alarm can be determined by polling the AL0 and AL1 bits or by enabling the $\overline{IRQ}$ output, using it as hardware flag.

The alarm enable bits are located in the MSB of the particular register. When all enable bits are set to ‘0’, there are no alarms.

– The user can set the X1288 to alarm every Wednesday at 8:00 AM by setting the EDWn*, the EHRn* and EMNn* enable bits to ‘1’ and setting the DWAn*, HRAn* and MNAn* Alarm registers to 8:00 AM Wednesday.

– A daily alarm for 9:30PM results when the EHRn* and EMNn* enable bits are set to ‘1’ and the HRAn* and MNAn* registers are set to 9:30 PM.

*n = 0 for Alarm 0: N = 1 for Alarm 1

REAL TIME CLOCK REGISTERS

Clock/Calendar Registers (SSEC, SC, MN, HR, DT, MO, YR)

These registers depict BCD representations of the time. As such, SSEC (1/100 Second) range from 00 to 99, SC (Seconds) and MN (Minutes) range from 00 to 59, HR (Hour) is 1 to 12 with an AM or PM indicator

(H21 bit) or 0 to 23 (with MIL=1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99. The SSEC register is read-only.

Date of the Week Register (DW)

This register provides a Day of the Week status and uses three bits DY2 to DY0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as ‘0’.

24 Hour Time

If the MIL bit of the HR register is 1, the RTC uses a 24-hour format. If the MIL bit is 0, the RTC uses a 12-hour format and H21 bit functions as an AM/PM indicator with a ‘1’ representing PM. The clock defaults to standard time with H21=0.

Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The X1288 does not correct for the leap year in the year 2100.

STATUS REGISTER (SR)

The Status Register is located in the CCR memory map at address 003Fh. This is a volatile register only and is used to control the WEL and RWEL write enable latches, read two power status and two alarm bits. This register is separate from both the array and the Clock/Control Registers (CCR).

Table 2. Status Register (SR)

Addr	7	6	5	4	3	2	1	0
003Fh	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF
Default	0	0	0	0	0	0	0	1

BAT: Battery Supply - Volatile

This bit set to “1” indicates that the device is operating from V_{BACK}, not V_{CC}. It is a read-only bit and is set/reset by hardware (X1288 internally). Once the device begins operating from V_{CC}, the device sets this bit to “0”.

AL1, AL0: Alarm Bits - Volatile

These bits announce if either alarm 0 or alarm 1 match the real time clock. If there is a match, the respective bit is set to ‘1’. The falling edge of the last data bit in a SR Read operation resets the flags. Note: Only the AL bits that are set when an SR read starts will be reset. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

RWEL: Register Write Enable Latch - Volatile

This bit is a volatile latch that powers up in the LOW (disabled) state. The RWEL bit must be set to “1” prior to any writes to the Clock/Control Registers. Writes to RWEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition. A write to the CCR requires both the RWEL and WEL bits to be set in a specific sequence.

WEL: Write Enable Latch - Volatile

The WEL bit controls the access to the CCR and memory array during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to the CCR or any array address will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the Status Register. Once set, WEL remains set until either reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again. Writes to WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

RTCF: Real Time Clock Fail Bit - Volatile

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL1288 internally) when the device powers up after having lost all power to the device (both V_{CC} and V_{BACK} go to 0V). The bit is set regardless of whether V_{CC} or V_{BACK} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. On power up after a total power failure, all registers are set to their default states and the clock will not increment until at least one byte is written to the clock register. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

Unused Bits:

This device does not use bits 3 or 4 in the SR, but must have a zero in these bit positions. The Data Byte output during a SR read will contain zeros in these bit locations.

CONTROL REGISTERS

The Control Bits and Registers, described under this section, are nonvolatile.

Block Protect Bits - BP2, BP1, BP0

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array. The partitions are described in Table 3.

Watchdog Timer Control Bits - WD1, WD0

The bits WD1 and WD0 control the period of the Watchdog Timer. See Table 4 for options.

Table 3. Block Protect Bits

BP2	BP1	BP0	Protected Addresses X1288	Array Lock
0	0	0	None	None (default)
0	0	1	6000h – 7FFFh	Upper 1/4
0	1	0	4000h – 7FFFh	Upper 1/2
0	1	1	0000h – 7FFFh	Full Array
1	0	0	0000h – 007Fh	First Page
1	0	1	0000h – 00FFh	First 2 pgs
1	1	0	0000h – 01FFh	First 4 pgs
1	1	1	0000h – 03FFh	First 8 Pgs

Table 4. Watchdog Timer Time-Out Options

WD1	WD0	Watchdog Time-Out Period
0	0	1.75 seconds
0	1	750 milliseconds
1	0	250 milliseconds
1	1	Disabled (default)

INTERRUPT CONTROL AND FREQUENCY OUTPUT REGISTER (INT)

Interrupt Control and Status Bits (IM, AL1E, AL0E)

There are two Interrupt Control bits, Alarm 1 Interrupt Enable (AL1E) and Alarm 0 Interrupt Enable (AL0E) to specifically enable or disable the alarm interrupt signal output ($\overline{IRQ}$). The interrupts are enabled when either AL1E and AL0E are set to '1', respectively.

Two volatile bits (AL1 and AL0), associated with the two alarms respectively, indicate if an alarm has happened. These bits are set on an alarm condition regardless of whether the $\overline{IRQ}$ interrupt is enabled. The AL1 and AL0 bits in the status register are reset by the falling edge of the eighth clock of a read of the register containing the bits.

Pulse Interrupt Mode

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence an repetitive or recurring alarm can be set for every n^{th} second, or n^{th} minute, or n^{th} hour, or n^{th} date, or for the same day of the week. The pulsed interrupt mode can be considered a repetitive interrupt mode, with the repetition rate set by the time setting fo the alarm.

The Pulse Interrupt Mode is enabled when the IM bit is set.

IM Bit	Interrupt/Alarm Frequency
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

The Alarm $\overline{IRQ}$ output will output a single pulse of short duration (approximately 10-40ms) once the alarm condition is met. If the interrupt mode bit (IM bit) is set, then this pulse will be periodic.

Programmable Frequency Output Bits - FO1, FO0

These are two output control bits. They select one of three divisions of the internal oscillator, that is applied to the PHZ output pin. Table 5 shows the selection bits for this output. When using the PHZ output function, the Alarm $\overline{IRQ}$ output function is disabled.

Table 5. Programmable Frequency Output Bits

FO1	FO0	Output Frequency (average of 100 samples)
0	0	Alarm $\overline{IRQ}$ output
0	1	32.768kHz
1	0	100Hz
1	1	1Hz

ON-CHIP OSCILLATOR COMPENSATION

Digital Trimming Register (DTR) - DTR2, DTR1 and DTR0 (Non-Volatile)

The digital trimming Bits DTR2, DTR1 and DTR0 adjust the number of counts per second and average the ppm error to achieve better accuracy.

DTR2 is a sign bit. DTR2=0 means frequency compensation is > 0. DTR2=1 means frequency compensation is < 0.

DTR1 and DTR0 are scale bits. DTR1 gives 10 ppm adjustment and DTR0 gives 20 ppm adjustment.

A range from -30ppm to +30ppm can be represented by using three bits above.

Table 6. Digital Trimming Registers

DTR Register			Estimated frequency PPM
DTR2	DTR1	DTR0	
0	0	0	0
0	1	0	+10
0	0	1	+20
0	1	1	+30
1	0	0	0
1	1	0	-10
1	0	1	-20
1	1	1	-30

Analog Trimming Register (ATR) (Non-volatile)

Six analog trimming Bits from **ATR5** to **ATR0** are provided to adjust the on-chip loading capacitance range. The on-chip load capacitance ranges from 3.25pF to 18.75pF. Each bit has a different weight for capacitance adjustment. Using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm range from +116ppm to -37ppm to the nominal frequency compensation. The combination of digital and analog trimming can give up to +146ppm adjustment.

The on-chip capacitance can be calculated as follows:

C_{ATR} = [(ATR value, decimal) x 0.25pF] + 11.0pF

Note that the ATR values are in two's complement, with ATR(000000) = 11.0pF, so the entire range runs from 3.25pF to 18.75pF in 0.25pF steps.

The values calculated above are typical, and total load capacitance seen by the crystal will include approximately 2pF of package and board capacitance in addition to the ATR value.

See Application section and Intersil's Application Note AN154 for more information.

WRITING TO THE CLOCK/CONTROL REGISTERS

Changing any of the nonvolatile bits of the clock/control register requires the following steps:

– Write a 02h to the Status Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop).

– Write a 06h to the Status Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).

– Write one to 8 bytes to the Clock/Control Registers with the desired clock, alarm, or control data. This sequence starts with a start bit, requires a slave byte of "11011110" and an address within the CCR and is terminated by a stop bit. A write to the CCR changes EEPROM values so these initiate a nonvolatile write cycle and will take up to 10ms to complete. Writes to undefined areas have no effect. The RWEL bit is reset by the completion of a nonvolatile write cycle, so the sequence must be repeated to again initiate another change to the CCR contents. If the sequence is not completed for any reason (by sending an incorrect number of bits or sending a start instead of a stop, for example) the RWEL bit is not reset and the device remains in an active mode.

– Writing all zeros to the status register resets both the WEL and RWEL bits.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

POWER-ON RESET

Application of power to the X1288 activates a Power-on Reset Circuit that pulls the $\overline{RESET}$ pin active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

– It prevents communication to the EEPROM, greatly reducing the likelihood of data corruption on power-up.

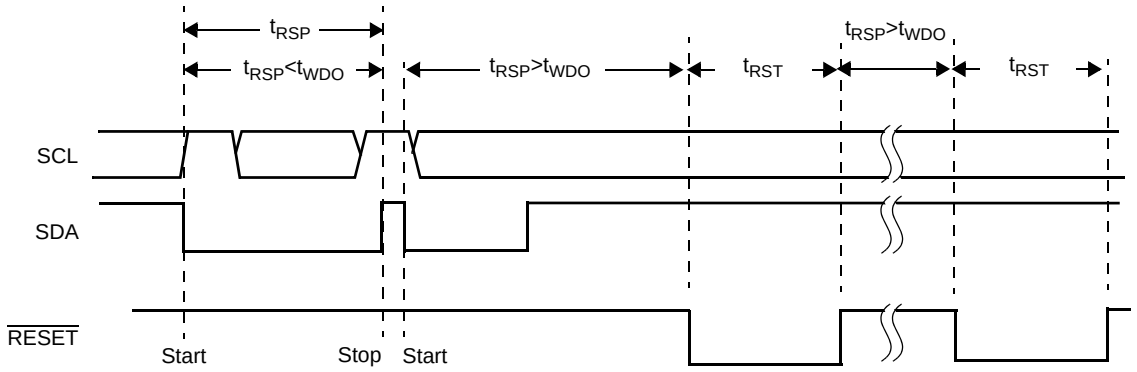
When V_{CC} exceeds the device V_{TRIP} threshold value for typically, 250ms the circuit releases $\overline{RESET}$, allowing the system to begin operation. Recommended V_{CC} slew rate is between 0.2V/ms and 50V/ms.

WATCHDOG TIMER OPERATION

The watchdog timer is selectable. By writing a value to WD1 and WD0, the watchdog timer can be set to 3 different time out periods or off. When the Watchdog timer is set to off, the watchdog circuit is configured for low power operation.

Watchdog Timer Restart

The Watchdog Timer is started by a falling edge of SDA when the SCL line is high and followed by a stop bit. The start signal restarts the watchdog timer counter, resetting the period of the counter back to the maximum. If another start fails to be detected prior to the watchdog timer expiration, then the $\overline{RESET}$ pin becomes active. In the event that the start signal occurs during a reset time out period, the start will have no effect. When using a single START to refresh watchdog timer, a STOP bit should be followed to reset the device back to stand-by mode.



Note: All inputs are ignored during the active reset period (t_{RST}).

FIGURE 4. WATCHDOG RESTART/TIME OUT

LOW VOLTAGE RESET OPERATION

When a power failure occurs, and the voltage to the part drops below a fixed v_{TRIP} voltage, a reset pulse is issued to the host microcontroller. The circuitry monitors the V_{CC} line with a voltage comparator which senses a preset threshold voltage. Power-up and power-down waveforms are shown in Figure 5. The Low Voltage Reset circuit is to be designed so the $\overline{RESET}$ signal is valid down to 1.0V.

When the low voltage reset signal is active, the operation of any in progress nonvolatile write cycle is unaffected, allowing a nonvolatile write to continue as long as possible (down to the power-on reset voltage). The low voltage reset signal, when active, terminates in progress communications to the device and prevents new commands, to reduce the likelihood of data corruption.

V_{CC} THRESHOLD RESET PROCEDURE [Optional]

The X1288 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X1288 threshold may be adjusted. The procedure is described below, and uses the application of a nonvolatile write control signal.

Setting the V_{TRIP} Voltage

It is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the $\overline{RESET}$ pin to the programming voltage V_P. Then write data 00h to address 01h. The stop bit following a valid write operation initiates the V_{TRIP} programming sequence. Bring $\overline{RESET}$ to V_{CC} to complete the operation. **Note:** this operation may take up to 10 milliseconds to complete and also writes 00h to address 01h of the EEPROM array.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP} voltage, apply more than 5.5V to the V_{CC} pin and tie the $\overline{RESET}$ pin to the programming voltage V_P. Then write 00h to address 03h. The stop bit of a valid write operation initiates the V_{TRIP} programming sequence. Bring $\overline{RESET}$ to V_{CC} to complete the operation. **Note:** this operation takes up to 10 milliseconds to complete and also writes 00h to address 03h of the EEPROM array.

For best accuracy in setting V_{TRIP}, it is advised that the following sequence be used.

1. Program V_{TRIP} as above.
2. Measure resulting V_{TRIP} by measuring the V_{CC} value where a $\overline{RESET}$ occurs. Calculate Delta = (Desired – Measured) V_{TRIP} value.
3. Perform a V_{TRIP} program using the following formula to set the voltage of the $\overline{RESET}$ pin:

   $V_{\overline{RESET}}$ = (Desired Value – Delta) + 0.025V

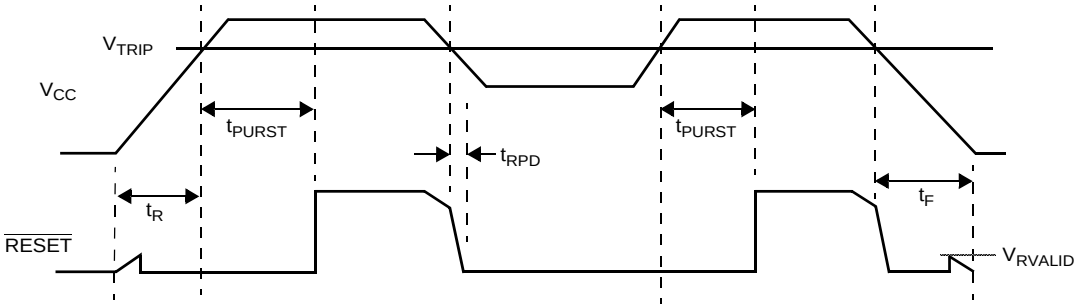
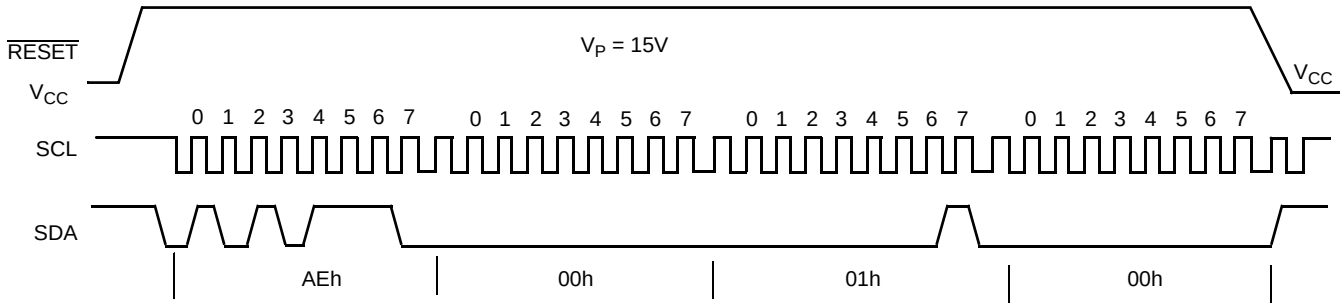
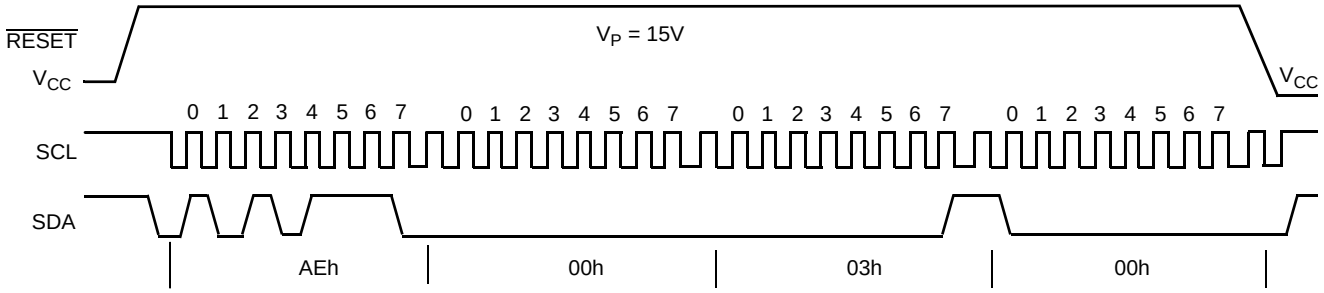


FIGURE 5. POWER-ON RESET AND LOW VOLTAGE RESET



Note: BP0, BP1, BP2 must be disabled.

FIGURE 6. SET V_{TRIP} LEVEL SEQUENCE (V_{CC} = DESIRED V_{TRIP} VALUE)



Note: BP0, BP1, BP2 must be disabled.

FIGURE 7. RESET V_{TRIP} LEVEL SEQUENCE

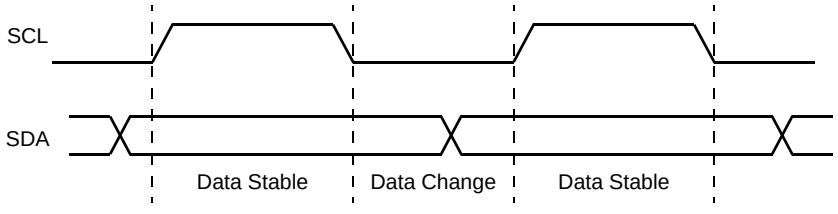


FIGURE 8. VALID DATA CHANGES ON THE SDA BUS

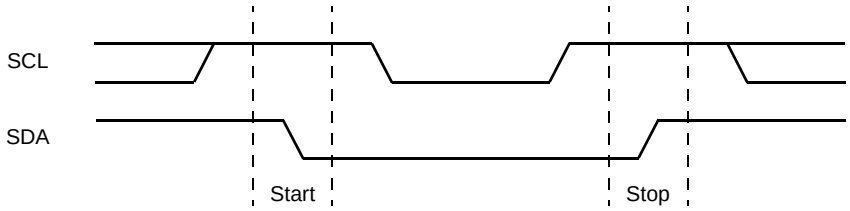


FIGURE 9. VALID START AND STOP CONDITIONS

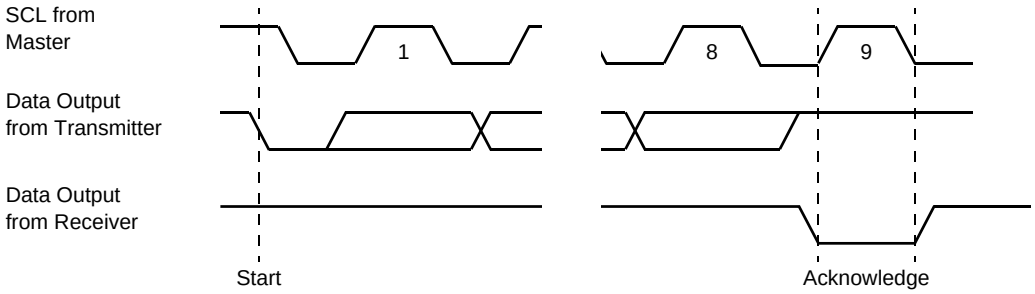


FIGURE 10. ACKNOWLEDGE RESPONSE FROM RECEIVER

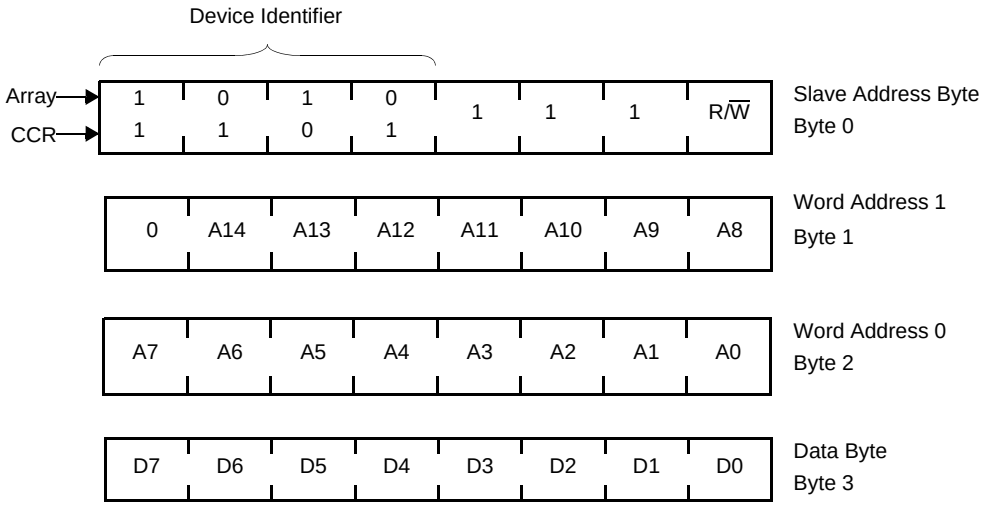


FIGURE 11. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES (128 BYTE PAGES)

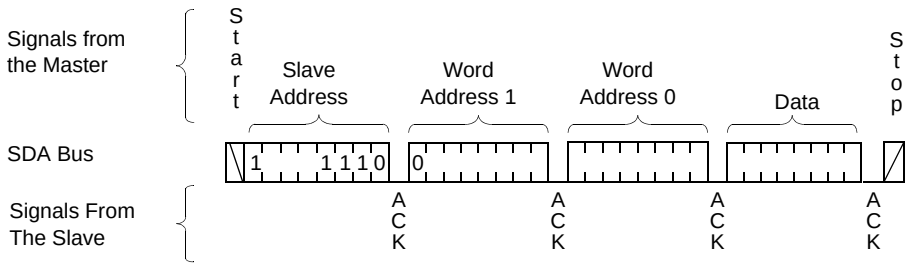


FIGURE 12. BYTE WRITE SEQUENCE

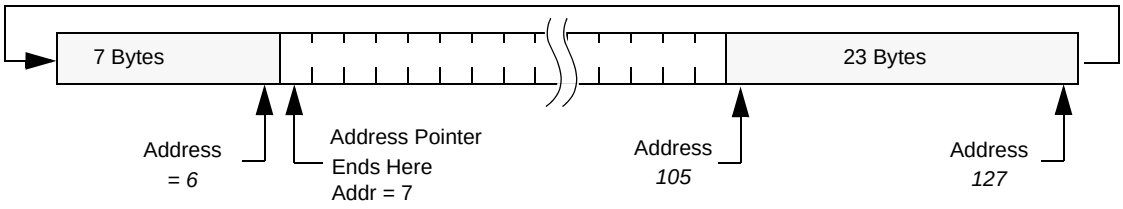


FIGURE 13. WRITING *30* BYTES TO A *128*-BYTE MEMORY PAGE STARTING AT ADDRESS *105*

SERIAL COMMUNICATION

Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 8.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 9.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 9.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 10.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for:

– The Slave Address Byte when the Device Identifier and/or Select bits are incorrect

– All Data Bytes of a write when the WEL in the Write Protect Register is LOW

– The 2nd Data Byte of a Status Register Write Operation (only 1 data byte is allowed)

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device

will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

DEVICE ADDRESSING

Following a start condition, the master must output a Slave Address Byte. The first four bits of the Slave Address Byte specify access to either the EEPROM array or to the CCR. Slave bits '1010' access the EEPROM array. Slave bits '1101' access the CCR.

When shipped from the factory, EEPROM array is UNDEFINED, and should be programmed by the customer to a known state.

Bit 3 through Bit 1 of the slave byte specify the device select bits. These are set to '111'.

The last bit of the Slave Address Byte defines the operation to be performed. When this R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 11.

After loading the entire Slave Address Byte from the SDA bus, the X1288 compares the device identifier and device select bits with '1010111' or '1101111'. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a two byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up the internal address counter is set to address 0h, so a current address read of the EEPROM array starts at address 0. When required, as part of a random read, the master must supply the 2 Word Address Bytes as shown in Figure 11.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. That is if the random read is from the array the slave byte must be 1010111x in both instances. Similarly, for a random read of the Clock/Control Registers, the slave byte must be 1101111x in both places.

Write Operations

Byte Write

For a write operation, the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the array or CCR. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See "Writing to the Clock/Control Registers." Upon receipt of each address byte, the X1288 responds with an acknowledge. After receiving both address bytes the X1288 awaits the eight bits of data. After receiving the 8 data bits, the X1288 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The X1288 then begins an internal write cycle of the data to the nonvolatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 12.

A write to a protected block of memory is ignored, but will still receive an acknowledge. At the end of the write command, the X1288 will not initiate an internal write cycle, and will continue to ACK commands.

Page Write

The X1288 has a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 127 more bytes to the memory array and up to 7 more bytes to the clock/control registers. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See "Writing to the Clock/Control Registers."

After the receipt of each byte, the X1288 responds with an acknowledge, and the address is internally incremented by one. When the counter reaches the end of the page, it "rolls over" and goes back to the first address on the same page. This means that the master can write 128 bytes to a memory array page or 8 bytes to a CCR section starting at any location on that page. For example, if the master begins writing at location 105 of the memory and loads 30 bytes, then the first 23 bytes are written to addresses 105 through 127, and the last 7 bytes are written to columns 0 through 6. Afterwards, the address counter would point to location 7 on the page that was just written. If the master supplies more than the maximum bytes in a page, then the previously loaded data is over written by the new data, one byte at a time. Refer to Figure 13.

The master terminates the Data Byte loading by issuing a stop condition, which causes the X1288 to begin the nonvolatile write cycle. As with the byte write oper-

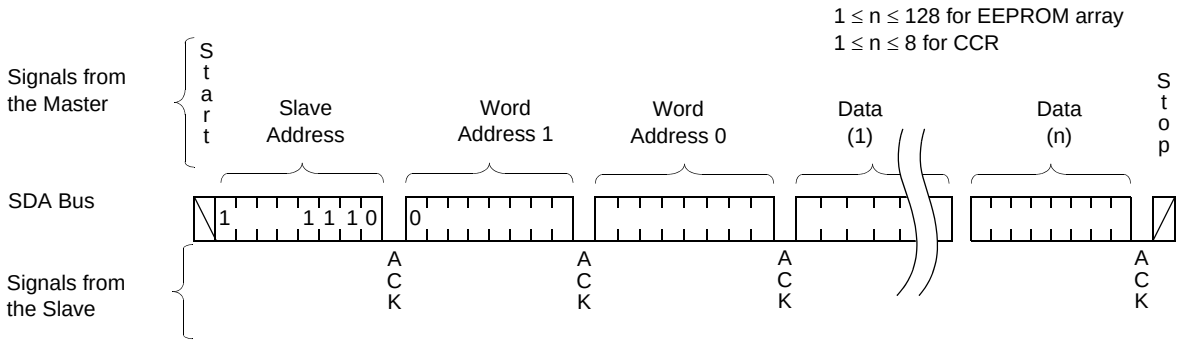


FIGURE 14. PAGE WRITE SEQUENCE

ation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 14 for the address, acknowledge, and data transfer sequence.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it's associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the X1288 resets itself without performing the write. The contents of the array are not affected.

Acknowledge Polling

Disabling of the inputs during nonvolatile write cycles can be used to take advantage of the typical 5mS write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the X1288 initiates the internal nonvolatile write cycle. Acknowledge polling can begin immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the X1288 is still busy with the nonvolatile write cycle then no ACK will be returned. When the X1288 has completed the write operation, an ACK is returned and the host can proceed with the read or write operation. Refer to the flow chart in Figure 16.

Read Operations

There are three basic read operations: Current Address Read, Random Read, and Sequential Read.

Current Address Read

Internally the X1288 contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the sixteen bit address is initialized to 0h. In this way, a current address read immediately after the power-on reset can download the entire contents of memory starting at the first location.Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the X1288 issues an acknowledge, then transmits eight data bits. The master terminates the read operation by not responding with an acknowledge during the ninth clock and issuing a stop condition. Refer to Figure 15 for the address, acknowledge, and data transfer sequence.

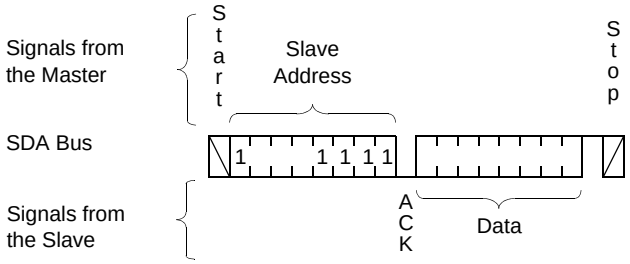


FIGURE 15. CURRENT ADDRESS READ SEQUENCE

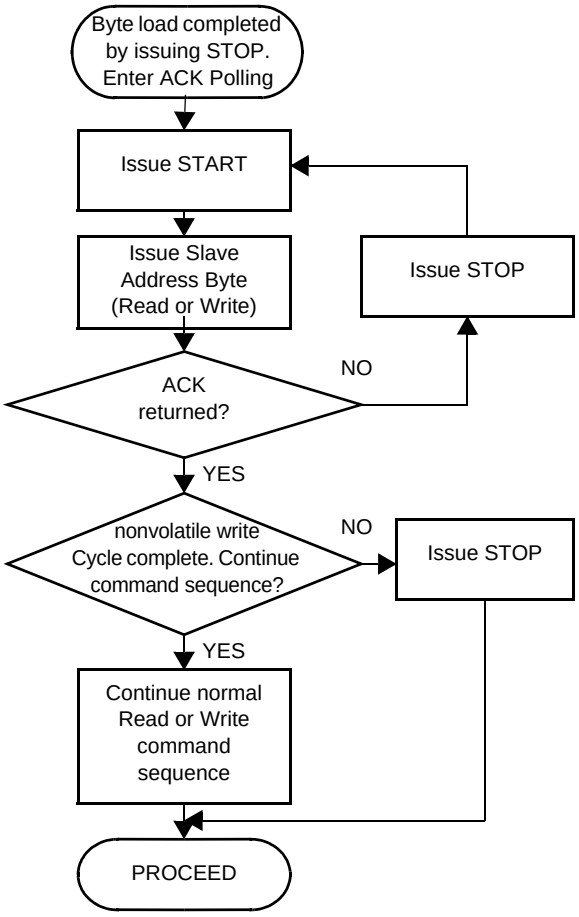


FIGURE 16. ACKNOWLEDGE POLLING SEQUENCE

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Random Read

Random read operations allows the master to access any location in the X1288. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to zero, the master must first perform a “dummy” write operation.

The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipt of each word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 17 for the address, acknowledge, and data transfer sequence.

In a similar operation called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 17. The X1288 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to the start of the address space and the X1288 continues to output data for each acknowledge received. Refer to Figure 18 for the acknowledge and data transfer sequence.

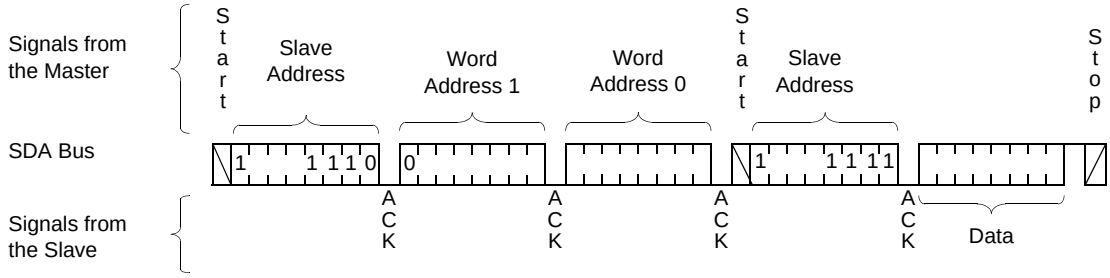


FIGURE 17. RANDOM ADDRESS READ SEQUENCE

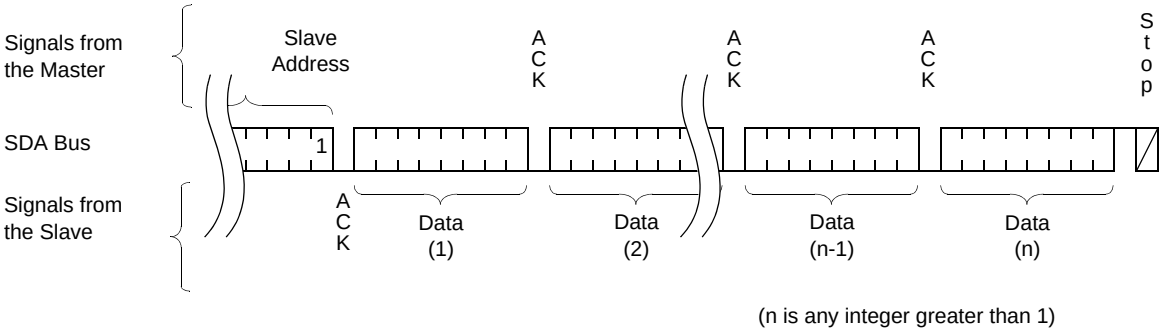


FIGURE 18. SEQUENTIAL READ SEQUENCE

APPLICATION SECTION

CRYSTAL OSCILLATOR AND TEMPERATURE COMPENSATION

Intersil has now integrated the oscillator compensation circuity on-chip, to eliminate the need for external components and adjust for crystal drift over temperature and enable very high accuracy time keeping (<5ppm drift).

The Intersil RTC family uses an oscillator circuit with on-chip crystal compensation network, including adjustable load-capacitance. The only external component required is the crystal. The compensation network is optimized for operation with certain crystal parameters which are common in many of the surface mount or tuning-fork crystals available today. Table 7 summarizes these parameters.

Table 8 contains some crystal manufacturers and part numbers that meet the requirements for the Intersil RTC products.

The turnover temperature in Table 7 describes the temperature where the apex of the of the drift vs. temperature curve occurs. This curve is parabolic with the drift increasing as $(T-T0)^2$. For an Epson MC-405 device, for example, the turnover temperature is typically 25°C, and a peak drift of >110ppm occurs at the temperature extremes of -40 and +85°C. It is possible to address this variable drift by adjusting the load capacitance of the crystal, which will result in predictable change to the crystal frequency. The Intersil RTC family allows this adjustment over temperature since the devices include on-chip load capacitor trimming. This control is handled by the Analog Trimming Register, or ATR, which has 6 bits of control . The load capacitance range covered by the ATR circuit is approximately 3.25pF to 18.75pF, in 0.25pf increments. Note that actual capacitance would also include about 2pF of package related capacitance. In-circuit tests with commercially available crystals demonstrate that this range of capacitance allows frequency control from +116ppm to -37ppm, using a 12.5pF load crystal.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the Intersil RTC family. There are three bits known as the Digital Trimming Register or DTR, and they operate by adding or skipping pulses in the clock signal. The range provided is ±30ppm in increments of 10ppm. The default setting is 0ppm. The DTR control can be used for coarse adjustments of frequency drift over temperature or for crystal initial accuracy correction.

Table 7. Crystal Parameters Required for Intersil RTC's

Parameter	Min	Typ	Max	Units	Notes
Frequency		32.768		kHz	
Freq. Tolerance			±100	ppm	Down to 20ppm if desired
Turnover Temperature	20	25	30	°C	Typically the value used for most crystals
Operating Temperature Range	-40		85	°C	
Parallel Load Capacitance		12.5		pF	
Equivalent Series Resistance			50	kΩ	For best oscillator performance

Table 8. Crystal Manufacturers

Manufacturer	Part Number	Temp Range	+25°C Freq Toler.
Citizen	CM201, CM202, CM200S	-40 to +85°C	±20ppm
Epson	MC-405, MC-406	-40 to +85°C	±20ppm
Raltron	RSM-200S-A or B	-40 to +85°C	±20ppm
SaRonix	32S12A or B	-40 to +85°C	±20ppm
Ecliptek	ECPSM29T-32.768K	-10 to +60°C	±20ppm
ECS	ECX-306/ECX-306I	-10 to +60°C	±20ppm
Fox	FSM-327	-40 to +85°C	±20ppm

A final application for the ATR control is in-circuit calibration for high accuracy applications, along with a temperature sensor chip. Once the RTC circuit is powered up with battery backup, the PHZ output is set at 32.768kHz and frequency drift is measured. The ATR control is then adjusted to a setting which minimizes drift. Once adjusted at a particular temperature, it is possible to adjust at other discrete temperatures for minimal overall drift, and store the resulting settings in the EEPROM. Extremely low overall temperature drift is possible with this method. The Intersil evaluation board contains the circuitry necessary to implement this control.

For more detailed operation see Intersil's application note AN154 on Intersil's website at www.intersil.com.

Layout Considerations

The crystal input at X1 has a very high impedance and will pick up high frequency signals from other circuits on the board. Since the X2 pin is tied to the other side of the crystal, it is also a sensitive node. These signals can couple into the oscillator circuit and produce double clocking or mis-clocking, seriously affecting the accuracy of the RTC. Care needs to be taken in layout of the RTC circuit to avoid noise pickup. Below in Figure 19 is a suggested layout for the X1286 or X1288 devices.

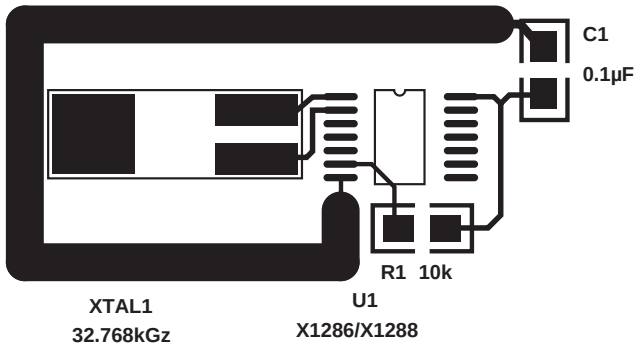


FIGURE 19. SUGGESTED LAYOUT FOR INTERSIL RTC IN SO-8

The X1 and X2 connections to the crystal are to be kept as short as possible. A thick ground trace around the crystal is advised to minimize noise intrusion, but ground near the X1 and X2 pins should be avoided as it will add to the load capacitance at those pins. Keep in mind these guidelines for other PCB layers in the vicinity of the RTC device. A small decoupling capacitor at the Vcc pin of the chip is mandatory, with a solid connection to ground.

The X1286 product has a special consideration. The PHZ/IRQ- pin on the 8-lead SOIC package is located next to the X2 pin. When this pin is used as a frequency output (PHZ) and is set to 32.768kHz output frequency, noise can couple to the X1 or X2 pins and cause double-clocking. The layout in Figure 19 can help minimize this by running the PHZ output away

from the X1 and X2 pins. Also, minimizing the switching current at this pin by careful selection of the pullup resistor value will reduce noise. Intersil suggests a minimum value of 5.1k for 32.768kHz, and higher values (i.e. 20kΩ) for lower frequency PHZ outputs.

For other RTC products, the same rules stated above should be observed, but adjusted slightly since the packages and pinouts are slightly different.

Assembly

Most electronic circuits do not have to deal with assembly issues, but with the RTC devices assembly includes insertion or soldering of a live battery into an unpowered circuit. If a socket is soldered to the board, and a battery is inserted in final assembly, then there are no issues with operation of the RTC. If the battery is soldered to the board directly, then the RTC device Vback pin will see some transient upset from either soldering tools or intermittent battery connections which can stop the circuit from oscillating. Once the battery is soldered to the board, the only way to assure the circuit will start up is to momentarily (very short period of time!) short the Vback pin to ground and the circuit will begin to oscillate.

Oscillator Measurements

When a proper crystal is selected and the layout guidelines above are observed, the oscillator should start up in most circuits in less than one second. Some circuits may take slightly longer, but startup should definitely occur in less than 5 seconds. When testing RTC circuits, the most common impulse is to apply a scope probe to the circuit at the X2 pin (oscillator output) and observe the waveform. DO NOT DO THIS! Although in some cases you may see a useable waveform, due to the parasitics (usually 10pF to ground) applied with the

scope probe, there will be no useful information in that waveform other than the fact that the circuit is oscillating. The X2 output is sensitive to capacitive impedance so the voltage levels and the frequency will be affected by the parasitic elements in the scope probe. Applying a scope probe can possibly cause a faulty oscillator to start up, hiding other issues (although in the Intersil RTC's, the internal circuitry assures startup when using the proper crystal and layout).

The best way to analyze the RTC circuit is to power it up and read the real time clock as time advances, or if the chip has the PHZ output, look at the output of that pin on an oscilloscope (after enabling it with the control register). Alternatively, the X1226/1286/1288 devices have an IRQ- output which can be checked by setting an alarm for each minute. Using the pulse interrupt mode setting, the once-per-minute interrupt functions as an indication of proper oscillation.

Backup Battery Operation

Many types of batteries can be used with the Intersil RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Intersil RTC device for up to 10 years. Another option is to use a supercapacitor for applications where Vcc may disappear intermittently for short periods of time. Depending on the value of supercapacitor used, backup time can last from a few days to two weeks (with >1F). A simple silicon or Schottky barrier diode can be used in series with Vcc to charge the supercapacitor, which is connected to the Vback pin. Do not use the diode to charge a battery (especially lithium batteries!).

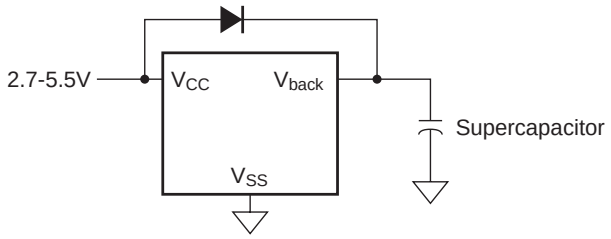


FIGURE 20. SUPERCAPACTOR CHARGING CIRCUIT

Since the battery switchover occurs at Vcc=Vback-0.1V (see Figure 20), the battery voltage must always be lower than the Vcc voltage during normal operation or the battery will be drained. A second consideration is the trip point setting for the system RESET- function, known as Vtrip. Vtrip is set at the factory at levels for systems with either Vcc = 5V or 3.3V operation, with the following standard options:

V_{TRIP} = 4.63V ± 3%
V_{TRIP} = 4.38V ± 3%
V_{TRIP} = 2.85V ± 3%
V_{TRIP} = 2.65V ± 3%

The summary of conditions for backup battery operation is given in Table 9:

Table 9. Battery Backup Operation

1. Example Application, Vcc=5V, Vback=3.0V

Condition	Vcc	Vback	Vtrip	Iback	Reset	Notes
a. Normal Operation	5.00	3.00	4.38	<<1µA	H	
b. Vcc on with no battery	5.00	0	4.38	0	H	
c. Backup Mode	0–1.8	1.8-3.0	4.38	<2µA	L	Timekeeping only

2. Example Application, Vcc=3.3V,Vback=3.0V

Condition	Vcc	Vback	Vtrip	Iback	Reset	
a. Normal Operation	3.30	3.00	2.65	<<1µA	H	
b. Vcc on with no battery	3.30	0	2.65	0	H	
c. Backup Mode	0–1.8	1.8–3.0*	2.65	<2µA*	L	Timekeeping only
d. UNWANTED - Vcc ON, Vback powering	2.65 - 3.30	> Vcc	2.65	up to 3mA	H	Internal Vcc=Vback

*since Vback>2.65V is higher than Vtrip, the battery is powering the entire device

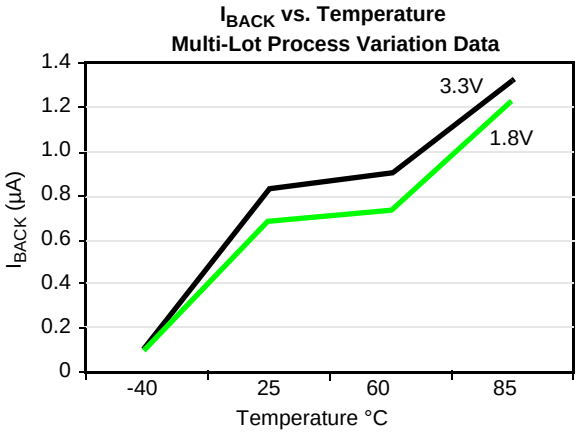
Referring to Figure 20, Vtrip applies to the “Internal Vcc” node which powers the entire device. This means that if Vcc is powered down and the battery voltage at Vback is higher than the Vtrip voltage, then the entire chip will be running from the battery. If Vback falls to lower than Vtrip, then the chip shuts down and all outputs are disabled except for the oscillator and timekeeping circuitry. The fact that the chip can be powered from Vback is not necessarily an issue since standby current for the RTC devices is <2µA for this mode (called “main timekeeping current” in the data sheet). Only when the serial interface is active is there an increase in supply current, and with Vcc powered down, the serial interface will most likely be inactive.

One way to prevent operation in battery backup mode above the Vtrip level is to add a diode drop (silicon diode preferred) to the battery to insure it is below Vtrip. This will also provide reverse leakage protection which may be needed to get safety agency approval.

One mode that should always be avoided is the operation of the RTC device with Vback greater than both Vcc and Vtrip (Condition 2d in Table 9). This will cause the battery to drain quickly as serial bus communication and non-volatile writes will require higher supplier current.

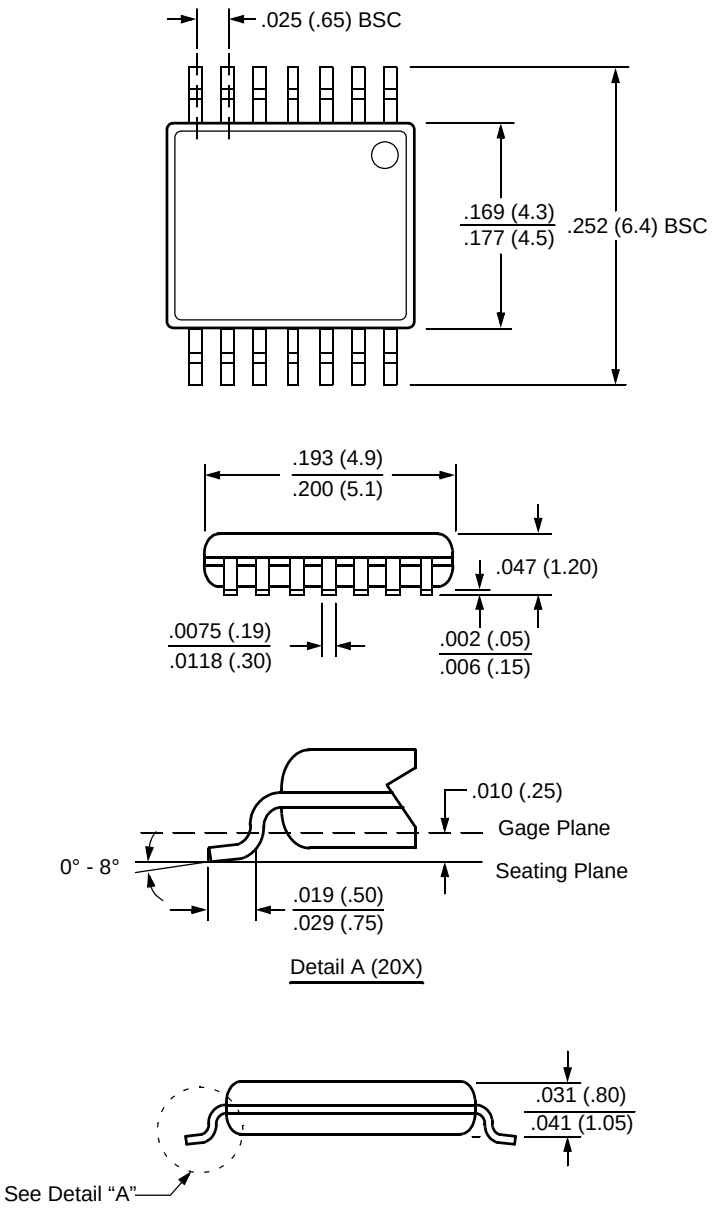
PERFORMANCE DATA

I_{BACK} Performance



PACKAGING INFORMATION

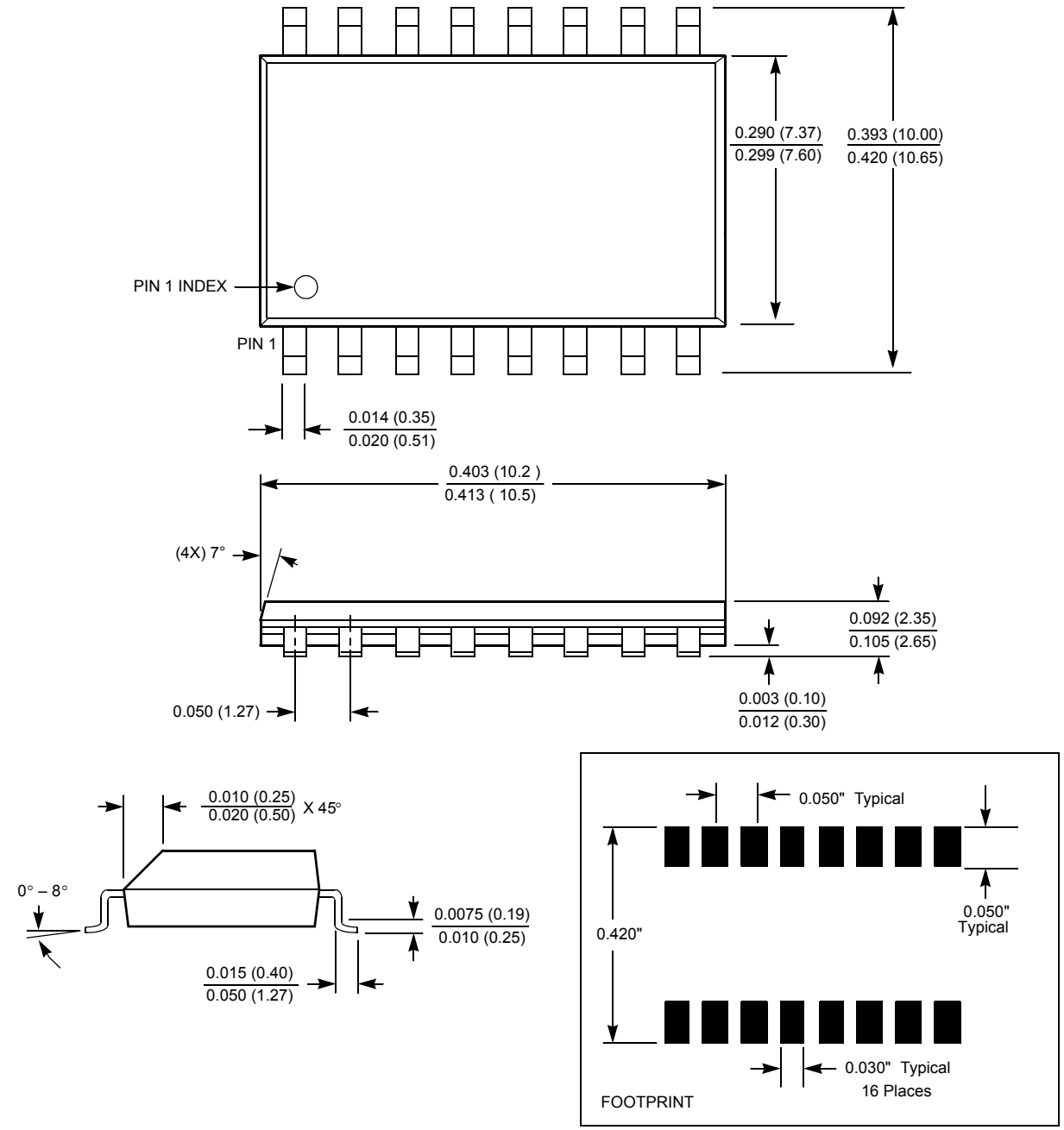
14-Lead Plastic, TSSOP, Package Code V14



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

16-Lead Plastic, SOIC (300-mil body), Package Code S16



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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