

256Kx32 SRAM MODULE PRELIMINARY*

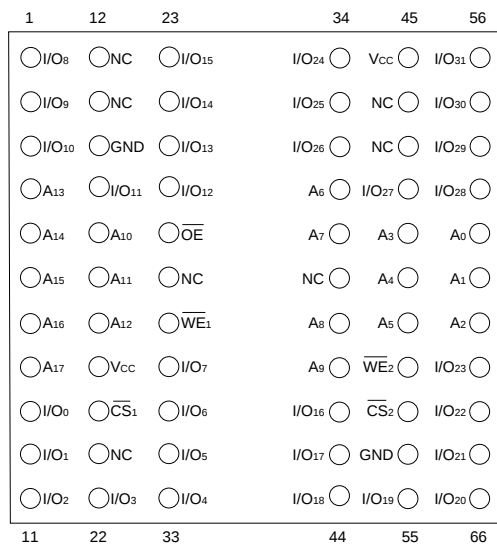
FEATURES

- Access Times 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 66 pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
 - 68 lead, 40mm, Hermetic CQFP (Package 501)
- Organized as 256Kx32, User Configurable as 512Kx16
- Upgradable to 512Kx32 for future expansion
- Data I/O Compatible with 3.3V devices
- 2V Data Retention devices available (WS256K32L-XXX low power version only)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Weight
 - WS256K32N-XXH - 13 grams typical
 - WS256K32-XG4X - 20 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

FIG. 1 PIN CONFIGURATION FOR WS256K32N-XXH

TOP VIEW



PIN DESCRIPTION

I/O ₀ -31	Data Inputs/Outputs
A ₀ -17	Address Inputs
WE ₁ -2	Write Enables
CS ₁ -2	Chip Selects
OE	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

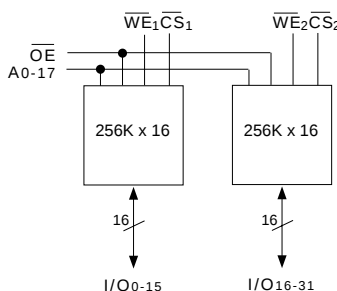
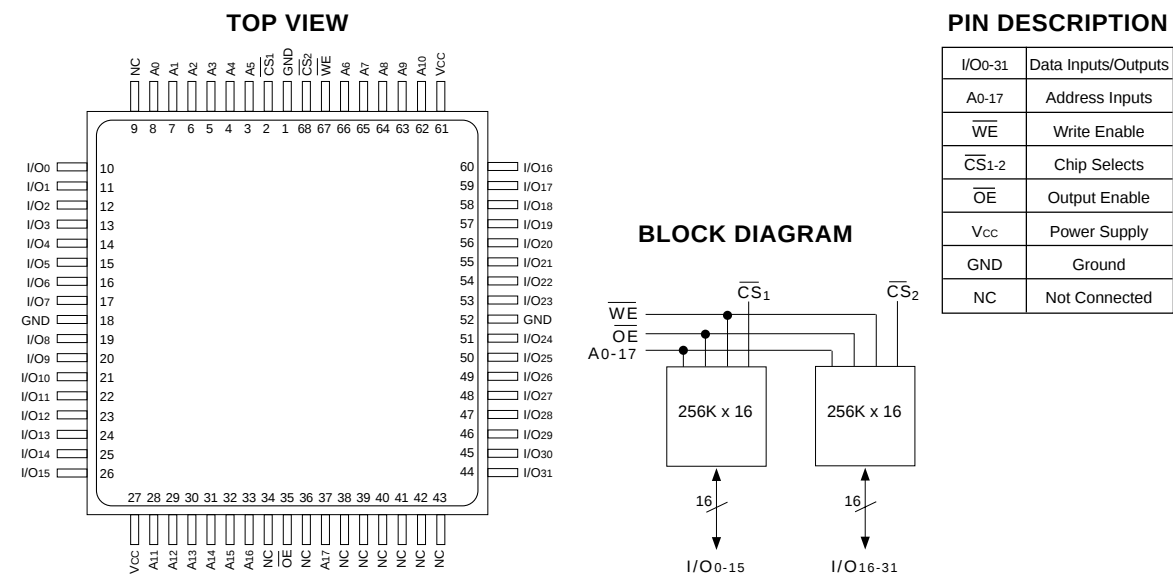
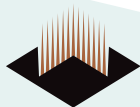




FIG. 2 PIN CONFIGURATION FOR WS256K32-XG4X





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T _A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	28	pF
$\overline{WE}$ 1-2 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4			28	
$\overline{CS}$ 1-2 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	28	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10
Operating Supply Current x 32 Mode	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		550
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		34
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4	

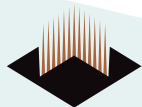
NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

LOW POWER DATA RETENTION CHARACTERISTICS

(WS256K32L-XXX ONLY)

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units		
			Min	Typ	Max
Data Retention Supply Voltage	V _{DR}	$\overline{CS}$ ≥ V _{CC} - 0.2V	2.0		5.5
Data Retention Current	I _{CCDR3}	V _{CC} = 3V		1.0	16



AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	20		25		35		ns
Address Access Time	t _{AA}		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		20		25		35	ns
Output Enable to Output Valid	t _{OE}		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		15		20	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

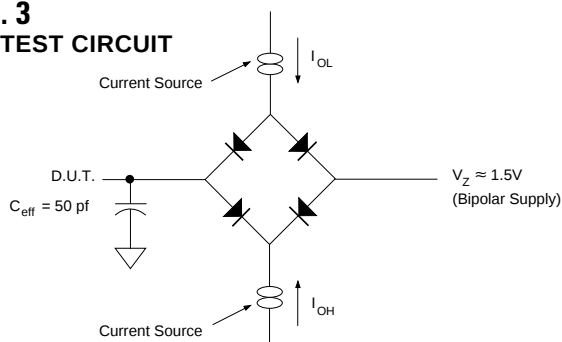
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	20		25		35		ns
Chip Select to End of Write	t _{CW}	17		20		25		ns
Address Valid to End of Write	t _{AW}	17		20		25		ns
Data Valid to End of Write	t _{DW}	12		15		20		ns
Write Pulse Width	t _{WP}	17		20		25		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	2		2		2		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		10		15	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 4
TIMING WAVEFORM - READ CYCLE

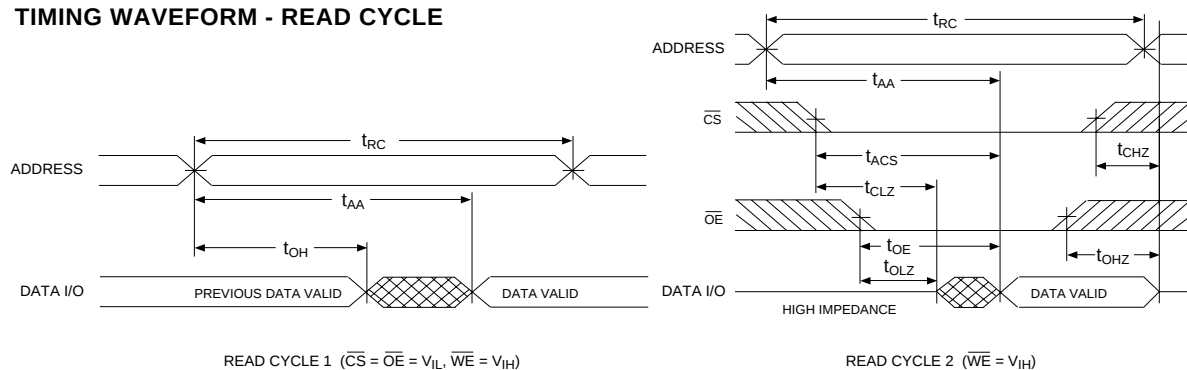


FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED

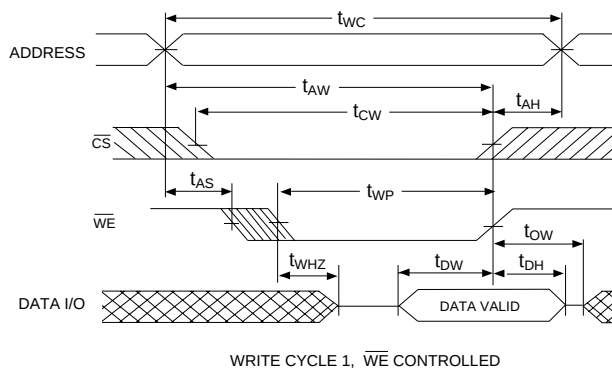
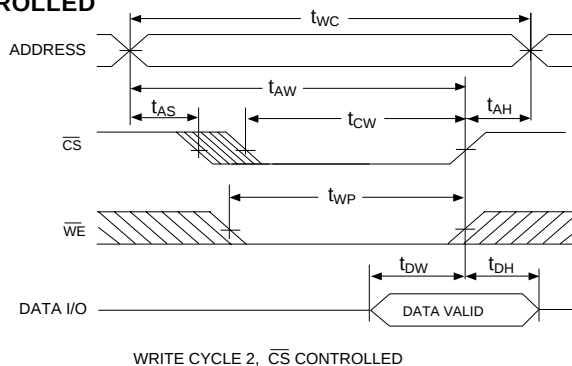
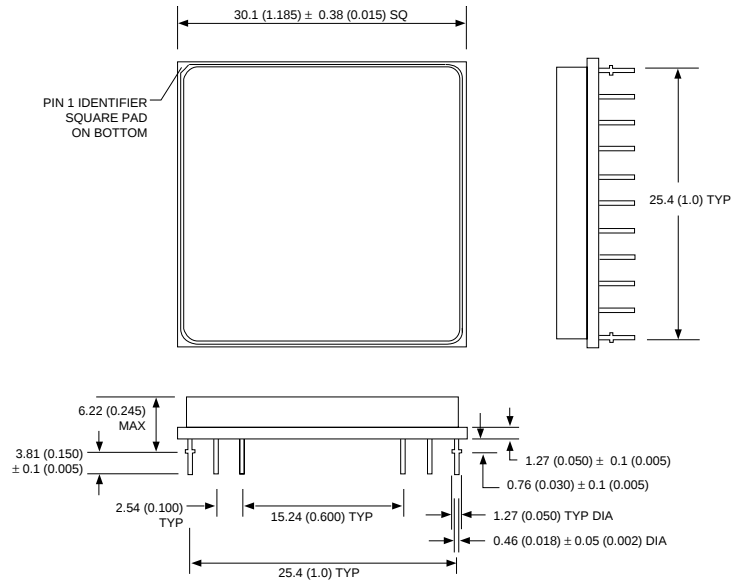


FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



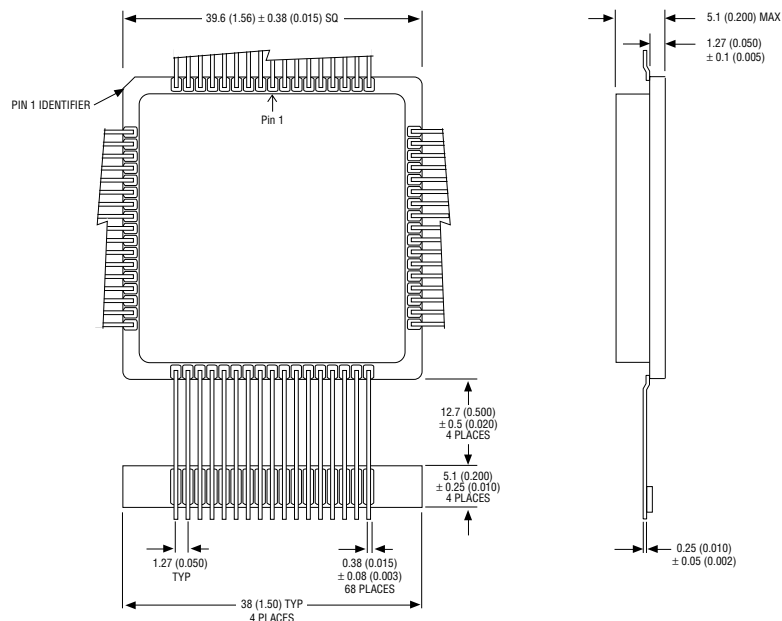


PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



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ORDERING INFORMATION

W S 256K32 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

H = Ceramic Hex-In-Line Package, HIP (Package 401)

G4 = 40mm Ceramic Quad Flat Pack, CQFP (Package 501)

ACCESS TIME (ns)

IMPROVEMENT MARK

N = No Connect at pins 21, 28 and 39 in HIP for Upgrades

Blank = Standard Power

L = Low Power Data Retention

ORGANIZATION, 256Kx32

User configurable as 512Kx16

SRAM

WHITE ELECTRONIC DESIGNS CORP.