WM8714

24-bit, 96kHz Stereo DAC

DESCRIPTION

The WM8714 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8714 supports data input word lengths from 16 to 24-bits and sampling rates up to 96kHz. The WM8714 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-pin SOIC package.

The WM8714 has a hardware control interface for selection of audio data interface format, mute and de-emphasis. The WM8714 supports I^2S, and right Justified audio data interfaces.

The WM8714 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in DVD players.

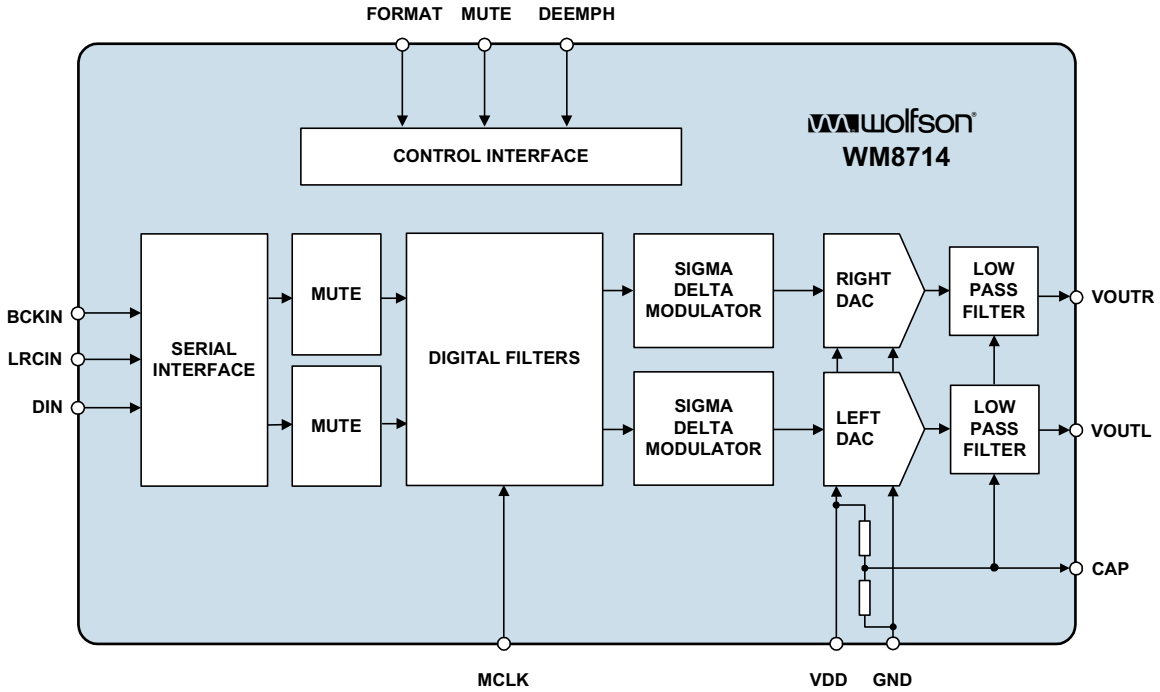
FEATURES

- Stereo DAC
- Audio Performance
  - 95dB SNR ('A' weighted @ 48kHz) DAC
  - -90dB THD
- DAC Sampling Frequency: 8kHz – 96kHz
- Pin Selectable Audio Data Interface Format
  - I^2S, Right Justified or DSP
- 3 - 5V Supply Operation
- 14-pin SOIC Package
- Pin Compatible with WM8725

APPLICATIONS

- DVD Players
- Digital TV
- Digital Set Top Boxes

BLOCK DIAGRAM



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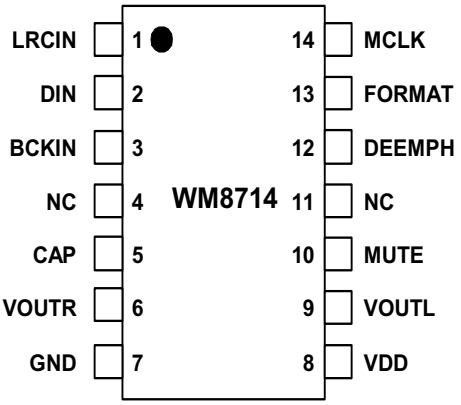
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8714ED	-25 to +85°C	14-pin SOIC	MSL1	240°C
WM8714ED/R	-25 to +85°C	14-pin SOIC (tape and reel)	MSL1	240°C
WM8714GED/V	-25 to +85°C	14-pin SOIC (lead free)	MSL2	260 °C
WM8714GED/RV	-25 to +85°C	14-pin SOIC (lead free, tape and reel)	MSL2	260 °C

Note:
Reel quantity = 3,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCKIN	Digital input	Bit clock input
4	NC	No connect	No internal connection
5	CAP	Analogue output	Analogue internal reference
6	VOUTR	Analogue output	Right channel DAC output
7	GND	Supply	Negative supply
8	VDD	Supply	Positive supply
9	VOUTL	Analogue output	Left channel DAC output
10	MUTE	Digital input	Soft mute control, Internal pull down High = Mute ON Low = Mute OFF
11	NC	No connect	No internal connection
12	DEEMPH	Digital input	De-emphasis select, Internal pull up High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified High = 16-24-bit I^2S
14	MCLK	Digital input	System clock input

Note:

1. Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7V
Voltage range digital inputs	GND -0.3V	VDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply range	VDD		2.7		5.5	V
Ground	GND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Supply current		VDD = 5V		15	25	mA
Supply current		VDD = 3.3V		12		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL} = 2mA			AGND + 0.3V	V
Output HIGH	V_{OH}	I_{OH} = 2mA	AVDD - 0.3V			V
Analogue Reference Levels						
Reference voltage (CAP)			VDD/2 - 50mV	VDD/2	VDD/2 + 50mV	V
Potential divider resistance	R_{VMID}	VDD to CAP and CAP to GND	80k	100k	120k	Ω
DAC Output (Load = 10k ohms. 50pF)						
0dBFs Full scale output voltage		At DAC outputs		1.1 x VDD/5		V_{rms}
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz	90	95		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz		93		dB
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz AVDD, DVDD = 3.3V		97		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz AVDD, DVDD = 3.3V		95		dB
SNR (Note 1,2,3)		Non A-weighted @ fs = 48kHz		92		dB
THD (Note 3)		1kHz, 0dBFs		-90	-74	dB
Dynamic Range (Note 2)		1kHz, THD+N @ -60dBFs	90	95		dB
DAC channel separation				95		dB

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output level		Load = 10kΩ, 0dBFS		1.1		V_{RMS}
		Load = 10kΩ, 0dBFS, (VDD = 3.3V)		0.72		V_{RMS}
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		1		kΩ
		To midrail or a.c. coupled (VDD = 3.3V)		1		kΩ
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				VDD/2		V
Power On Reset (POR)						
POR threshold				1.8		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured A-weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. CAP pin decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

MASTER CLOCK TIMING

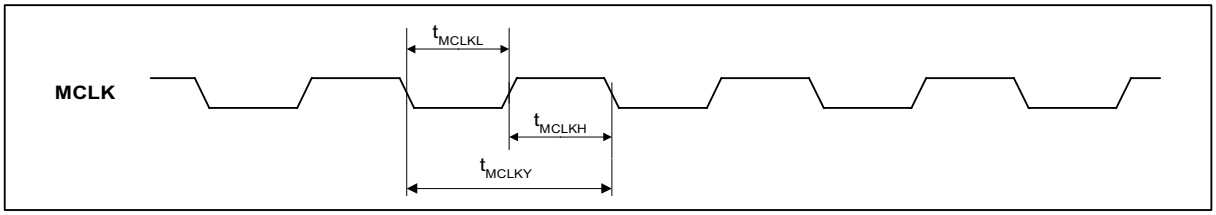


Figure 1 Master Clock Timing Requirements

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		8			ns
MCLK Master clock pulse width low	t_{MCLKL}		8			ns
MCLK Master clock cycle time	t_{MCLKY}		20			ns
MCLK Duty cycle			40:60		60:40	

DIGITAL AUDIO INTERFACE

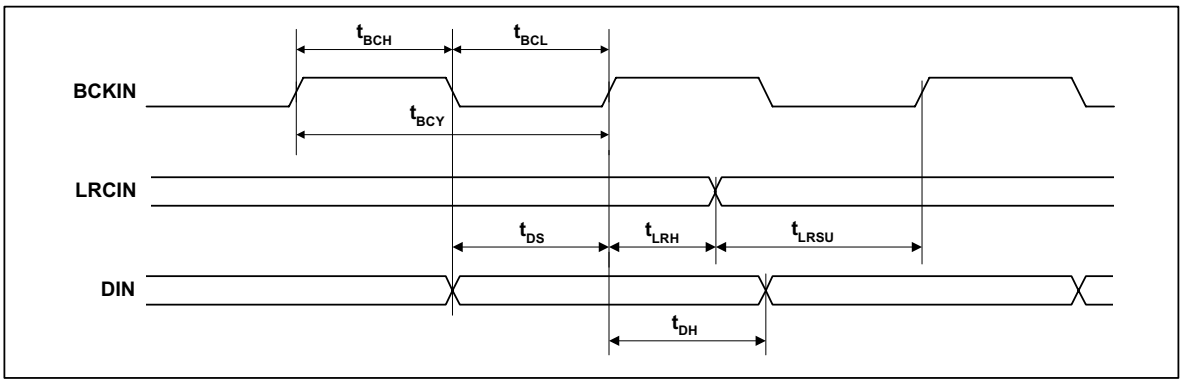


Figure 2 Digital Audio Data Timing

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from BCKIN rising edge	t_{LRH}		8			ns
DIN set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN hold time from BCKIN rising edge	t_{DH}		8			ns

DEVICE DESCRIPTION

GENERAL INTRODUCTION

The WM8714 is a high performance DAC designed for digital consumer audio applications. The range of features make it ideally suited for use in DVD players, AV receivers and other consumer audio equipment.

The WM8714 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters. It is fully compatible and an ideal partner for a range of industry standard DSPs and audio controllers. A novel multi bit sigma-delta DAC design is used, utilising a 128x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance. (In 'high-rate' operation, the oversampling ratio is 64x for system clocks of 128fs or 192fs)

Control of internal functionality of the device is provided by hardware control (pin programmed).

Operation using master clocks of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

The audio data interface supports 16-bit right justified or 16-24-bit I^2S (Philips left justified, one bit delayed) interface formats.

Single 2.7-5.5V supplies may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption combined with the low pin count small package make the WM8714 attractive for many consumer applications.

The device is packaged in a small 14-pin SOIC.

DAC CIRCUIT DESCRIPTION

The WM8714 DAC is designed to allow playback of 24-bit PCM audio or similar data with high resolution and low noise and distortion. The two DACs on the WM8714 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the up to 96ks/s input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 24-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images on the output of the DAC. To ensure that generation of tones characteristic to sigma-delta converters is not a problem, dithering is used in the digital modulator along with a higher order modulator. The multi-bit switched capacitor technique used in the DAC reduces sensitivity to clock jitter, and dramatically reduces out of band noise compared to switched current or single bit techniques used in other implementations.

The voltage on the CAP pin is used as the reference for the DACs. Therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP pin. An external reference could be used to drive into the CAP pin if desired, with a value typically of about midrail ideal for optimum performance.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers. These amplifiers will source load currents of several mA and sink current up to 1.5mA allowing significant loads to be driven. The output source is active and the sink is Class A, i.e. fixed value, so greater loads might be driven if an external 'pull-down' resistor is connected at the output.

Typically an external low pass filter circuit will be used to remove residual out of band noise characteristic of delta sigma converters. However, the advanced multi-bit DAC used in WM8714 produces far less out of band noise than single bit traditional sigma delta DACs, and so in many applications this filter may be removed, or replaced with a simple RC pole.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master clock can be applied directly through the MCLK input pin with no configuration necessary for sample rate selection.

Note that on the WM8714, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Two interface formats are supported:

- Right Justified mode
- I^2S mode

All formats send the MSB first. The data format is selected with the FORMAT pin. When FORMAT is LOW, right justified data format is selected and word lengths up to 16-bits may be used. When the FORMAT pin is HIGH, I^2S format is selected and word length of any value up to 24-bits may be used. (If the word length shorter than 24-bits is used, the unused bits will be padded with zeros).

'Packed' mode (i.e. only 32 or 48 clocks per LRCLK period) operation is also supported in both I^2S (16-24 bits) and right justified formats, (16 wordlength). If a 'packed' format of 16-bit word length is applied (16 BITCLKS per LRCLK half period), the device auto-detects this mode and switches to 16-bit data length.

I^2S MODE

The WM8714 supports word lengths of 16-24 bits in I^2S mode.

In I^2S mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In I^2S modes, the minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met.

In I^2S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left samples and high during the right samples.

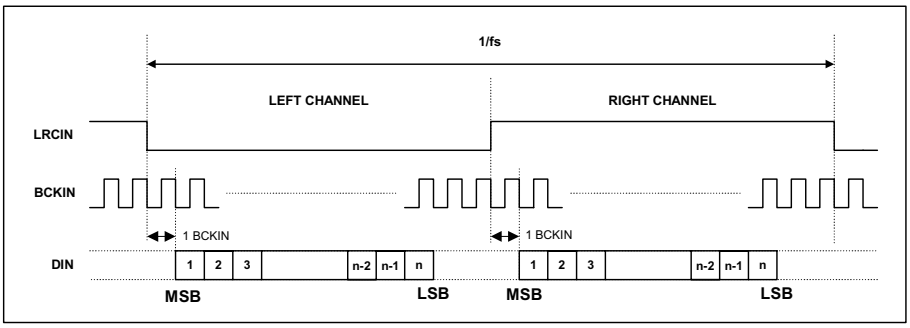


Figure 3 I^2S Mode Timing Diagram

RIGHT JUSTIFIED MODE

The WM8714 supports word lengths of 16-bits in right justified mode.

In right justified mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In right justified mode, the minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met.

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

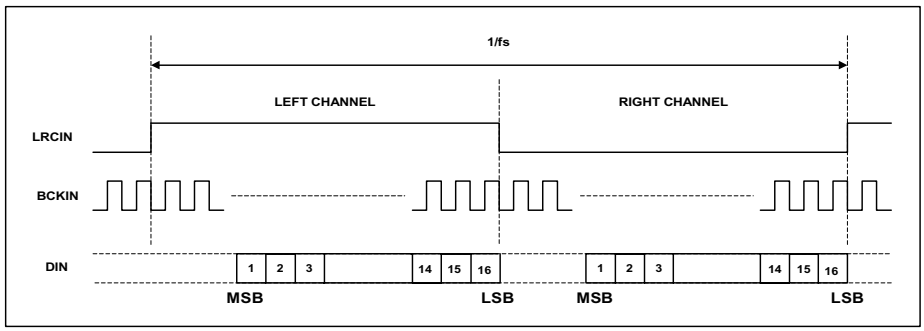


Figure 4 Right Justified Mode Timing Diagram

AUDIO DATA SAMPLING RATES

The master clock for WM8714 supports audio sampling rates from 256fs and 384fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, and 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8714 has a master clock detection circuit that automatically determines the relation between the master clock frequency and the sampling rate (to within +/- 8 master clocks). If there is a greater than 8 clocks error, the interface shuts down the DAC and mutes the output. The master clock should be synchronised with LRCIN, although the WM8714 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE	MASTER CLOCK FREQUENCY (MHZ) (MCLK)	
(LRCIN)	256fs	384fs
32kHz	8.192	12.288
44.1kHz	11.2896	16.9340
48kHz	12.288	18.432
96kHz	24.576[1]	36.864[1]

Table 1 Master Clock Frequencies Versus Sampling Rate

Notes:

1. 96kHz sample rate at either 256fs or 384fs are only supported with 5V supplies.

HARDWARE CONTROL MODES

The WM8714 is hardware programmable providing the user with options to select input audio data format, de-emphasis and mute.

MUTE OPERATION

Pin 10 (MUTE) controls selection of MUTE directly, and can be used to enable and disable the mute.

MUTE PIN	DESCRIPTION
0	Normal Operation, MUTE off
1	Mute DAC channels

Table 2 Mute Control

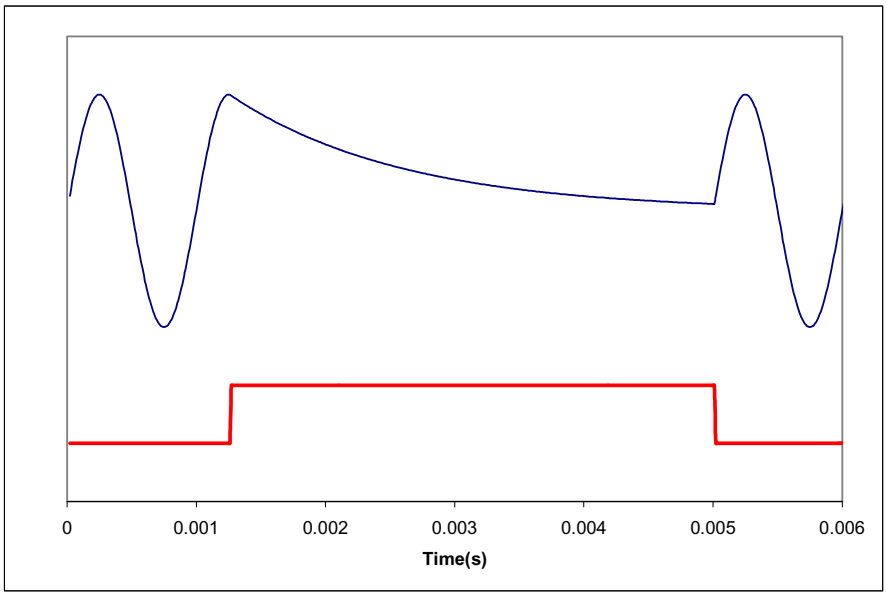


Figure 5 Application and Release of MUTE

The MUTE pin is an input to select mute or not mute. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter. Refer to figure 5.

INPUT AUDIO FORMAT SELECTION

FORMAT (pin 13) controls the data input format.

FORMAT	INPUT DATA MODE
0	16 right justified
1	16 - 24-bit I^2S

Table 3 Input Audio Format Selection

Notes:

1. In 16-24 bit I^2S mode, any width of 24 bits or more is supported provided that LRCIN is high for a minimum of 24 BCKINs and low for a minimum of 24 BCKINs, unless Note 2.
2. If exactly 16 BCKIN cycles occur in both the low and high period of LRCIN the WM8714 will assume the data is 16-bit and accept the data accordingly.

DE-EMPHASIS CONTROL

DEEMPH (pin 12) is an input control for selection of de-emphasis filtering to be applied.

DEEMPH	DE-EMPHASIS
0	Off
1	On

Table 4 De-emphasis Control

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.25	dB
Stopband Attenuation		f > 0.555fs	-40			dB

Table 5 Digital Filter Characteristics

RECOMMENDED EXTERNAL COMPONENTS

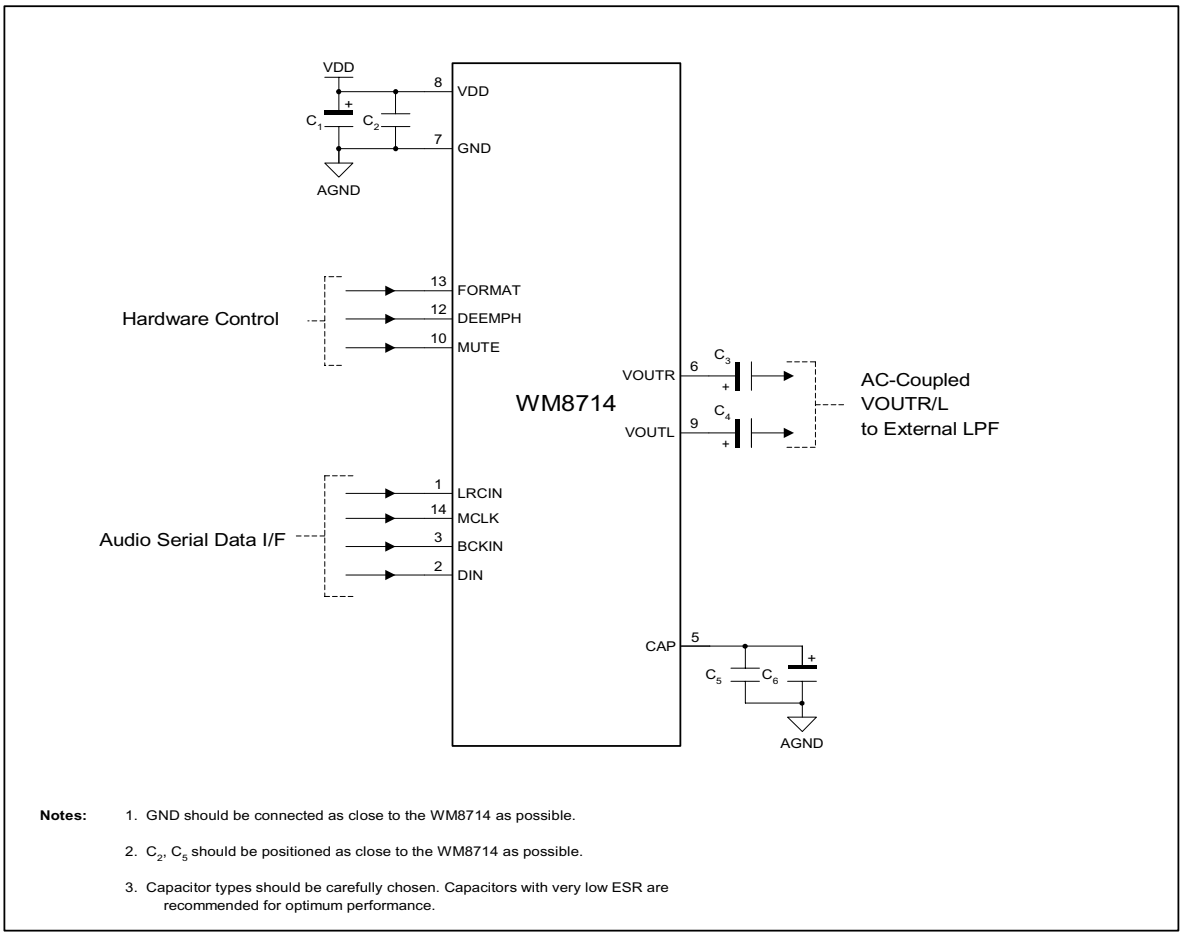


Figure 65 External Component Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	10µF	De-coupling for VDD
C2	0.1µF	De-coupling for VDD
C3 and C4	10µF	Output AC coupling caps to remove midrail DC level from outputs
C5	0.1µF	Reference de-coupling capacitors for CAP pin
C6	10µF	

Table 6 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER (OPTIONAL)

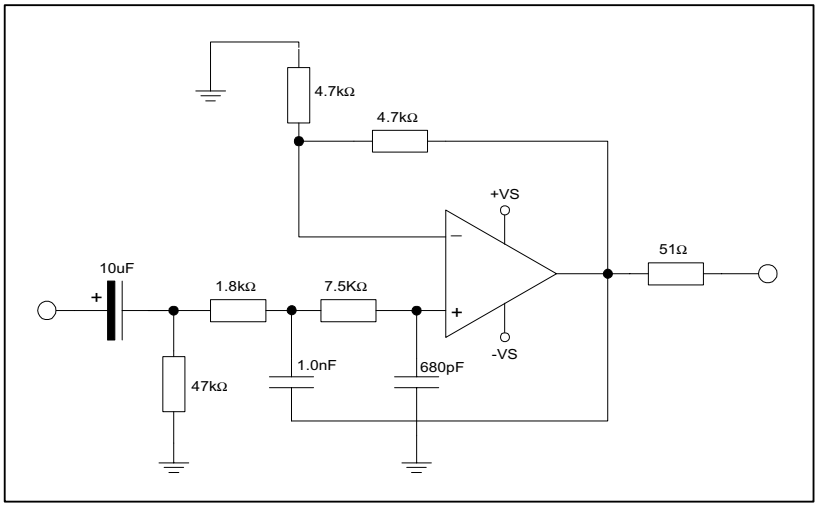


Figure 7 Recommended 2nd Order Low Pass Filter (Optional)

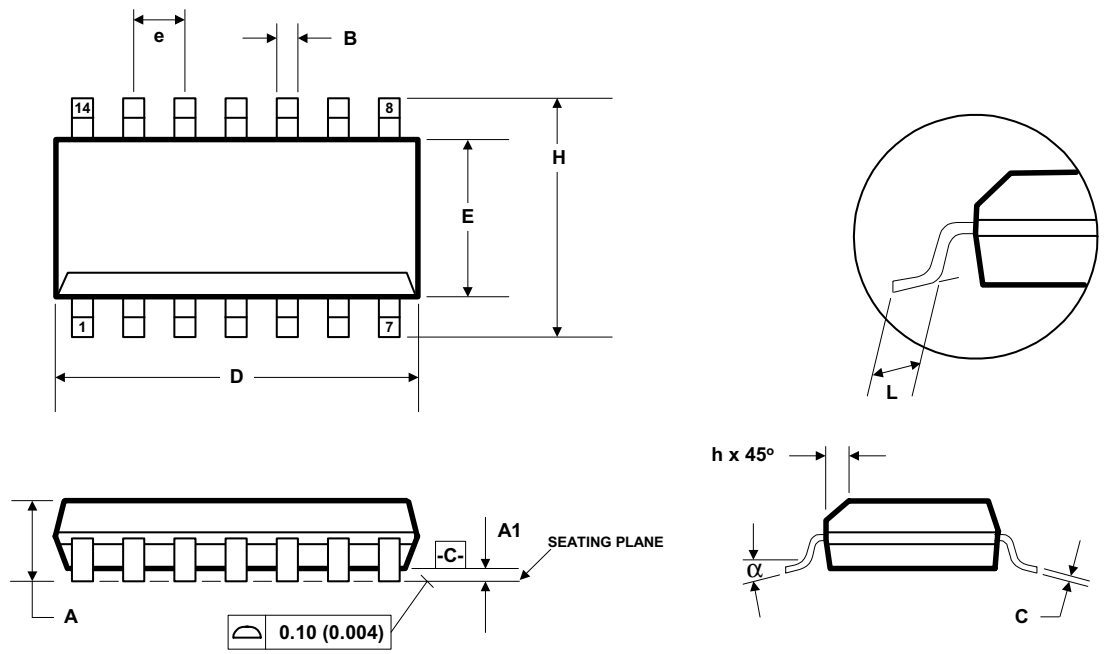
An external low pass filter is recommended (see Figure 7) if the device is driving a wideband amplifier. In some applications, a passive RC filter may be adequate.

PCB LAYOUT

1. Place all supply decoupling capacitors as close as possible to their respective supply pins and provide a low impedance path from the capacitors to the appropriate ground.
2. Separate analogue and digital ground planes should be situated under respective analogue and digital device pins.
3. Digital input signals should be screened from each other and from other sources of noise to avoid cross-talk and interference. They should also run over the digital ground plane to avoid introducing unwanted noise into the analogue ground plane.
4. Analogue output signal tracks should be kept as short as possible and over the analogue ground plane reducing the possibility of losing signal quality.

PACKAGE DRAWING

D: 14 PIN SOIC 3.9mm Wide Body **DM001.C**



Symbols	Dimensions (MM)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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