W78ERD2 Data Sheet

8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W78ERD2 is an 8-bit microcontroller which has an in-system programmable Flash EPROM for firmware updating. The instruction set of the W78ERD2 is fully compatible with the standard 8052. The W78ERD2 contains a 64K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 64KB main Flash EPROM to be updated by the loader program located at the 4KB auxiliary Flash EPROM ROM; 256 bytes of on-chip RAM, 1K AUX-RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by a nine sources four level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78ERD2 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78ERD2 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

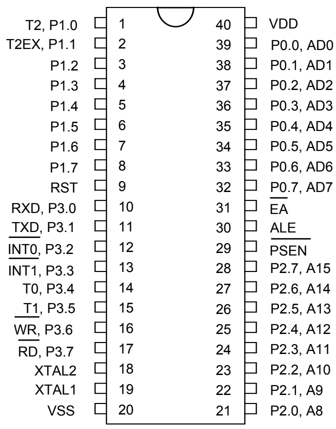
2. FEATURES

- 8-bit CMOS microcontroller
- Pin compatible with standard 80C52
- Instruction-set compatible with MCS-51
- Four 8-bit I/O Ports
- One extra 4-bit I/O port, interrupt, chip select function
- Three 16-bit Timers
- Programmable clock out
- Programmable Counter Array (PCA): PWM, Capture, Compare, Watchdog
- 9 interrupt sources with 4 levels of priority
- One enhanced full duplex serial port with framing error detection and automatic address recognition
- 64KB In-system Programmable Flash EPROM (AP Flash EPRAOM)
- 4KB Auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256+1K bytes of on-chip RAM. (Including 1K bytes of AUX-RAM, software selectable)
- Software Reset
- 12 clocks per machine cycle operation (default). Speed up to 40 MHz.
- 6 clocks per machine cycle operation which is set by the writer. Speed up to 20 MHz.
- 2 DPTR registers
- Low EMI (inhibit ALE)
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  – DIP 40: W78ERD2A40DN
  – PLCC 44: W78ERD2A40PN
  – QFP 44: W78ERD2A40FN

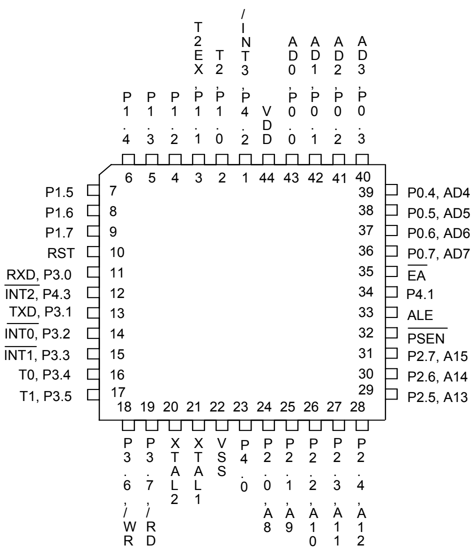
Winbond Electronics Corp.

3. PIN CONFIGURATIONS

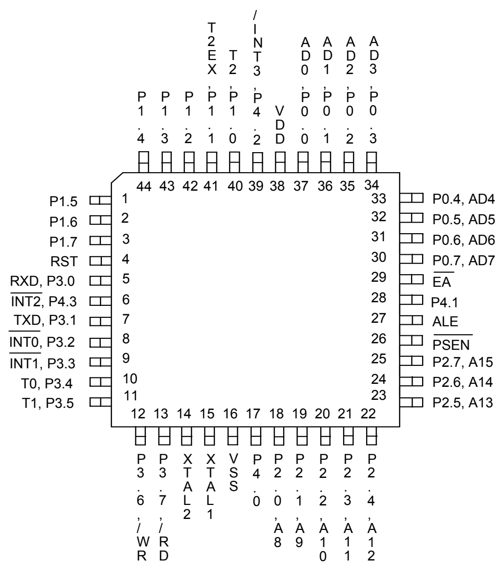
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	I	GROUND: ground potential.
VDD	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: Function is the same as that of standard 8052.
P1.0 – P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0 – P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0 – P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0 – P4.3	I/O H	PORT 4: A bi-directional I/O. See details below.

* **Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

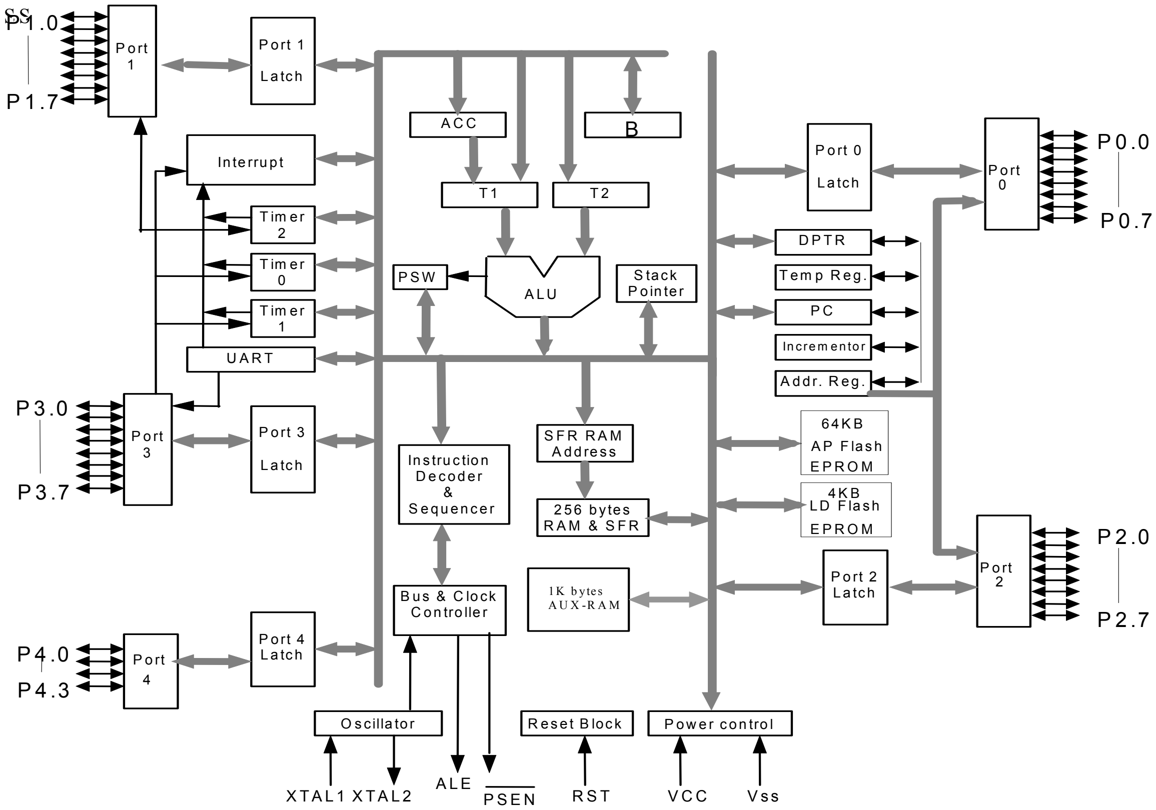
PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1.

Example:

```
P4      REG     0D8H
MOV     P4, #0AH          ; Output data "A" through P4.0 – P4.3.
MOV     A, P4             ; Read P4 status to Accumulator.
ORL     P4, #00000001B
ANL     P4, #11111110B
```

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

The W78ERD2 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 256 bytes of RAM, 1K AUX-RAM, three timer/counters, a serial port and an internal 74373 latch and 74244 buffer which can be switched to port2. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

6.1 RAM

The internal data RAM in the W78ERD2 is 256 + 1K bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 1K bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H – 7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are

  R0 and R1 of the selected register bank.
- RAM 80H – FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0,

  R1 of the selected registers bank.
- AUX-RAM 0H –3FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than 3FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM will be enabled after a reset.

Clearing the bit 1 in AUXR register will enable the access to AUX-RAM. When AUX-RAM is enabled the instructions of "MOVX @Ri" will always access to on-chip AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example,

```
ANL     AUXR, #11111101B  ; Enable AUX-RAM
MOV     DPTR, #1234H
MOV     A, #56H
MOVX    @DPTR, A          ; Write 56h data to external memory at address 1234H
MOV     XRAMAH, #02H      ; Only 2 LSB effective
MOV     R0, #34H
MOV     A, @R0            ; Read AUX-RAM data at address 0234H
```

6.2 Timers 0, 1 and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

6.3 Clock

The W78ERD2 is designed with either a crystal oscillator or an external clock.

6.4 Crystal Oscillator

The W78ERD2 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

6.5 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

6.6 Power Management

6.6.1 Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

6.6.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$ when enabled and set to level triggered.

6.7 Reduce EMI Emission

If the crystal frequency is under 25 MHz, please option.b7 is set to 0 by the writer. Please refer option bits description to operate this bit.

6.8 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78ERD2 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

7. SPECIAL FUNCTION REGISTER

W78E51RD2 Special Function Registers (SFRs) and Reset Values

F8		CH 00000000	CCAP0H 00000000	CCAP1H 00000000	CCAP2H 00000000	CCAP3H 00000000	CCAP4H 00000000		FF
F0	+B 00000000						CHPENR 00000000		F7
E8	+P4 xxxx1111	CL 00000000	CCAP0L 00000000	CCAP1L 00000000	CCAP2L 00000000	CCAP3L 00000000	CCAP4L 00000000		EF
E0	+ACC 00000000								E7
D8	CCON x0000000	CMOD 00xxx000	CCAPM0 x0000000	CCAPM1 x0000000	CCAPM2 x0000000	CCAPM3 x0000000	CCAPM4 x0000000	CKCON xx000xx1	DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000	T2MOD xxxxxx00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000	XICONH 0xxx0xxx	P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000	C7
B8	+IP x0000000	SADEN 00000000						CHPCON 000xx000	BF
B0	+P3 00000000				P43AL 00000000	P43AH 00000000		IPH x0000000	B7
A8	+IE 00000000	SADDR 00000000			P42AL 00000000	P42AH 00000000	P4CSIN 00000000		AF
A0	+P2 11111111	XRAMAH 00000000	AUXR1 xxxxx0x0				WDTRST 00000000		A7
98	+SCON 00000000	SBUF xxxxxxxx					P2EAL 00000000	P2EAH 00000000	9F
90	+P1 11111111				P41AL 00000000	P41AH 00000000			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR 00000000		8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	P40AL 00000000	P40AH 00000000	PORT 00000000	PCON 00110000	87

Notes:

1. The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

Port 4.0 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

Port 4.0 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic: P40AH Address: 85h

Port Option Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0PH

Mnemonic: POPT Address: 86h

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	-	Reserve
2	-	Reserve
1	-	Reserve
0	P0PH	0: Disable Port 0 weak up. 1: Enable Port 0 weak up. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the P0UP bit in the POPT register is set, the pins of port 0 will perform a bi-directional I/O port with internal pull-up that is structurally the same Port2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable, then and SCON.7 indicates a Frame Error and acts as the FE (FE_1) flag.

Continued

BIT	NAME	FUNCTION
5	-	Reserve
4	POF	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	These two bits are general purpose user flags.
2	GF0	These two bits are general purpose user flags.
1	PD	1: Setting this bit causes the Chip to go into the POWER DOWN mode. In this mode all the clocks are stopped and program execution is frozen.
0	IDL	1: Setting this bit causes the Chip to go into the IDLE mode. In this mode the clocks to the CPU are stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0

Mnemonic: TMOD   Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.
6	$C/\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.
5	M1	Mode Select bits:
4	M0	Mode Select bits:
3	GATE	Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.
2	$C/\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.
1	M1	Mode Select bits:
0	M0	Mode Select bits:

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 18-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0   Address: 8Ah

TL0.7-0: Timer 0 Low byte

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 Low byte

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 High byte

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 High byte

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EXTRAM	ALEOFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	-	Reserve
2	-	Reserve
1	EXTRAM	0 = Enable AUX-RAM 1 = Disable AUX-RAM
0	ALEOFF	0: ALE expression is enabled. 1: ALE expression is disabled.

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

Port 4.1 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

Port 4.1 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port 0, Mode 0 bit or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial port Mode bit 1: Mode: SM0 SM1 Description Length Baud rate 0 0 0 Synchronous 8 4/12 Tclk 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 64/32 Tclk 3 1 1 Asynchronous 11 Variable

Continued

BIT	NAME	FUNCTION
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052.
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port 1 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

Ram High Byte Address

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	XRAMA H.1	XRAMA H.0

Mnemonic: XRAMAH Address: A1h

The AUX-RAM high byte address

Auxiliary 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	GF3	0	-	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	GF2	The GF2 bit is a general purpose user–defined flag.
2	0	The bit can’t be written and always read as 0
1	-	Reserve
0	DPS	When DPS = 1 switch to DPTR0. DPS = 1 switch to DPTR1.

Watchdog Timer Reset Register

Bit:	7	6	5	4	3	2	1	0
	WDTRST.7	WDTRST.6	WDTRST.5	WDTRST.4	WDTRST.3	WDTRST.2	WDTRST.1	WDTRST.0

Mnemonic: WDTRST   Address: A6h

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE   Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts except for PFI.
6	EC	Enable PCA interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR   Address: A9h

BIT	NAME	FUNCTION
7	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

Port 4.2 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AL.7	P42AL.6	P42AL.5	P42AL.4	P42AL.3	P42AL.2	P42AL.1	P42AL.0

Mnemonic: P42AL   Address: ACh

Port 4.2 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic: P42AH Address: ADh

Port 4 CS Sign

Bit:	7	6	5	4	3	2	1	0
	P4CSIN.7	P4CSIN.6	P4CSIN.5	P4CSIN.4	P4CSIN.3	P4CSIN.2	P4CSIN.1	P4CSIN.0

Mnemonic: P4CSIN Address: AEh

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P32.6	P3.5	P32.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

Port 4.3 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AL.7	P43AL.6	P43AL.5	P43AL.4	P43AL.3	P43AL.2	P43AL.1	P43AL.0

Mnemonic: P43AL Address: B4h

Port 4.3 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AH.7	P43AH.6	P43AH.5	P43AH.4	P43AH.3	P43AH.2	P43AH.1	P43AH.0

Mnemonic: P43AH Address: B5h

Interrupt Priority High

Bit:	7	6	5	4	3	2	1	0
	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IPH Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PPCH	1: To set interrupt priority of PCA is highest priority level.
5	PT2H	1: To set interrupt priority of Timer 2 is highest priority level.
4	PSH	1: To set interrupt priority of Serial port 0 is highest priority level.
3	PT1H	1: To set interrupt priority of Serial port 0 is highest priority level.
2	PX1H	1: To set interrupt priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt priority of External interrupt 0 is highest priority level.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PPC	1: To set interrupt priority of PCA is higher priority level.
5	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Serial port 0 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN.n is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

On-Chip Programming Control

Bit:	7	6	5	4	3	2	1	0
	SWRST/REBOOT	-	-	-	-	0	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	SWRESET/ REBOOT (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the H/W REBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	-	Reserve
3	-	Reserve
2	-	Reserve
1	FBOOTSL	The Program Location Select. 0: The Loader Program locates at the 64 KB AP Flash EPROM. 4KB LD Flash EPROM is destination for re-programming. 1: The Loader Program locates at the 4 KB memory bank. 64KB AP Flash EPROM is destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. = 1: enable. The microcontroller enter the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieve when device enters idle mode. = 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority high if set
6	EX3	External interrupt 3 enable if set
5	IE3	1: IE3 is set/cleared automatically by hardware when interrupt is detected / serviced
4	IT3	1: External interrupt 3 is falling-edge/low-level triggered when this bit is set / cleared by software
3	PX2	External interrupt 2 priority high if set
2	EX2	External interrupt 2 enable if set
1	IE2	1: IE2 is set/cleared automatically by hardware when interrupt is detected / serviced
0	IT2	1: External interrupt 2 is falling-edge/low-level triggered when this bit is set / cleared by software

External Interrupt High Control

Bit:	7	6	5	4	3	2	1	0
	PXH3	-	-	-	PXH2	-	-	-

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PXH3	External interrupt 3 priority highest if set
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	PXH2	External interrupt 2 priority highest if set
2	-	Reserve
1	-	Reserve
0	-	Reserve

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.

BIT	NAME	FUNCTION
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15 – A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15 – A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15 – A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

F/W Flash Low Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAL Address: C4h

F/W flash low byte address

F/W Flash High Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAH Address: C5h

F/W flash high byte address

F/W Flash Data

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRFD Address: C6h

F/W flash data

F/W Flash Control

Bit:	7	6	5	4	3	2	1	0
	0	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: C7h

BIT	NAME	FUNCTION
7	-	Reserve
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. 0: 64K bytes Flash EPROM bank is selected as destination for re-programming. 1: 4K bytes Flash EPROM bank is selected as destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3~0	CTRL[3:0]	The flash control signals

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.
6	EXF2	Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 underflow/overflow will cause this flag to set based on the CP/RL2, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.
5	RCLK	Receive clock Flag: This bit determines the serial port time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, else timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
4	TCLK	Transmit clock Flag: This bit determines the serial port time-base when transmitting data in mode 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock, else timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

Continued

BIT	NAME	FUNCTION
3	EXEN2	Timer 2 External Enable: This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, else a negative transition detected on the T2EX pin will result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables/disables the operation of timer 2.halting this will preserve the current count in TH2, TL2.
1	C/T2	Counter/Timer select: This bit determines whether timer 2 will function as a timer or a counter. Independent of this bit, the timer will run at 2 clocks per tick when used in baud rate generator mode. If it is set to 0, then timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5), else, it will count negative edges on T2 pin.
0	CP/RL2	Capture/Reload Select: This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX if EXEN2 = 1.

Timer 2 Mode

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	T2OE	DCEN

Mnemonic: T2MOD   Address: C9h

BIT	NAME	FUNCTION
7~2	-	Reserve
1	T2OE	Timer 2 Output Enable. This bit enables/disables the Timer 2 clock out function.
0	DCEN	Down Count Enable: This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture Low

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L   Address: CAh

RCAP2L Timer 2 Capture LSB: This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Capture High

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H Timer 2 Capture HSB: This register is used to capture the TH2 value when a timer 2 is configured in capture mode. RCAP2H is also used as the HSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Register Low

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TLH2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

Timer 2 Register High

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TL2 Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PCA Counter Control Register

Bit:	7	6	5	4	3	2	1	0
	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Mnemonic: CCON Address: D8h

PCA Counter Mode Register

Bit:	7	6	5	4	3	2	1	0
	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Mnemonic: CMOD Address: D9h

PCA Module 0 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0

Mnemonic: CCAPM0 Address: DAh

PCA Module 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1

Mnemonic: CCAPM1 Address: DBh

PCA Module 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2

Mnemonic: CCAPM2 Address: DCh

PCA Module 3 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3

Mnemonic: CCAPM3 Address: DDh

PCA Module 4 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4

Mnemonic: CCAPM4 Address: DEh

Clock Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	T2M	T1M	T0M	-	-	MD

Mnemonic: CKCON Address: DFh

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	T2M	Timer 2 clock select: When T2M is set to 1, timer 2 uses a divide by 6 clock, and when set to 0 uses a divide by 12 clock. (This bit has no effect if bit 3 of Option-bits is set to 1 to select 12 clocks/machine cycle)
4	T1M	Timer 1 clock select: When T1M is set to 1, timer 1 uses a divide by 6 clock, and when set to 0 uses a divide by 12 clock. (This bit has no effect if bit 3 of Option-bits is set to 1 to select 12 clocks/machine cycle)
3	T0M	Timer 0 clock select: When T0M is set to 1, timer 0 uses a divide by 6 clock, and when set to 0 uses a divide by 12 clock. (This bit has no effect if bit 3 of Option-bits is set to 1 to select 12 clocks/machine cycle)
2	-	Reserve
1	-	Reserve
0	MD	Stretch MOVX select bits: This bit is used to select the stretch value for the MOVX instruction. Using a variable MOVX length. Enables the user to access slower memory devices or peripherals without the need for external circuits. The RD or WR strobe will be stretched by the selected interval. All internal timing s are also stretched by the same amount. This operation is transparent to the user. By default, the stretch has value 1 cycle. If the user needs faster accessing, then stretch value of 0 should be selected

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3/INT2	P4.2/INT3	P4.1	P4.0

Mnemonic: ACC Address: E8h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P4.3	Port 4 Data bit which outputs to pin P4.3 at mode 0, or external Interrupt 2.
2	P4.2	Port 4 Data bit which outputs to pin P4.2 at mode 0, or external Interrupt 3.
1	P4.1	Port 4 Data bit which outputs to pin P4.1 at mode 0.
0	P4.0	Port 4 Data bit which outputs to pin P4.0 at mode 0.

PCA Counter Low Register

Bit:	7	6	5	4	3	2	1	0
	CL.7	CL.6	CL.6	CL.4	CL.3	CL.2	CL.1	CL.0

Mnemonic: CL Address: E9h

PCA Module 0 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP0L.7	CCAP0L.6	CCAP0L.5	CCAP0L.4	CCAP0L.3	CCAP0L.2	CCAP0L.1	CCAP0L.0

Mnemonic: CCAP0L Address: EAh

PCA Module 1 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP1L.7	CCAP1L.6	CCAP1L.5	CCAP1L.4	CCAP1L.3	CCAP1L.2	CCAP1L.1	CCAP1L.0

Mnemonic: CCAP1L Address: EBh

PCA Module 2 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP2L.7	CCAP2L.6	CCAP2L.5	CCAP2L.4	CCAP2L.3	CCAP2L.2	CCAP2L.1	CCAP2L.0

Mnemonic: CCAP2L Address: ECh

PCA Module 3 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP3L.7	CCAP3L.6	CCAP3L.5	CCAP3L.4	CCAP3L.3	CCAP3L.2	CCAP3L.1	CCAP3L.0

Mnemonic: CCAP3L Address: EDh

PCA Module 4 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP4L.7	CCAP4L.6	CCAP4L.5	CCAP4L.4	CCAP4L.3	CCAP4L.2	CCAP4L.1	CCAP4L.0

Mnemonic: CCAP4L Address: EEh

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

Chip Enable Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: CHPENR Address: F6h

PCA Counter High Register

Bit:	7	6	5	4	3	2	1	0
	CH.7	CH.6	CH.6	CH.4	CH.3	CH.2	CH.1	CH.0

Mnemonic: CH Address: F9h

PCA Module 0 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP0H.7	CCAP0H.6	CCAP0H.5	CCAP0H.4	CCAP0H.3	CCAP0H.2	CCAP0H.1	CCAP0H.0

Mnemonic: CCAP0H Address: FAh

PCA Module 1 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP1H.7	CCAP1H.6	CCAP1H.5	CCAP1H.4	CCAP1H.3	CCAP1H.2	CCAP1H.1	CCAP1H.0

Mnemonic: CCAP1H Address: FBh

PCA Module 2 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP2H.7	CCAP2H.6	CCAP2H.5	CCAP2H.4	CCAP2H.3	CCAP2H.2	CCAP2H.1	CCAP2H.0

Mnemonic: CCAP2H Address: FCh

PCA Module 3 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP3H.7	CCAP3H.6	CCAP3H.5	CCAP3H.4	CCAP3H.3	CCAP3H.2	CCAP3H.1	CCAP3H.0

Mnemonic: CCAP3H Address: FDh

PCA Module 4 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP4H.7	CCAP4H.6	CCAP4H.5	CCAP4H.4	CCAP4H.3	CCAP4H.2	CCAP4H.1	CCAP4H.0

Mnemonic: CCAP4H Address: FEh

8. PORT 4 AND BASE ADDRESS REGISTERS

Port 4, address E8H, is a 4-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation modes.

Mode 0: P4.0 – P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{INT3}$ and $\overline{INT2}$ if enabled.

Mode 1: P4.0 – P4.3 are read strobe signals that are synchronized with $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: P4.0 – P4.3 are write strobe signals that are synchronized with $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 3: P4.0 – P4.3 are read/write strobe signals that are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. The registers P4xAH and P4xAL contain the 16-bit base address of P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

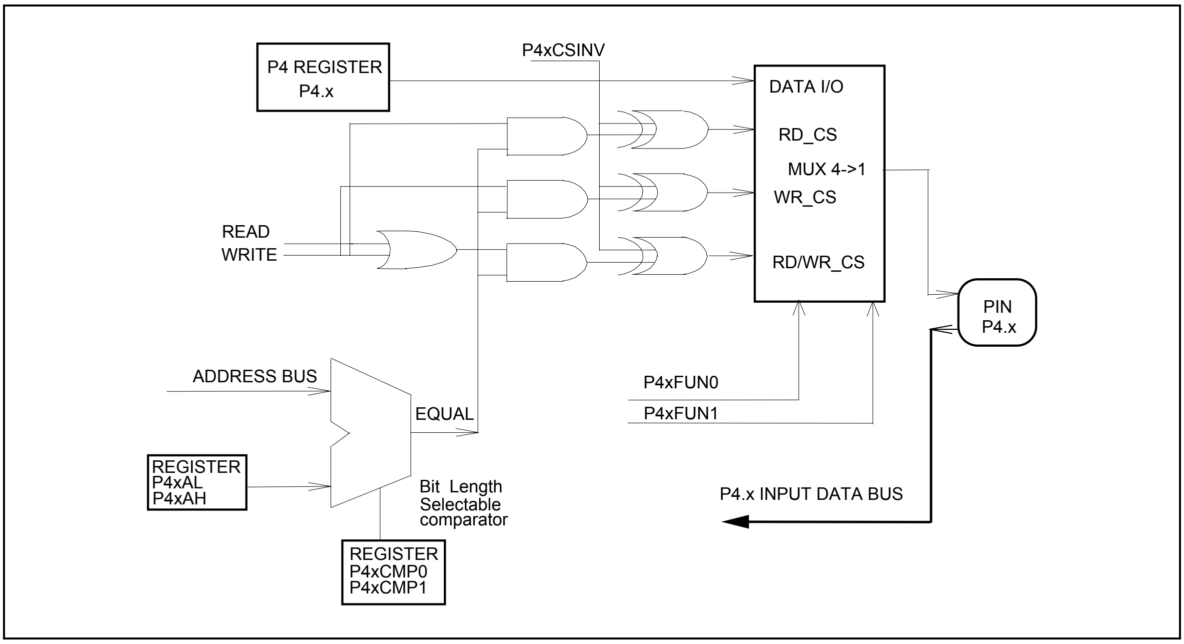
P4 (E8H)

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H – 1237H and positive polarity, and P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H             ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B      ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H            ; P4.1 – P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H            ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                             ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H – 1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3 – P4.1.



9. INTERRUPT

$\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{CLR}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

Nine-source interrupt information

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Programmable Counter Array	33H	4	IE.6	-
Serial Port	23H	5	IE.4	-
Timer/Counter 2	2BH	6	IE.5	-
External Interrupt 2	33H	7	XICON.2	XICON.0
External Interrupt 3	3BH	8 (lowest)	XICON.6	XICON.3

Four-level interrupt priority

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.X	IP.X	
0	0	Level 0(lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3(highest priority)

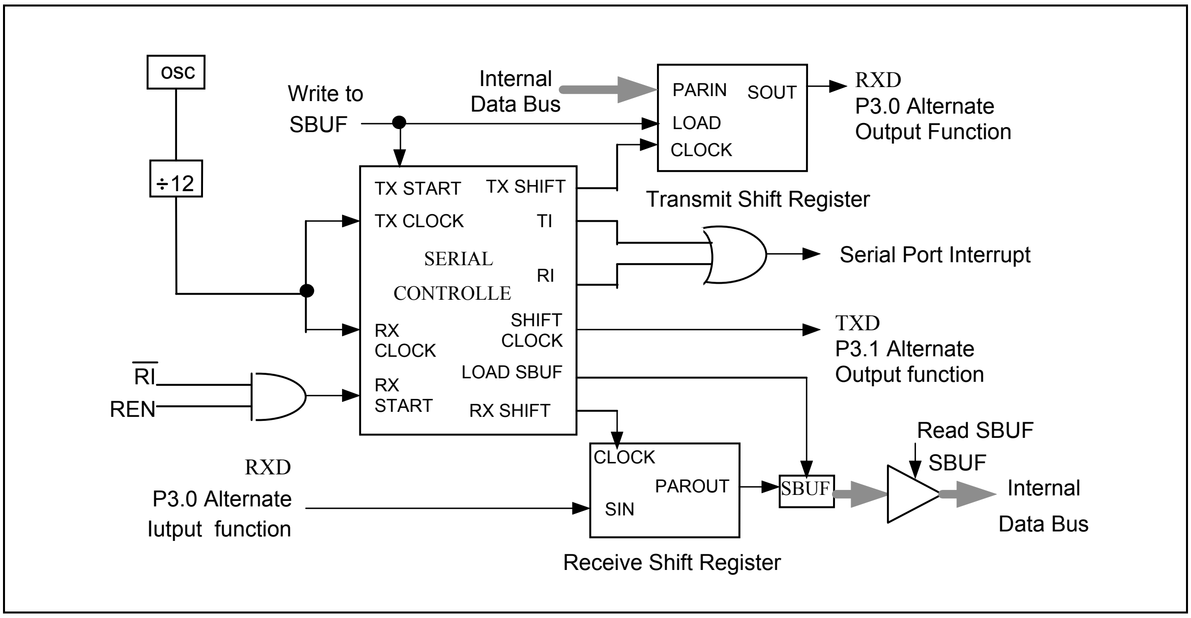
10. ENHANCED FULL DUPLEX SERIAL PORT

Serial port in the W78ERD2 is a full duplex port. The W78ERD2 provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W78ERD2 generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

10.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W78ERD2 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 of the oscillator frequency.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the W78ERD2 and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.



Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

10.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

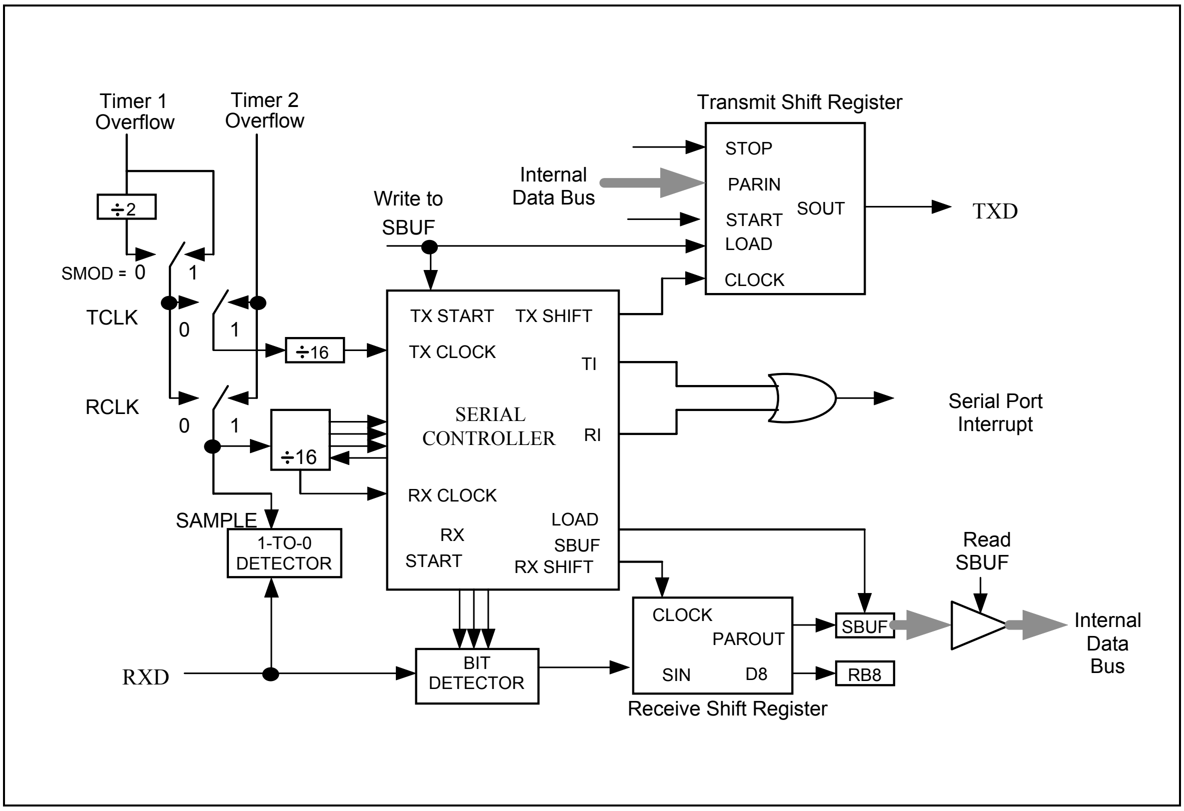
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

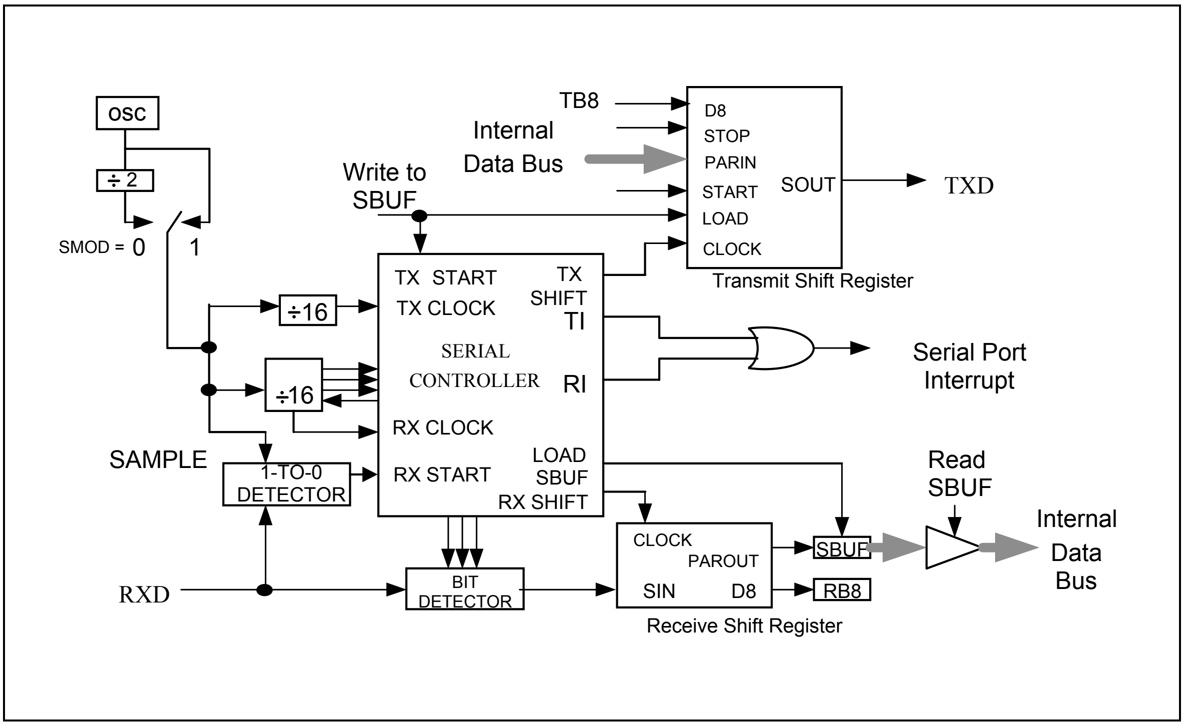
If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.



Serial Port Mode 1

10.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.



Serial Port Mode 2

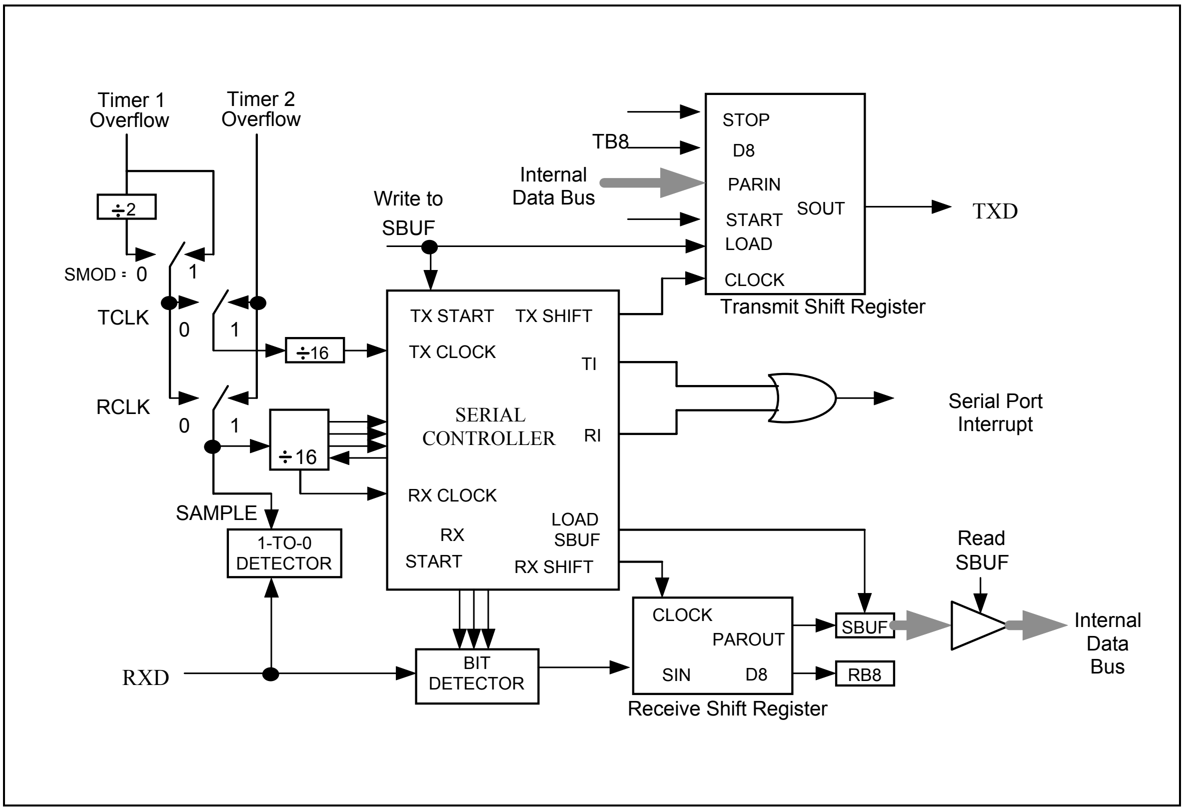
If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

10.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.



Serial Port Mode 3

Serial Ports Modes

SM1	SM0	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

10.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W78ERD2 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W78ERD2 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

10.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W78ERD2, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR	1010 0100
SADEN	1111 1010
Given	1010 0x0x

Slave 2:

SADDR	1010 0111
SADEN	1111 1001
Given	1010 0xx1

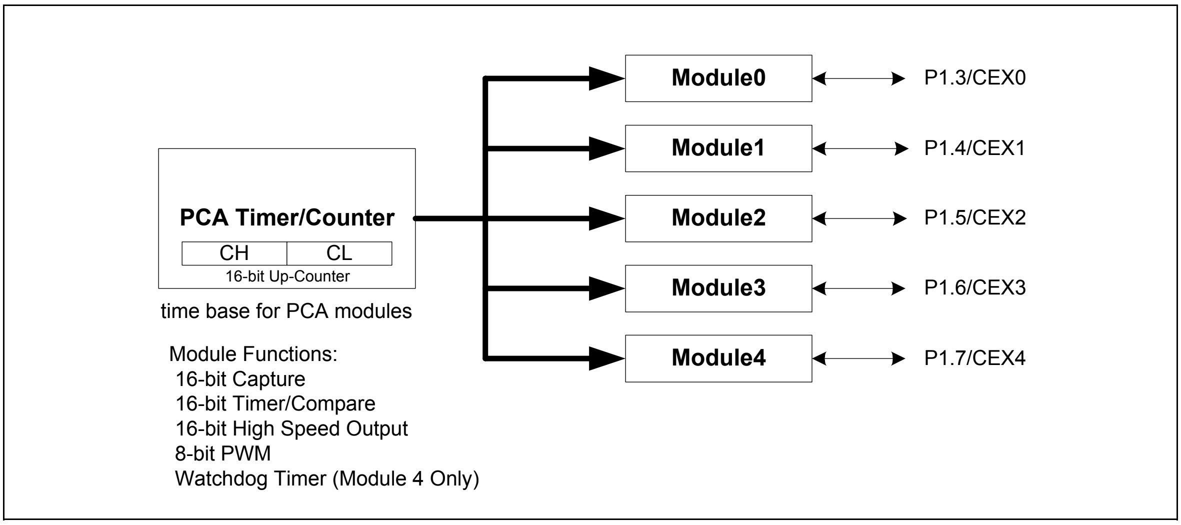
The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical ORing of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

11. PROGRAMMABLE COUNTER ARRAY (PCA)

The PCA is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associate with it in port 1. module0 is connected to p1.3(CEX0), module1 is connected to p1.4(CEX1), etc.



Programmable Counter Array (PCA)

Each module in the PCA has a special function register associated with it. These register are: CCAPM0 for module0, CCAPM1 for module1, etc. The registers contain the bits that control the mode that each module will operate in. The ECCF bit enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM enables the pulse width modulation mode. The TOG bit when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's compare/capture register. The match bit MAT when set will cause the CCF bit in the CCON register to be set when there is a match between the PCA counter and the module's compare/capture register. The bits CAPP and CAPN determine the edge that a capture input will be active on. The CAPP bit enables the positive edge, and the CAPN bit enables the negative edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The bit ECOM enables the comparator function.

The PCA Timer is a common time base for all five modules and can be programmed to select the different timer source. The default value is 12 clocks (T) per machine cycle. 12T / 6T can be set by the option bit. The option bits only are set by the writer. The timer count source is determined from the CPS1 and CPS2 bits in the CMOD SFR as follows:

CPS1	CPS0	PCA TIMER COUNT SOURCE FOR 12T	PCA TIMER COUNT SOURCE FOR 6T
0	0	Oscillator frequency / 12	Oscillator frequency / 6
0	1	Oscillator frequency / 4	Oscillator frequency / 2
1	0	Timer0 overflow	Timer0 overflow
1	1	External input at ECI pin	External input at ECI pin

CMOD(D8H)

BIT	NAME	FUNCTION
7	CILD	Counter idle control: CILD = 0 programs the PCA Counter to continue functioning during idle mode CILD = 1 programs it to be gated off during idle.
6	WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA module 4. WDTE = 1 enables it.
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	CPS1	PCA Count Pulse Select bit 1
1	CPS0	PCA Count Pulse Select bit 0
0	ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

There are three additional bits associated with the PCA in the CMOD SFR. They are CILD which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module4 (the watchdog timer is executed in module4), and ECF which when set causes an interrupt and the PCA overflow flag CF to be set when the PCA timer overflows.

CCON(D8H)

BIT	NAME	FUNCTION
7	CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off
5	-	Reserved
4	CCF4	PCA Module4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module to run the PCA the CR bit (CCON.6) must be set by software. The PCA is turned off by clearing this bit. The CF bit (CCON.7) is set when the PCA Counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. CCON.0~CCON.4 are the flags for the modules and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

CCAPMn

CCAPM0(DAH) , CCAPM1(DBH) , CCAPM2(DCH) , CCAPM3(DDH), CCAPM4(DEH)

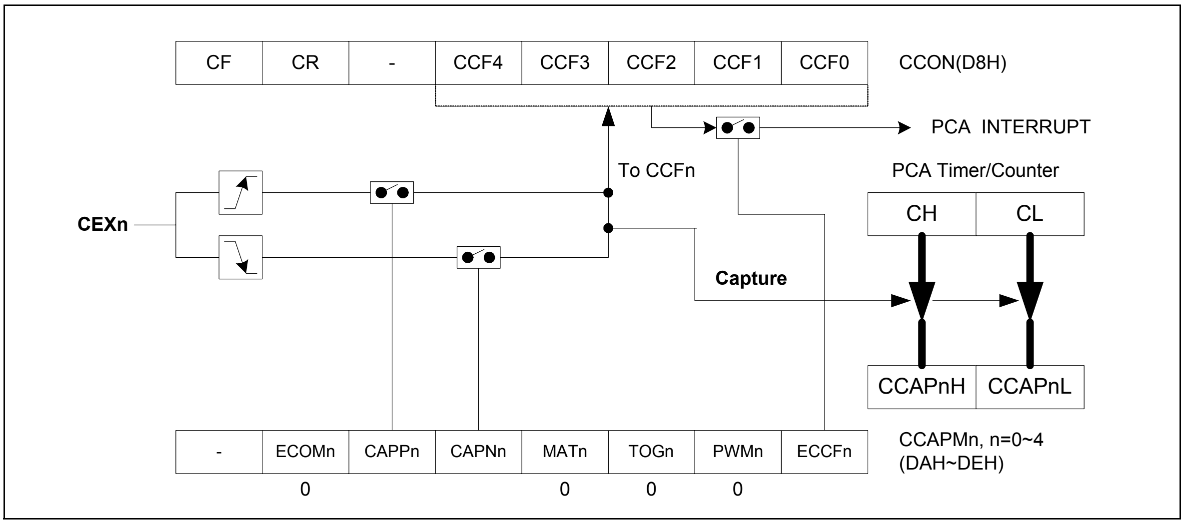
BIT	NAME	FUNCTION
7	-	Reserved
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function
5	CAPPn	Capture Positive. CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative. CAPNn = 1 enables negative edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
2	TOGn	Toggle. When TOGn = 1 a match of the PCA counter with this module's compare/capture register causes the CEXn bit to toggle.
1	PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn bit to be used as a pulse width modulated output.
0	ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

MODULE FUNCTION	ECOMN	CAPPN	CAPNN	MATN	TOGN	PWMN	ECCFN
No operation	0	0	0	0	0	0	0
16-bit capture by a positive edge trigger on CEXn	X	1	0	0	0	0	X
16-bit capture by a negative trigger on CEXn	X	0	1	0	0	0	X
16-bit capture by a transition on CEXn	X	1	1	0	0	0	X
16-bit Software Timer	1	0	0	1	0	0	X
16-bit High Speed Output	1	0	0	1	1	0	X
8-bit PWM	1	0	0	0	0	1	0
Watchdog Timer (only in module4)	1	0	0	1	X	0	X

PCA Module Modes (CCAPMn Register)

11.1 PCA Capture Mode

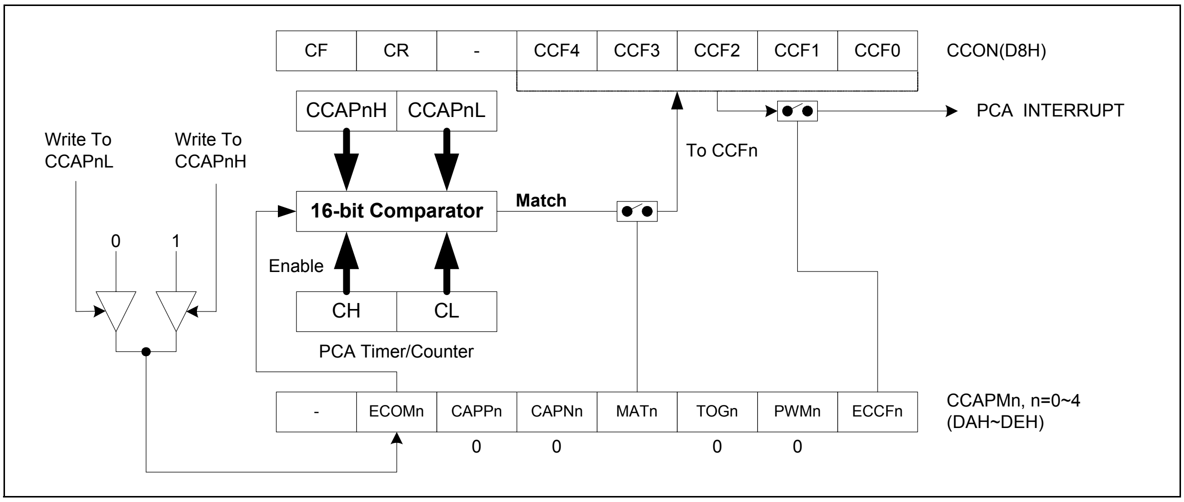
To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnH and CCAPnL). If the CCFn(CCON) bit for the module and the ECCFn(CCAPMn) bit are set then an interrupt will be generated.



PCA Capture Mode

11.2 16-bit Software Timer Comparator Mode

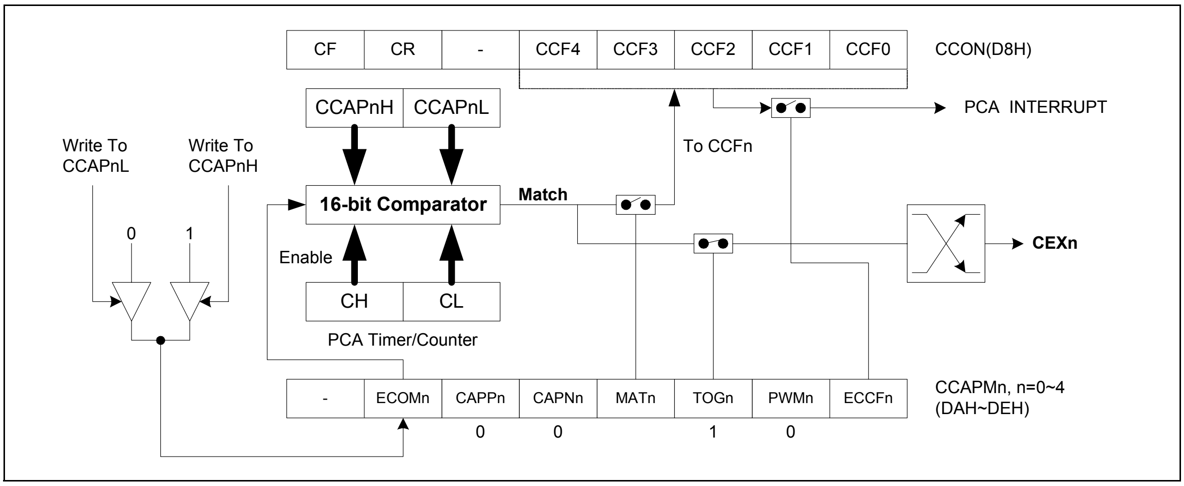
The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn(CCON) and the ECCFn(CCAPMn) bits for the module are both set.



PCA 16-bit Timer Comparator Mode

11.3 High Speed Output Mode

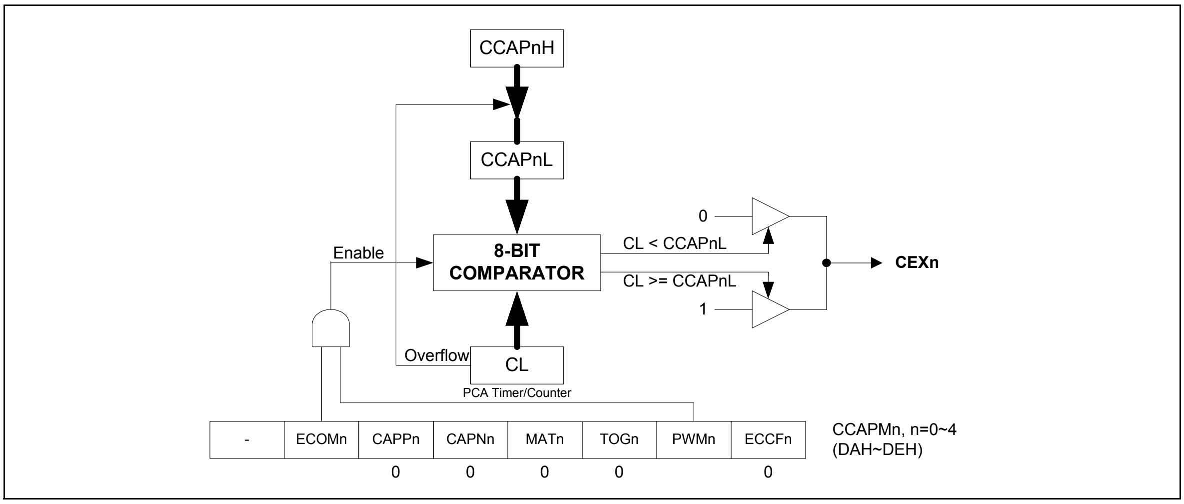
In this mode the CEX output (on port1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM(CCAPMn) bits must be set.



PCA High Speed Output Mode

11.4 Pulse Width Modulator Mode

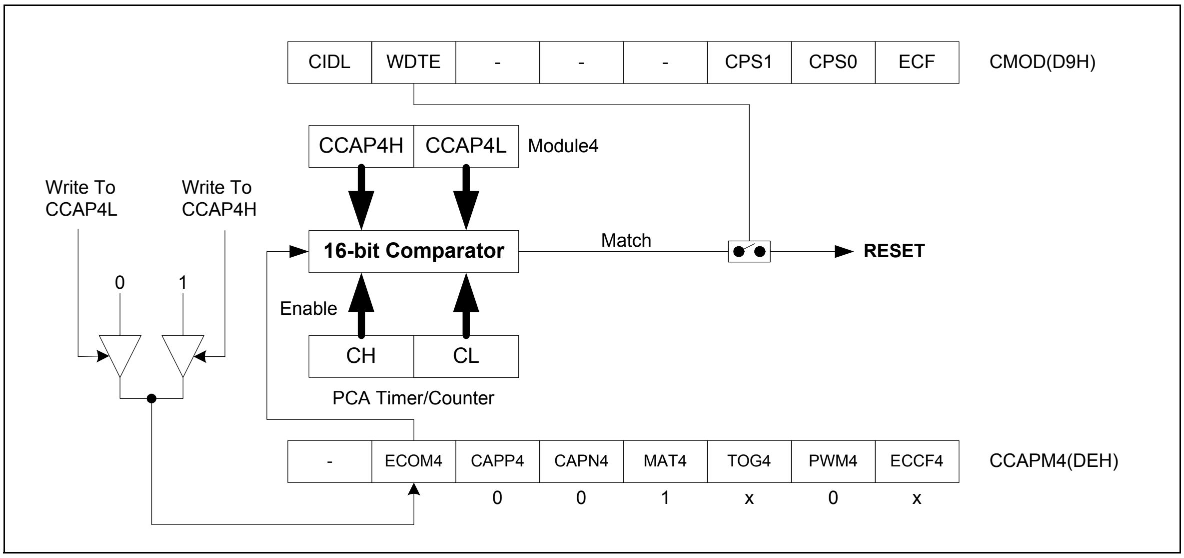
All of the PCA modules can be use as PWM outputs. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCApHn. This allows updating the PWM with out glitches. The PWM and ECOM(CCAPM) bits must be set to enable the PWM mode.



PAC PWM Mode

11.5 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor. The watchdog timer function is only implemented in module4. However, module4 can still be used for other modes if the watchdog is not needed. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be high.



PCA Watchdog Timer Mode

12. HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the Watchdog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and **there is no way to disable the WDT except through reset** (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output reset HIGH pulse at the RST-pin. It does not need the external pull-down resistor and pull-up CAP on the reset pin.

12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 3FFFH and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 3FFFH machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the reset pin. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset. The RESET high pulse width is 98 source clock at 12-clock mode, or 49 source clock at 6-clock mode.

13. DUAL DPTR

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them. The DPS bit status should be saved by software when switching between DPTR0 and DPTR1. Note that bit 2 can't be written and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the GF2 bits.

14. IN-SYSTEM PROGRAMMING (ISP) MODE

The W78ERD2 equips one 64K byte of main Flash EPROM bank for application program (called AP Flash EPROM) and one 4K byte of auxiliary Flash EPROM bank for loader program (called LD Flash EPROM). In the normal operation, the microcontroller executes the code in the AP Flash EPROM. If the content of AP Flash EPROM needs to be modified, the W78ERD2 allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78ERD2 achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of AP Flash EPROM, software located at AP Flash EPROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LD Flash EPROM. Because the device will clear the program counter while switching from AP Flash EPROM to LD Flash EPROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LD Flash EPROM area. The device offers software reset for switching back to AP Flash EPROM while the content of AP Flash EPROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as an external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip Flash EPROM in the in-system programming mode. SFRFAH contains the high-order byte of address, SFRFAL contains the low-order byte of address.

SFRFD: The programming data for on-chip Flash EPROM in programming mode.

SFRCN: The control byte of on-chip Flash EPROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. = 0: 64K bytes Flash EPROM bank is selected as destination for re-programming. = 1: 4K bytes Flash EPROM bank is selected as destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB AP Flash EPROM	0	0010	1	0	X	X
Program 64KB AP Flash EPROM	0	0001	1	0	Address in	Data in
Read 64KB AP Flash EPROM	0	0000	0	0	Address in	Data out
Erase 4KB LD Flash EPROM	1	0010	1	0	X	X
Program 4KB LD Flash EPROM	1	0001	1	0	Address in	Data in
Read 4KB LD Flash EPROM	1	0000	0	0	Address in	Data out

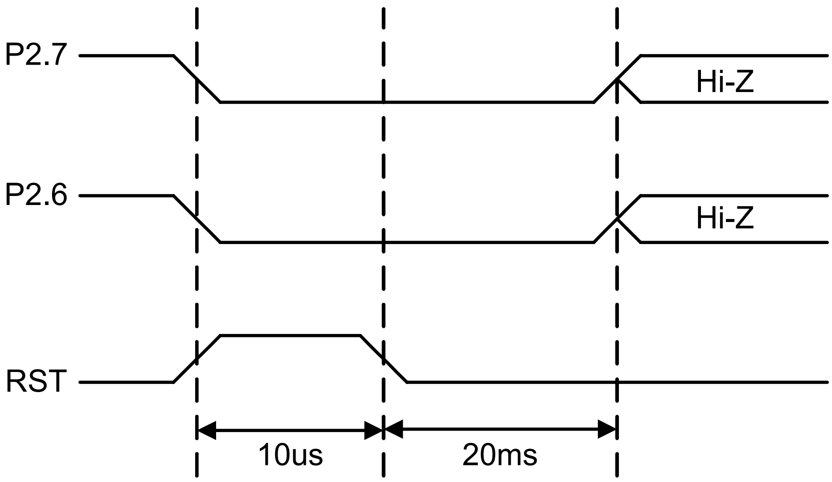
15. H/W REBOOT MODE (BOOT FROM LDROM)

By default, the W78ERD2 boots from AP Flash EPROM program after a power on reset. On some occasions, user can force the W78ERD2 to boot from the LD Flash EPROM program via following settings. The possible situation that you need to enter H/W REBOOT mode when the AP Flash EPROM program can not run properly and device can not jump back to LD Flash EPROM to execute in-system programming function. Then you can use this H/W REBOOT mode to force the W78ERD2 jumps to LD Flash EPROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the AP Flash EPROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78ERD2 to enter the H/W REBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the AP Flash EPROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or H/W REBOOT mode.

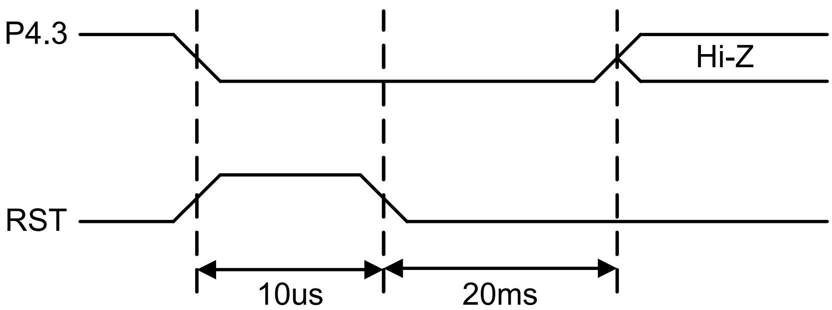
H/W REBOOT MODE

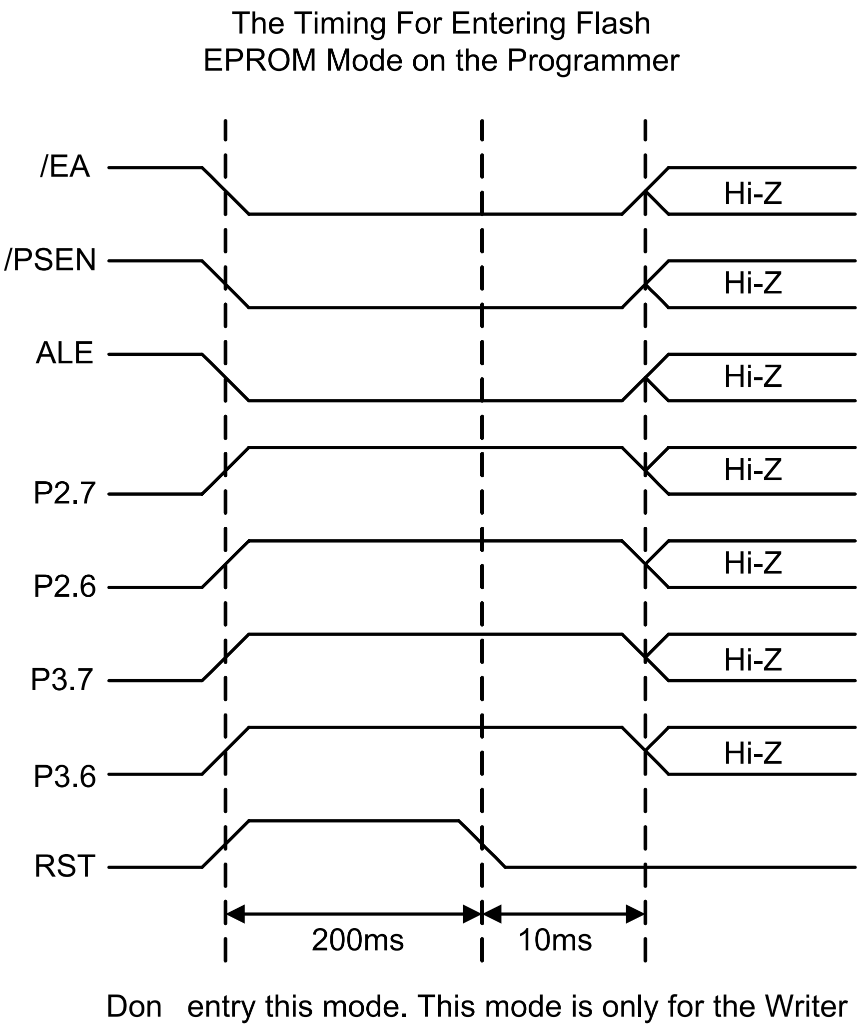
P4.3	P2.7	P2.6	OPTION BIT	MODE
X	L	L	Bit4 = L	H/W REBOOT
L	X	X	Bit5 = L	H/W REBOOT

The Reset Timing For Entering H/W
REBOOT Mode 1

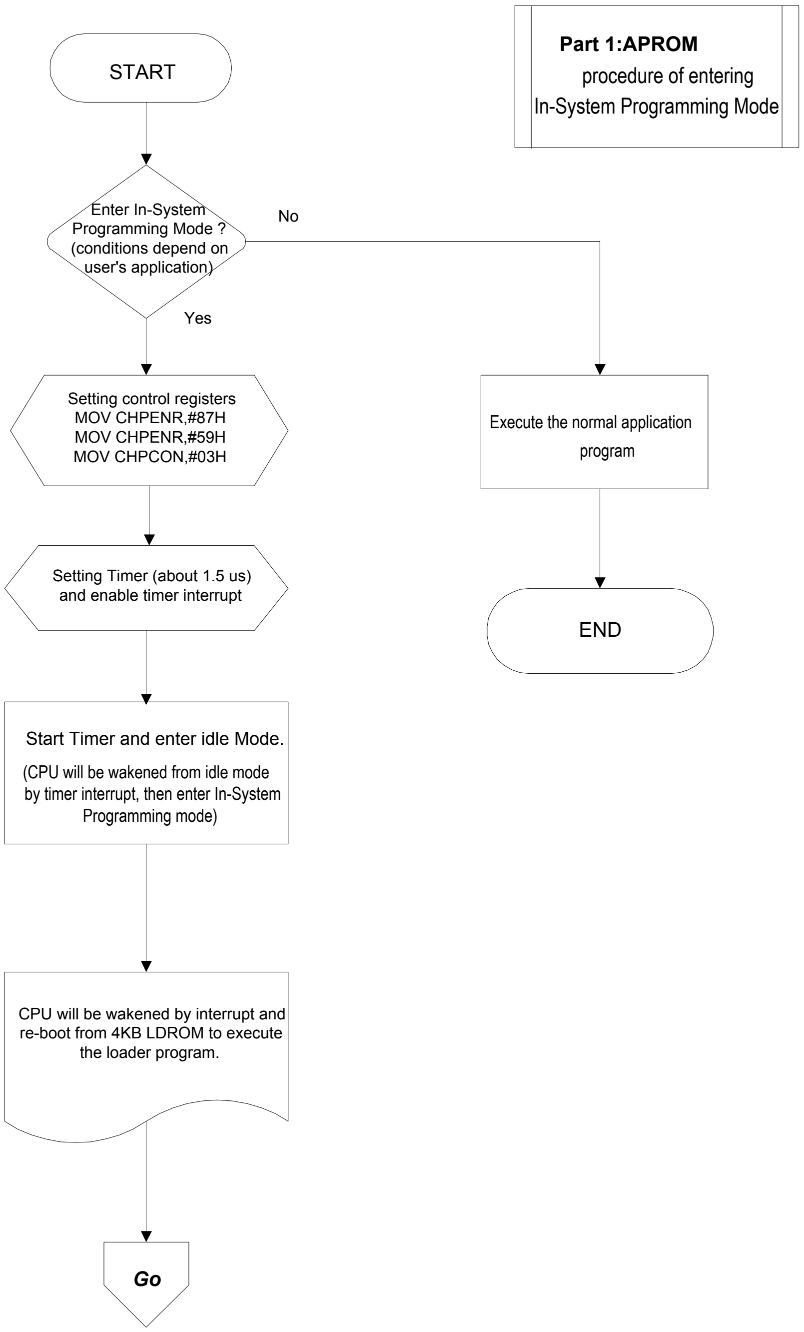


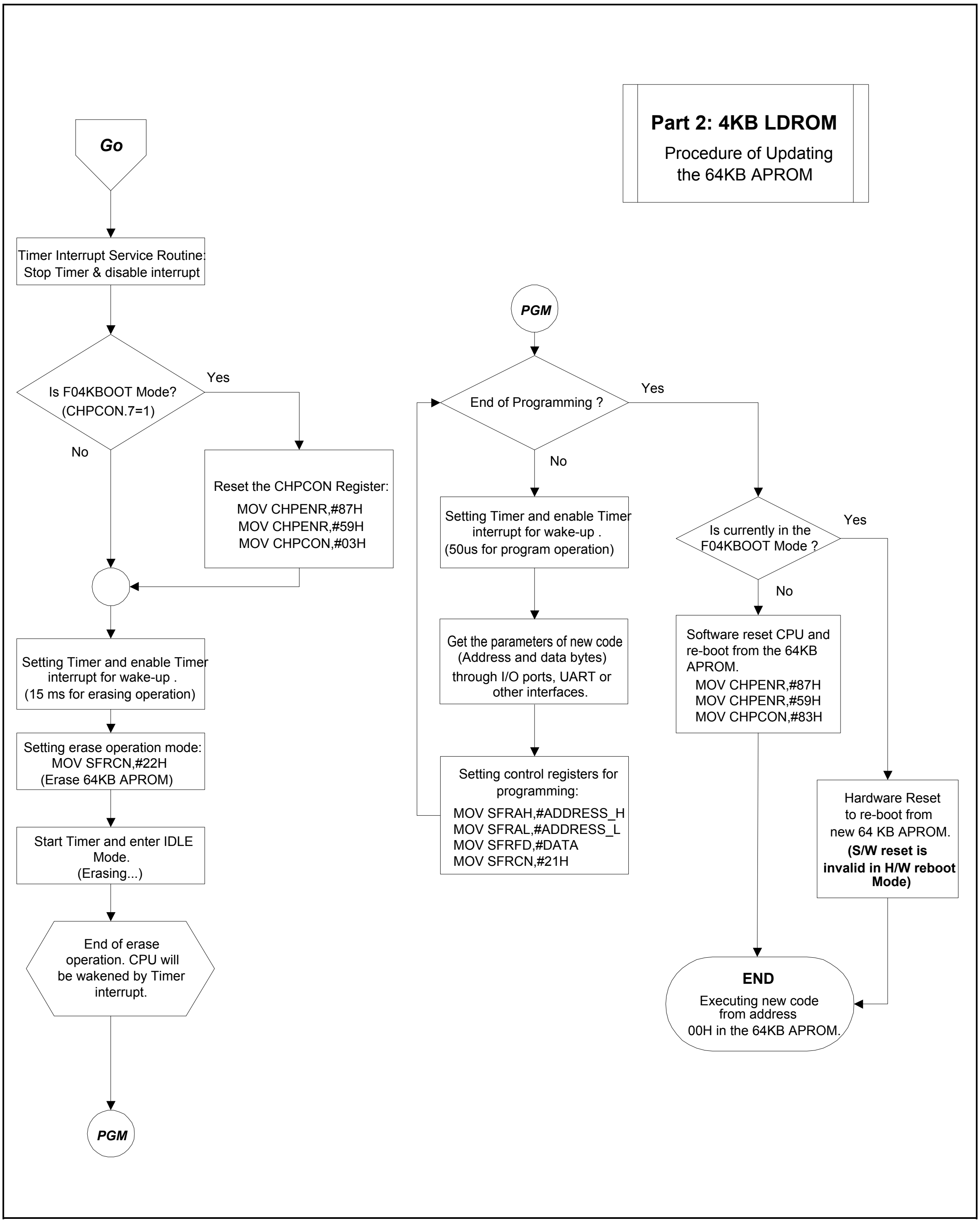
H/W REBOOT Mode 2




The Timing For Entering Flash
EPROM Mode on the Programmer
/EA
/PSEN
ALE
P2.7
P2.6
P3.7
P3.6
RST
Hi-Z
Hi-Z
Hi-Z
Hi-Z
Hi-Z
Hi-Z
Hi-Z
200ms
10ms
Don   entry this mode. This mode is only for the Writer

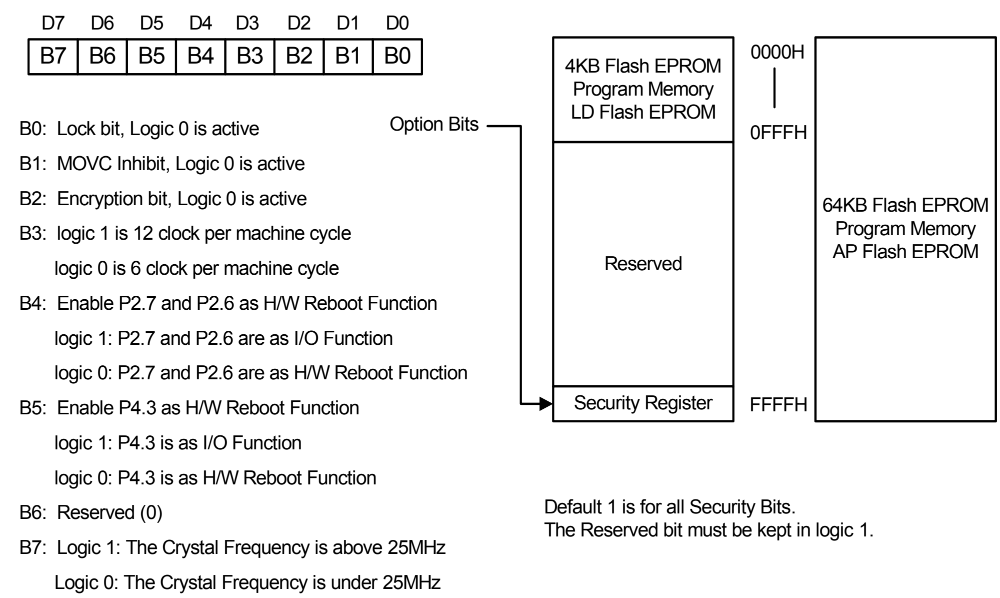
The Algorithm of In-System Programming




Part 2: 4KB LDROM
Procedure of Updating the 64KB APROM
Go
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for wake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV SFRCN,#22H (Erase 64KB APROM)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU will be wakened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for wake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Software reset CPU and re-boot from the 64KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardware Reset to re-boot from new 64 KB APROM.
(S/W reset is invalid in H/W reboot Mode)
END
Executing new code from address 00H in the 64KB APROM.

16. OPTION BITS

During the on-chip Flash EPROM programming mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.



Special Setting Register

Lock bit

This bit is used to protect the customer's program code in the W78ERD2. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

Oscillator Control

W78ERD2 allow user to diminish the gain of on-chip oscillator amplifier by using programmer to set the bit B7 of option bits register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may improperly affect the external crystal operation at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

17. ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

17.2 D.C. Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	10	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	μA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	0	+300	μA	V_{DD} = 5.5V 0< V_{IN} <V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 5.5V 0V< V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL}[*4]	-500	-	μA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V

D.C. Electrical Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P3, P4	Isk1	4	8	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Sink Current P0, P2, ALE, $\overline{PSEN}$	Isk2	10	15	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 µA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 µA
Source Current P1, P2, P3, P4	Isr1	-180	-300	µA	V_{DD} = 4.5V V_{IN} = 2.4V
Source Current P0, P2, ALE, $\overline{PSEN}$	Isr2	-8	-12	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*3. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

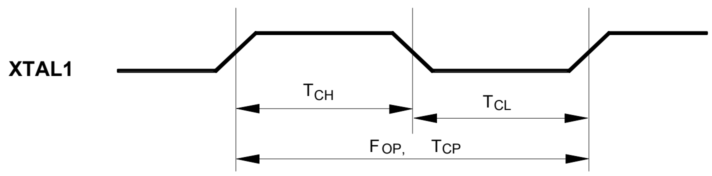
*4. XTAL1 is a CMOS input.

*5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

17.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{RD}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{RD}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{RD}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

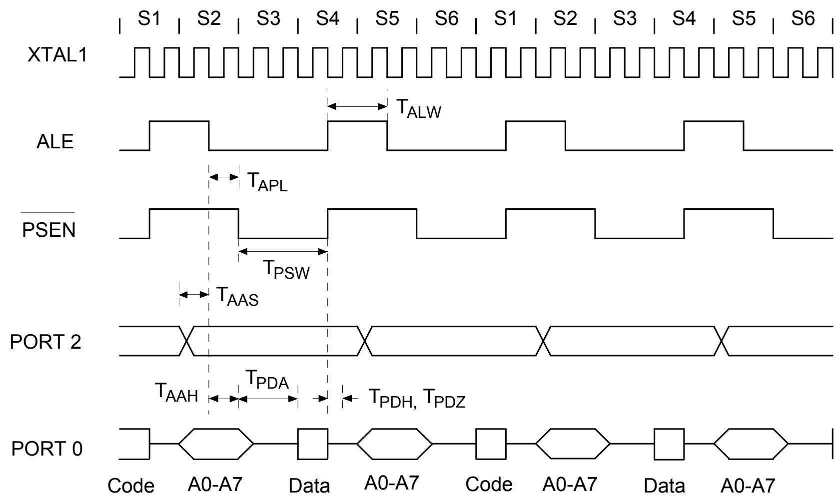
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

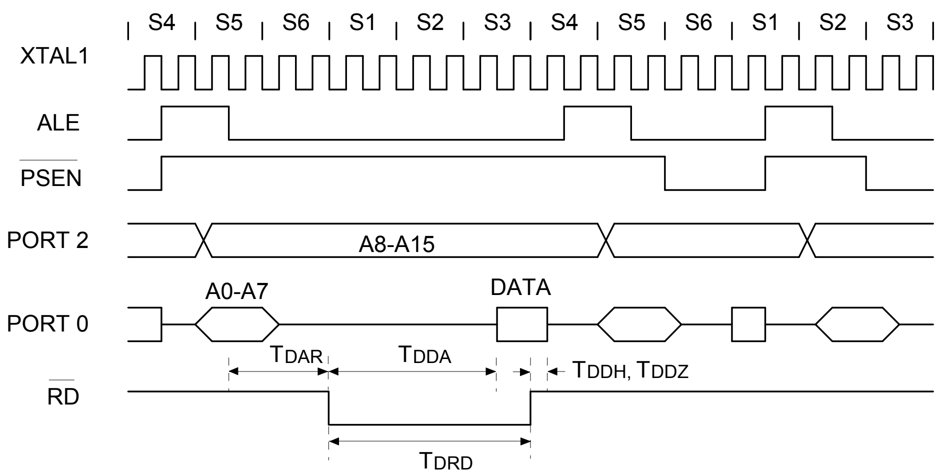
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

18. TIMING WAVEFORMS

Program Fetch Cycle

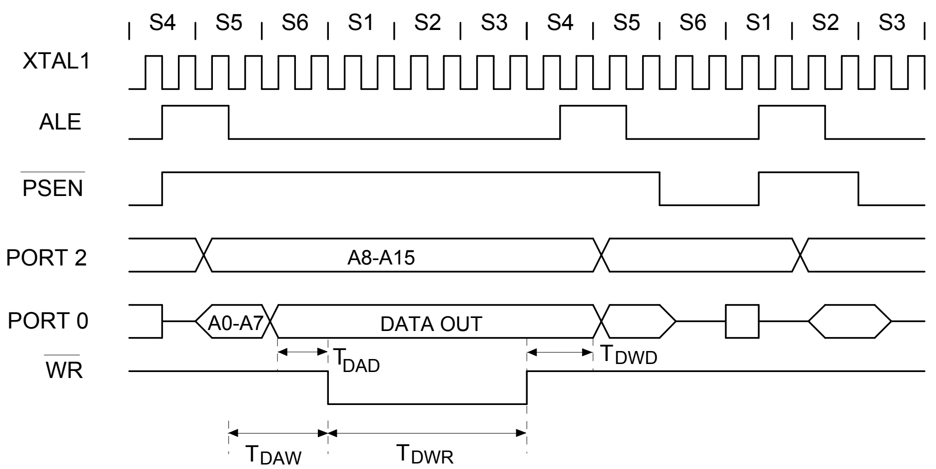


Data Read Cycle

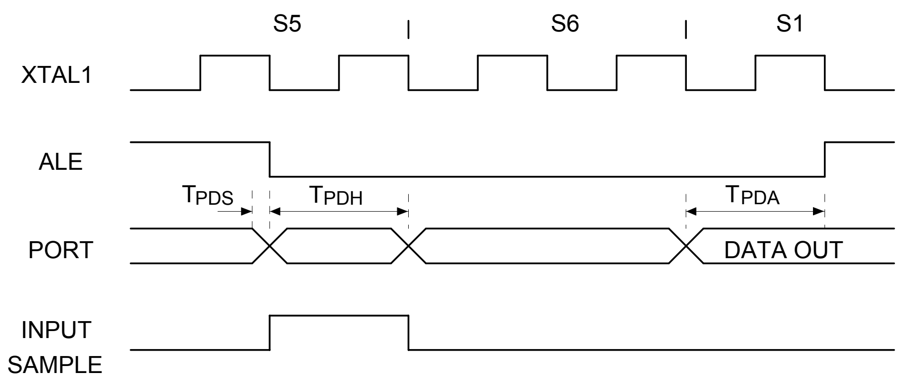


Timing Waveforms, continued

Data Write Cycle



Port Access Cycle



Winbond Electronics Corp.

19. TYPICAL APPLICATION CIRCUITS

19.1 External Program Memory and Crystal

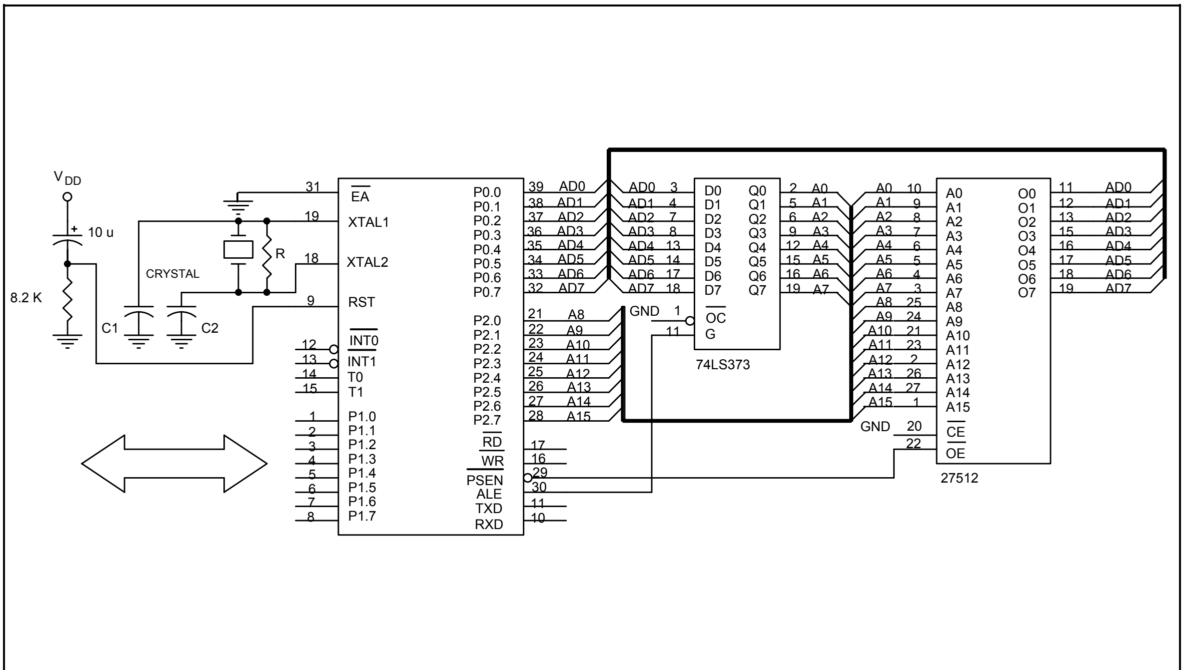


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	15P	-
32 MHz	10P	10P	6.8K
40 MHz	1P	1P	3 K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuits, continued

19.2 Expanded External Data Memory and Oscillator

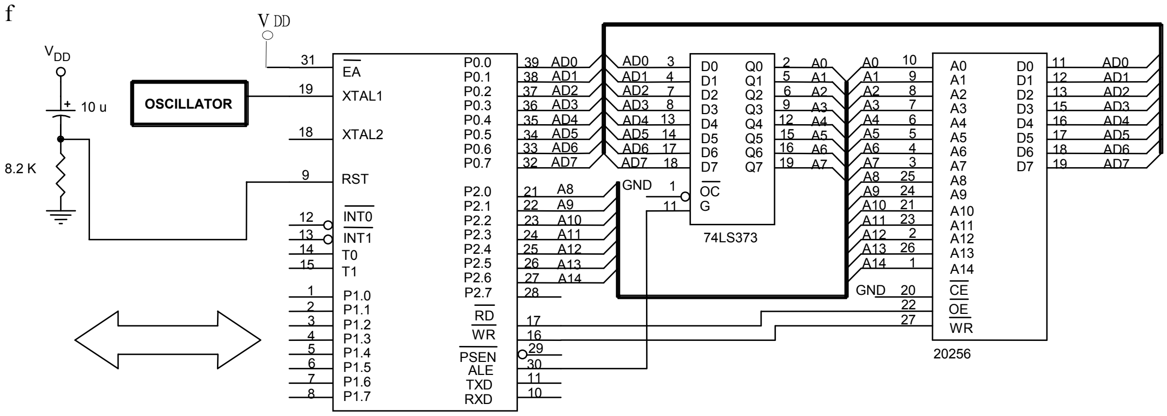
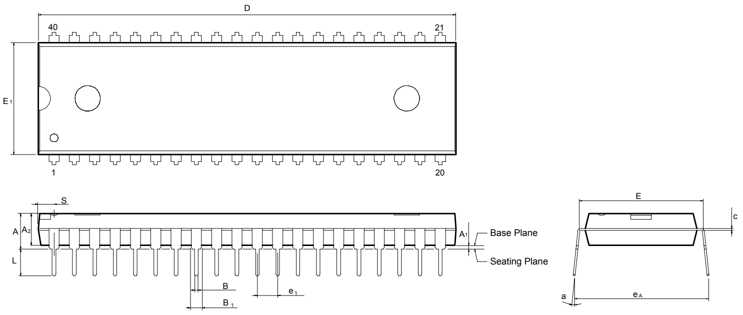


Figure B

20. PACKAGE DIMENSIONS

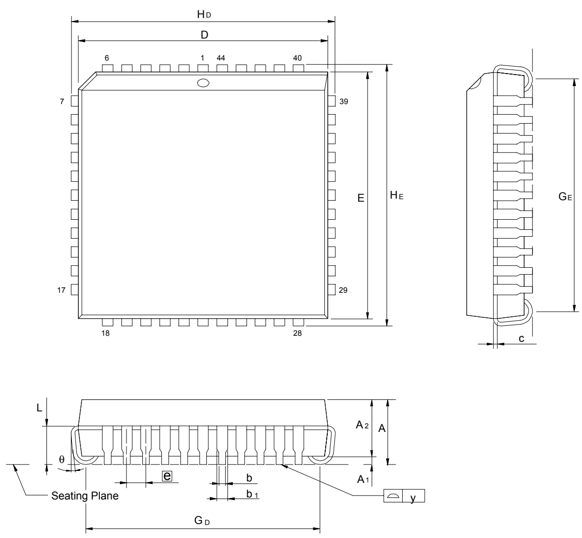
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

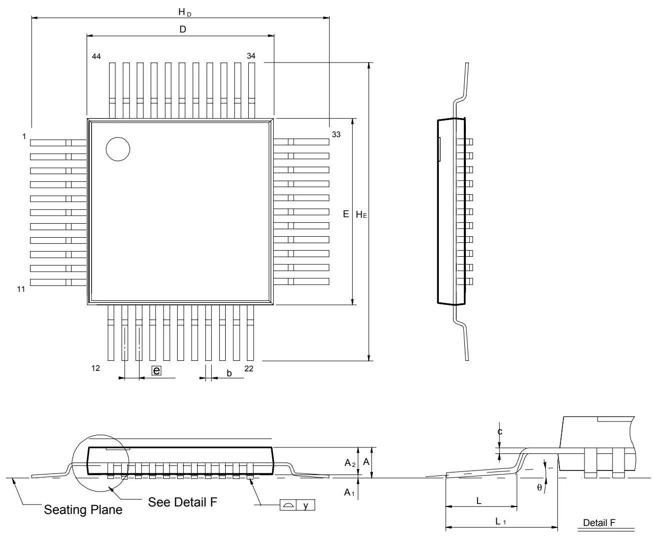


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
$\boxed{e}$		0.050 BSC			1.27 BSC	
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued.

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
$\boxed{e}$	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

21. APPLICATION NOTE

21.1 In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78ERD2 Flash EPROM microcontroller. In this example, microcontroller will boot from 64 KB AP Flash EPROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64 KB AP Flash EPROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LD Flash EPROM bank. The loader program erases the 64 KB AP Flash EPROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB AP Flash EPROM.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of 64K AP Flash EPROM program: Program will scan the P1.0. if P1.0 = 0, enters
;* in-system Programming mode for updating the content of AP Flash EPROM code else executes the
;* current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU    BFH
        CHPENR    EQU    F6H
        SFRAL     EQU    C4H
        SFRAH     EQU    C5H
        SFRFD     EQU    C6H
        SFRCN     EQU    C7H

        ORG    0H
        LJMP   100H                  ; JUMP TO MAIN PROGRAM
   ;************************************************************************
   ;*  TIMER0 SERVICE VECTOR ORG = 000BH
   ;************************************************************************
        ORG    00BH
        CLR    TR0                   ; TR0 = 0, STOP TIMER0
        MOV    TL0, R6
        MOV    TH0, R7
        RETI
   ;************************************************************************
   ;*  64K AP Flash EPROM MAIN PROGRAM
   ;************************************************************************
       ORG 100H

MAIN_64K:
        MOV A, P1                     ; SCAN P1.0
        ANL A, #01H
        CJNE A, #01H, PROGRAM_64K     ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H              ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR, #59H              ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H              ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
```

```
        MOV TCON, #00H              ; TR = 0 TIMER0 STOP
        MOV IP, #00H                ; IP = 00H
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMABILITY
;*******************************************************************************
;* Normal mode 64KB AP Flash EPROM program: depending user's application
;*******************************************************************************
NORMAL_MODE:
        .                           ; User's application program
        .
        .
        .
```

EXAMPLE 2:

```
;*****************************************************************************************************************
;* Example of 4KB LD Flash EPROM program: This lorder program will erase the 64KB AP Flash EPROM
;* first,then reads the new ;* code from external SRAM and program them into 64KB AP Flash EPROM bank.
;* XTAL = 40MHz
;*****************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON      EQU     BFH
    CHPENR      EQU     F6H
    SFRAL       EQU     C4H
    SFRAH       EQU     C5H
    SFRFD       EQU     C6H
    SFRCN       EQU     C7H

        ORG     000H
        LJMP    100H                ; JUMP TO MAIN PROGRAM
;************************************************************************
;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
;************************************************************************
        ORG 000BH
        CLR   TR0                   ; TR0 = 0, STOP TIMER0
        MOV TL0, R6
        MOV TH0, R7
        RETI
;************************************************************************
;*  4KB LD Flash EPROM MAIN PROGRAM
;************************************************************************
        ORG 100H
```

```
MAIN_4K:
        MOV SP, #C0H            ; BE INITIAL SP REGISTER
        MOV CHPENR, #87H        ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H        ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV A, CHPCON
        ANL A, #80H
        CJNE A, #80H, UPDATE_64K; CHECK H/W REBOOT MODE ?

        MOV CHPCON, #03H        ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV TMOD, #01H          ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE

UPDATE_64K:
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H          ; TMOD = 01H, MODE1
        MOV R6, #3CH            ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                                ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B0H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H         ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H          ; READ 64KB AP Flash EPROM MODE
        MOV SFRAH, #0H          ; START ADDRESS = 0H
        MOV SFRAL, #0H
        MOV R6, #FBH            ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0                ; ENABLE TIMER 0
        MOV PCON, #01H          ; ENTER IDLE MODE
        MOV A, SFRFD            ; READ ONE BYTE
```

```
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL              ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*****************************************************************************
;* RE-PROGRAMMING 64KB AP Flash EPROM BANK
;*****************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H          ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H           ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H           ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H          ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1          ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H        ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH           ; SET TIMER FOR PROGRAMMING, ABOUT 50 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2          ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR          ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A           ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H         ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H         ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;*****************************************************************************
; * VERIFY 64KB AP Flash EPROM BANK
;*****************************************************************************
        MOV R4, #03H           ; ERROR COUNTER
        MOV R6, #FBH           ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H          ; The start address of sample code
        MOV R2, #0H            ; Target low byte address
        MOV R1, #0H            ; Target high byte address
        MOV SFRAH, R1          ; SFRAH, Target high address
        MOV SFRCN, #00H        ; SFRCN = 00 (Read ROM CODE)
```

```
READ_VERIFY_64K:
        MOV SFRAL, R2        ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H       ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #0H, READ_VERIFY_64K

;*********************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*********************************************************************************
        MOV CHPENR, #87H        ; CHPENR = 87H
        MOV CHPENR, #59H        ; CHPENR = 59H
        MOV CHPCON, #83H        ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
        DJNZ R4, UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .                       ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

21.2 How to Use Programmable Counter Array

Please refer to Winbond website http://www.winbond.com.tw to get the application note.

22. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 2004	-	Initial Issued
A2	August 2004	36	Modify the content of PCA
		71	Add the application of PCA
A3	Sep. 30, 2004	38	Add Enhanced full duplex serial port with framing error detection and automatic address recognition
A4	April 20, 2005	72	Add Important Notice

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