PROGRAMMABLE 27-BIT DISPLAY SERIAL INTERFACE TRANSMITTER

FEATURES

- **FlatLink™3G serial interface technology**
- **Compatible with FlatLink3G receivers such as SN65LVDS302 (product under preview)**
- **Input supports 24-bit RGB video mode interface**
- **24-Bit RGB Data, 3 Control Bits, 1 Parity Bit and 2 Reserved Bits Transmitted over 1, 2 or 3 Differential Lines**
- **SubLVDS Differential Voltage Levels**
- **Effective Data Throughput up to 1755Mbps**
- **Three Operating Modes to Conserve Power**
  - **Active-Mode QVGA 17.4 mW (typ)**
  - **Active-Mode VGA 28.8 mW (typ)**
  - **Shutdown Mode ≈ 0.5 μA (typ)**
  - **Standby Mode ≈ 0.5 μA (typ)**
- **Bus Swap for Increased PCB Layout Flexibility**
- **1.8-V Supply Voltage**
- **ESD Rating > 2 kV (HBM)**
- **Typical Application: Host-Controller to Display-Module Interface**
- **Pixel Clock Range of 4 MHz–65 MHz**
- **Failsafe on all CMOS Inputs**
- **Packaging: 80 Pin 5 mm × 5 mm μBGA®**
- **Very low EMI meets SAE J1752/3 'M'-spec**

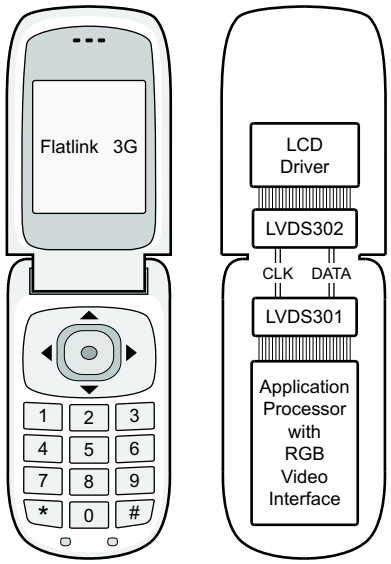
DESCRIPTION

The SN65LVDS301 serializer device converts 27 parallel data inputs to 1, 2, or 3 Sub Low-Voltage Differential Signaling (SubLVDS) serial outputs. It loads a shift register with 24 pixel bits and 3 control bits from the parallel CMOS input interface. In addition to the 27 data bits, the device adds a parity bit and two reserved bits into a 30-bit data word. Each word is latched into the device by the pixel clock (PCLK). The parity bit (odd parity) allows a receiver to detect single bit errors. The serial shift register is uploaded at 30, 15, or 10 times the pixel-clock data rate depending on the number of serial links used. A copy of the pixel clock is output on a separate differential output.

FPC cabling typically interconnects the SN65LVDS301 with the display. Compared to parallel signaling, the LVDS301 outputs significantly reduce the EMI of the interconnect by over 20dB. The electromagnetic emission of the device itself is very low and meets the meets SAE J1752/3 'M'-spec. (see Figure 31)

The SN65LVDS301 supports three power modes (Shutdown, Standby and Active) to conserve power. When transmitting, the PLL locks to the incoming pixel clock PCLK and generates an internal high-speed clock at the line rate of the data lines. The parallel data are latched on the rising or falling edge of PCLK as selected by the external control signal CPOL. The serialized data is presented on the serial outputs D0, D1, D2 with a recreated PCLK generated from the internal high-speed clock, output on the CLK output. If PCLK stops, the device enters a standby mode to conserve power

The parallel (CMOS) input bus offers a bus-swap feature. The SWAP pin configures the input order of the pixel data to be either R[7:0]. G[7:0], B[7:0], VS, HS, DE or B[0:7]. G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the host controller pinout or to put the transmitter device on the top side or the bottom side of the PCB.



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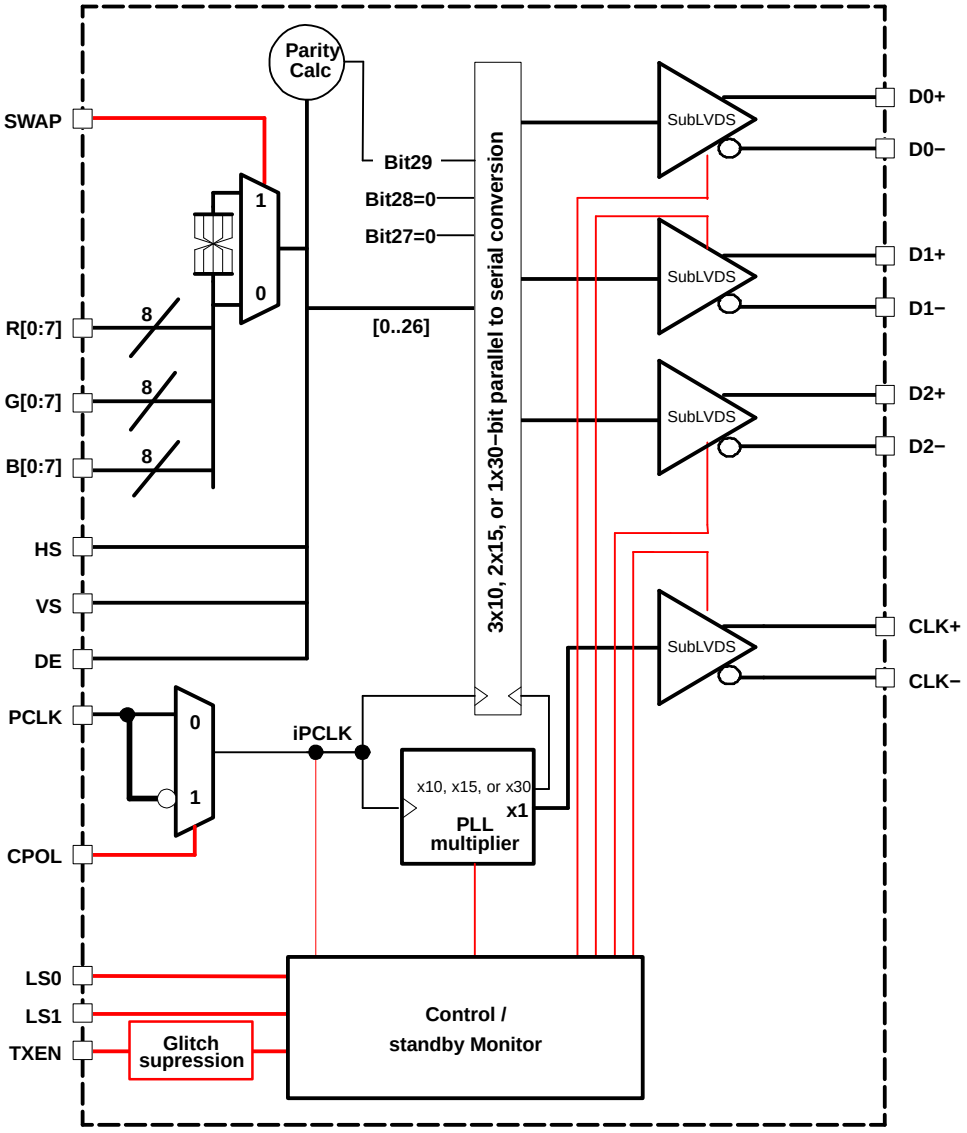
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Two Link Select lines LS0 and LS1 control whether 1, 2 or 3 serial links are used. The TXEN input may be used to put the SN65LVDS301 in a shutdown mode. The SN65LVDS301 enters an active Standby mode if the input clock PCLK stops. This minimizes power consumption without the need for controlling an external pin. The SN65LVDS301 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS inputs offer failsafe to protect the input from damage during power-up and to avoid current flow into the device inputs during power-up. An input voltage of up to 2.165 V can be applied to all CMOS inputs while VDD is between 0V and 1.65V.

Functional Block Diagram



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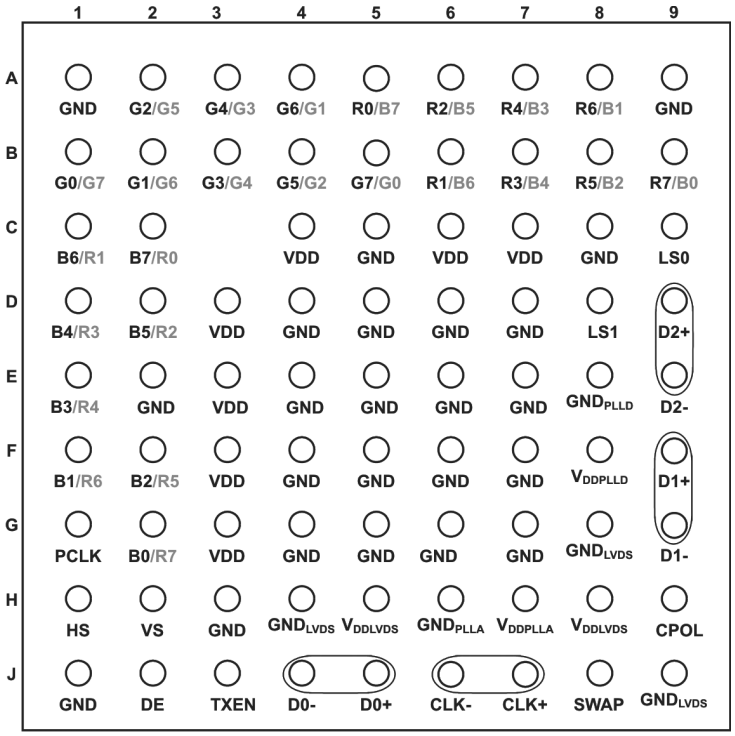
PINOUT - TOP VIEW



RGB Input pin assignment based on SWAP pin setting:

SWAP=0/SWAP=1

SWAP PIN FUNCTIONALITY

The SWAP pin allows the pcb designer to reverse the RGB bus, thus minimize potential signal crossovers due to signal routing. The two drawings beneath show the RGB signal pin assignment based on the SWAP pin setting.

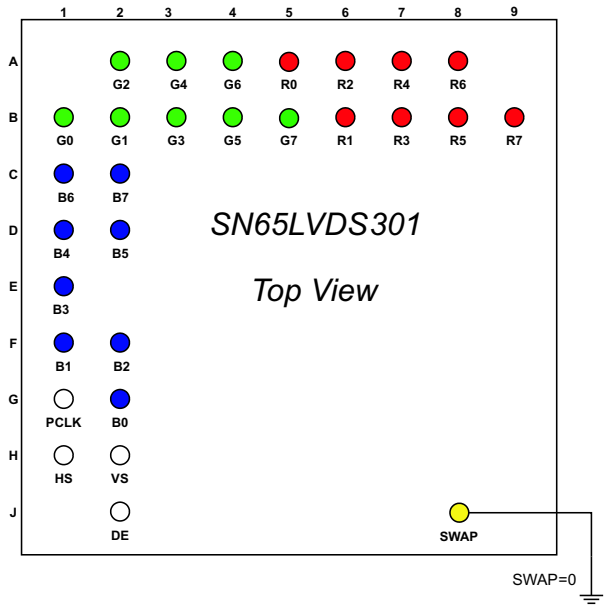


Figure 1. SWAP PIN = 0

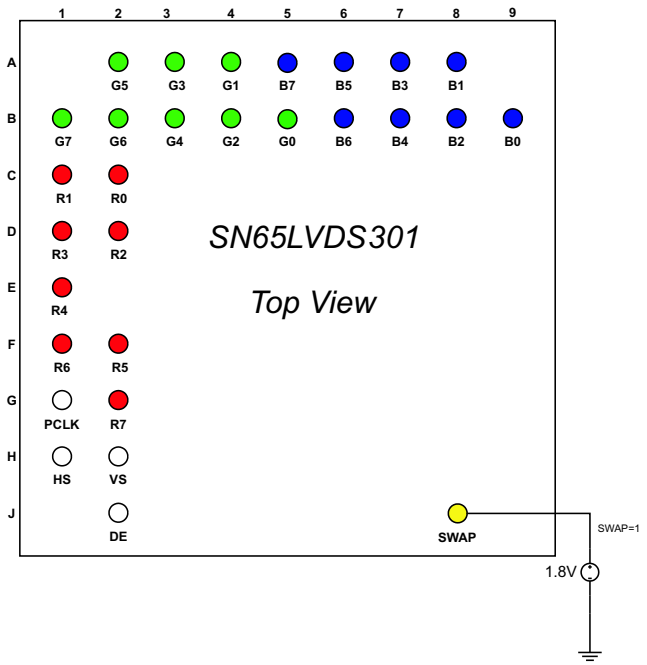


Figure 2. SWAP PIN = 1

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Table 1. NUMERIC PIN LIST

PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL
A1	—	GND	**C1**	0	B6	**F1**	0	B1
A2	0	G2		1	R1		1	R6
	1	G5	**C2**	0	B7	**F2**	0	B2
A3	0	G4		1	R0		1	R5
	1	G3	**C3**	UNPOPULATED		**F3**	—	V_{DD}
A4	0	G6	**C4**	—	VDD	**F4**	—	GND
	1	G1	**C5**	—	GND	**F5**	—	GND
A5	0	R0	**C6**	—	VDD	**F6**	—	GND
	1	B7	**C7**	—	VDD	**F7**	—	GND
A6	0	R2	**C8**	—	GND	**F8**	—	V_{DDPLLD}
	1	B5	**C9**	—	LS0	**F9**	—	D1+
A7	0	R4	**D1**	0	B4	**G1**	—	PCLK
	1	B3		1	R3	**G2**	0	B0
A8	0	R6	**D2**	0	B5		1	R7
	1	B1		1	R2	**G3**	—	V_{DD}
A9	—	GND	**D3**	—	VDD	**G4**	—	GND
B1	0	G0	**D4**	—	GND	**G5**	—	GND
	1	G7	**D5**	—	GND	**G6**	—	GND
B2	0	G1	**D6**	—	GND	**G7**	—	GND
	1	G6	**D7**	—	GND	**G8**	—	GND_{LVDS}
B3	0	G3	**D8**	—	LS1	**G9**	—	D1–
	1	G4	**D9**	—	D2+	**H1**	—	HS
B4	0	G5	**E1**	0	B3	**H2**	—	VS
	1	G2		1	R4	**H3**	—	GND
B5	0	G7	**E2**	—	GND	**H4**	—	GND_{LVDS}
	1	G0	**E3**	—	VDD	**H5**	—	V_{DDLVDS}
B6	0	R1	**E4**	—	GND	**H6**	—	GND_{PLLA}
	1	B6	**E5**	—	GND	**H7**	—	V_{DDPLLA}
B7	0	R3	**E6**	—	GND	**H8**	—	V_{DDLVDS}
	1	B4	**E7**	—	GND	**H9**	—	CPOL
B8	0	R5	**E8**	—	GND_{PLLD}	**J1**	—	GND
	1	B2	**E9**	—	D2–	**J2**	—	DE
B9	0	R7				**J3**	—	TXEN
	1	B0				**J4**	—	D0–
						J5	—	D0+
						J6	—	CLK–
						J7	—	CLK+
						J8	—	SWAP
						J9	—	GND_{LVDS}

TERMINAL FUNCTIONS

NAME	I/O	DESCRIPTION
D0+, D0–	SubLVDS Out	SubLVDS Data Link (active during normal operation)
D1+, D1–		SubLVDS Data Link (active during normal operation when LS0 = high and LS1 = low, or LS0 = low and LS1=high; high impedance if LS0 = LS1 = low)
D2+, D2–		SubLVDS Data Link (active during normal operation when LS0 = low and LS1 = high, high-impedance when LS1 = low)
CLK+, CLK–		SubLVDS output Clock; clock polarity is fixed
R0–R7	CMOS IN	Red Pixel Data (8); pin assignment depends on SWAP pin setting
G0–G7		Green Pixel Data (8); pin assignment depends on SWAP pin setting
B0–B7		Blue Pixel Data (8); pin assignment depends on SWAP pin setting
HS		Horizontal Sync
VS		Vertical Sync
DE		Data Enable
PCLK		Input Pixel Clock; rising or falling clock polarity is selected by control input CPOL
LS0, LS1		Link Select (Determines active SubLVDS Data Links and PLL Range) See Table 2
TXEN		Disables the CMOS Drivers and Turns Off the PLL, putting device in shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (Shutdown) Note: The TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 µs to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 µs to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0
CPOL	CMOS In	Input Clock Polarity Selection 0 – rising edge clocking 1 – falling edge clocking
SWAP	CMOS In	Bus Swap swaps the bus pins to allow device placement on top or bottom of pcb. See pinout drawing for pin assignments. 0 – data input from B0...R7 1 – data input from R7...B0
V_{DD}	Power Supply(1)	Supply Voltage
GND		Supply Ground
V_{DDLVDS}		SubLVDS I/O supply Voltage
GND_{LVDS}		SubLVDS Ground
V_{DDPLLA}		PLL analog supply Voltage
GND_{PLLA}		PLL analog GND
V_{DDPLLD}		PLL digital supply Voltage
GND_{PLLD}		PLL digital GND

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

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FUNCTIONAL DESCRIPTION

Serialization Modes

The SN65LVDS301 transmitter has three modes of operation controlled by link-select pins LS0 and LS1. Table 2 shows the serializer modes of operation.

Table 2. Logic Table: Link Select Operating Modes

LS1	LS0		Mode of Operation	Data Links Status
0	0	1ChM	1-channel mode (30-bit serialization rate)	D0 active; D1, D2 high-impedance
0	1	2ChM	2-channel mode (15-bit serialization rate)	D0, D1 active; D2 high-impedance
1	0	3ChM	3-channel mode (10-bit serialization rate)	D0, D1, D2 active
1	1		Reserved	Reserved

1-Channel Mode

While LS0 and LS1 are held low, the SN65LVDS301 transmits payload data over a single SubLVDS data pair, D0. The PLL locks to PCLK and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to serialize (shift out) the data payload on D0. Two reserved bits and the parity bit are added to the data frame. Figure 3 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and presented on the SubLVDS CLK output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats (e.g. QVGA to HVGA) that do not require the full bandwidth capabilities of the SN65LVDS301.

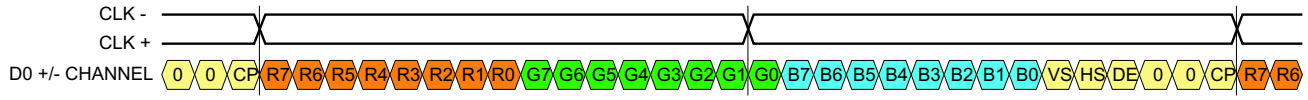

Figure 3. Data and Clock Output in 1-Channel Mode (LS0 and LS1 = low).

2-Channel Mode

While LS0 is held high and LS1 is held low, the SN65LVDS301 transmits payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to PCLK and internally multiplies it by a factor of 15. The internal high-speed clock is used to serialize the data payload on D0, and D1. Two reserved bits and the parity bit are added to the data frame. Figure 4 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split into the two output channels. The internal high-speed clock is divided by 15 to recreate the pixel clock, and presented on SubLVDS CLK. The PLL can lock to a clock that is in the range of 8 MHz through 30 MHz in this mode. Typical applications for using the 2-channel mode are HVGA and VGA displays.

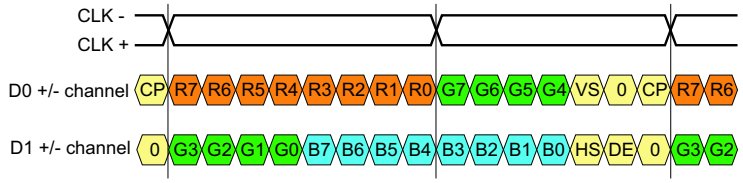

Figure 4. Data and Clock Output in 2-Channel Mode (LS0 = high; LS1 = low).

3-Channel Mode

While LS0 is held low and LS1 is held high, the SN65LVDS301 transmits payload data over three SubLVDS data pairs D0, D1, and D2. The PLL locks to PCLK, and internally multiplies it by 10. The internal high-speed clock is used to serialize the data payload on D0, D1, and D2. Two reserved bits and the parity bit are added to the data frame. Figure 5 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split over the three output channels. The internal high speed clock is divided back down by a factor of 10 to recreate the pixel clock and presented on SubLVDS CLK output. While in this mode, the PLL can lock to a clock in the range of 20 MHz through 65 MHz. Application in 3-channel mode support very large display resolutions such as VGA or XGA.

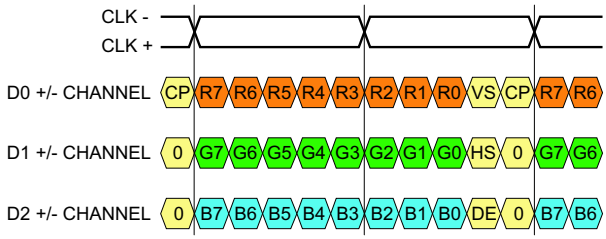

Figure 5. Data and Clock Output in 3-Channel Mode (LS0 = low; LS1 = high).

Powerdown Modes

The SN65LVDS301 Transmitter has two powerdown modes to facilitate efficient power management.

Shutdown Mode

The SN65LVDS301 enters Shutdown mode when the TXEN pin is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high-impedance. Current consumption in Shutdown mode is nearly zero.

Standby Mode

The SN65LVDS301 enters the Standby mode if TXEN is high and the PCLK input signal frequency is less than 500kHz. All circuitry except the PCLK input monitor is shut down, and all outputs enter high-impedance mode. The current consumption in Standby mode is very low. When the PCLK input signal is completely stopped, the I_{DD} current consumption is less than 10 µA. The PCLK input must not be left floating.

NOTE:

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. To prevent large leakage current, a CMOS gate must be kept at a valid logic level, either V_{IH} or V_{IL}. This can be achieved by applying an external voltage of V_{IH} or V_{IL} to all LVDS301 inputs.

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Active Modes

When TXEN is high and the PCLK input clock signal is faster than 3MHz, the SN65LVDS301 enters Active mode. Current consumption in Active mode depends on operating frequency and the number of data transitions in the data payload.

Acquire Mode (PLL approaches lock)

The PLL is enabled and attempts to lock to the input Clock. All outputs remain in high-impedance mode. When the PLL monitor detects stable PLL operation, the device switches from Acquire to Transmit mode. For proper device operation, the pixel clock frequency must fall within the valid fPCLK range specified under recommended operating conditions. If the pixel clock frequency is larger than 3MHz but smaller than f_{PCLK}(min), the SN65LVDS301 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

Transmit Mode

After the PLL achieves lock, the device enters the normal transmit mode. The CLK pin outputs a copy of PCLK. Based on the selected mode of operation, the D1, D2, and D3 outputs carry the serialized data. In 1-channel mode, outputs D2 and D3 remain high-impedance. In the 2-channel mode, output D3 remains high-impedance.

Parity Bit Generation

The SN65LVDS301 transmitter calculates the parity of the transmit data word and sets the parity bit accordingly. The parity bit covers the 27 bit data payload consisting of 24 bits of pixel data plus VS, HS and DE. The two reserved bits are not included in the parity generation. ODD Parity bit signaling is used. The transmitter sets the Parity bit if the sum of the 27 data bits result in an even number of ones. The Parity bit is cleared otherwise. This allows the receiver to verify Parity and detect single bit errors.

Status Detect and Operating Modes Flow diagram

The SN65LVDS301 switches between the power saving and active modes in the following way:

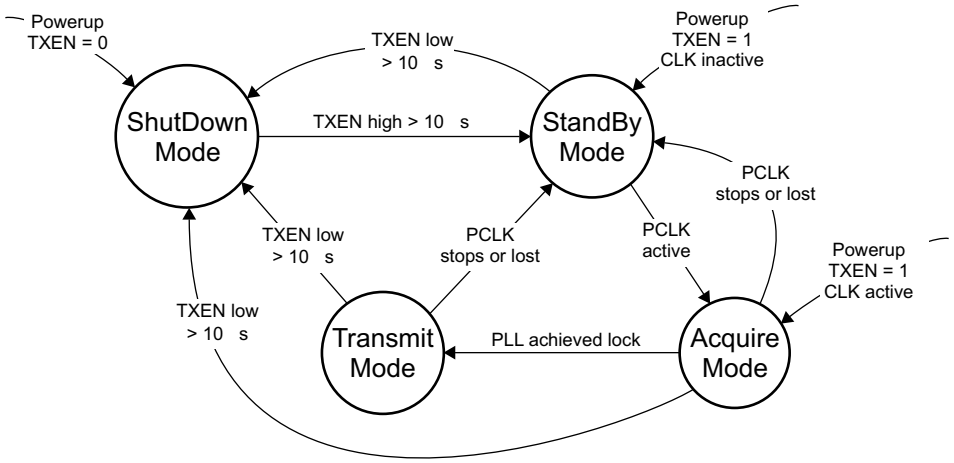

Figure 6. Status Detect and Operating Modes Flow Diagram

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Table 3. Status Detect and Operating Modes Descriptions

Mode	Characteristics	Conditions
Shutdown Mode	Least amount of power consumption(1) (most circuitry turned off); All outputs are high-impedance	TXEN is low(1)(2)
Standby Mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); All outputs are high-impedance	TXEN is high; PCLK input signal is missing or inactive(2)
Acquire Mode	PLL tries to achieve lock; All outputs are high-impedance	TXEN is high; PCLK input monitor detected input activity
Transmit Mode	Data transfer (normal operation); Transmitter serializes data and transmits data on serial output; unused outputs remain high-impedance	TXEN is high and PLL is locked to incoming clock

(1) In Shutdown Mode, all SN65LVDS301 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.
(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All inputs must be tied to a valid logic level V_{IL} or V_{IH} during Shutdown or Standby Mode.

Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Drive TXEN high to enable transmitter	1. TXEN high > 10 µs 2. Transmitter enters standby mode a. All outputs are high-impedance b. Transmitter turns on clock input monitor
Standby → Acquire	Transmitter activity detected	1. PCLK input monitor detects clock input activity; 2. Outputs remain high-impedance; 3. PLL circuit is enabled
Acquire → Transmit	Link is ready to transfer data	1. PLL is active and approaches lock 2. PLL achieved lock within 2 ms 3. Parallel Data input latches into shift register 4. CLK output turns on 5. selected Data outputs turn on and send out first serial data bit
Transmit → Standby	Request Transmitter to enter Standby mode by stopping PCLK	1. PCLK Input monitor detects missing PCLK 2. Transmitter indicates standby, putting all outputs into high-impedance; 3. PLL shuts down; 4. PCLK activity input monitor remains active
Transmit/Standby → Shutdown	Turn off Transmitter	1. TXEN pulled low for longer than 10us 2. Transmitter indicates standby, putting output CLK+ and CLK– into high-impedance state; 3. Transmitter puts all other outputs into high-impedance state 4. Most IC circuitry is shut down for least power consumption

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ORDERING INFORMATION

PART NUMBER	PACKAGE	SHIPPING METHOD
SN65LVDS301ZQE	ZQE	Tray
SN65LVDS301ZQER		Reel

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, V_{DD}(2), V_{DDPLLA}, V_{DDPLLD}, V_{DDLVDS}		-0.3 to 2.175	V
Voltage range at any output terminal		-0.5 to 2.175	V
Voltage range at any input terminal		-0.5 to 2.175	V
Electrostatic discharge	Human Body Model(3) (all Pins)	±3	kV
	Charged-Device Mode(4)l (all Pins)	±500	V
	Machine Model(5) (all pins)	±200	
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
ZQE	Low-K(2)	592 mW	7.407 mW/°C	148 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-2.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		VALUE	UNIT
P_D Device Power Dissipation	Typical	V_{DDx} = 1.8 V, T_A = 25°C, 3-channel mode	PCLK at 4 MHz	14.4	mW
			PCLK at 65 MHz	44.5	
	Maximum	V_{DDx} = 1.95 V, T_A = –40°C	PCLK at 4 MHz	22.3	mW
			PCLK=65 MHz	71.8	

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RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDS}	Supply voltages		1.65	1.8	1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude 50 MHz (all supplies)	Test set-up see Figure 12				mV
		f(PCLK) ≤ 50MHz; f(noise) = 1Hz to 2 GHz			100	
		f(PCLK) > 50MHz; f(noise) = 1Hz to 1MHz			100	
		f(PCLK) > 50 MHz; f(noise) > 1MHz			40	
f_{PCLK}	Pixel clock frequency	1-Channel transmit mode, see Figure 3	4		15	MHz
		2-Channel transmit mode, see Figure 4	8		30	
		3-Channel transmit mode, see Figure 5	20		65	
		Frequency threshold Standby mode to active mode(2), see Figure 16	0.5		3	
$t_H \times f_{PCLK}$	PCLK input duty cycle		0.33		0.67	
T_A	Operating free-air temperature		–40		85	°C
$t_{jit(per)PCLK}$	PCLK RMS period jitter(3)	Measured on PCLK input			5	ps-rms
$t_{jit(TJ)PCLK}$	PCLK total jitter				$0.05/f_{PCLK}$	s
$t_{jit(CC)PCLK}$	PCLK peak cycle-to-cycle jitter(4)				$0.02/f_{PCLK}$	s
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage				$0.3 \times V_{DD}$	V
t_{DS}	Data set up time prior to PCLK transition	f (PCLK) = 65 MHz; see Figure 8	2.0			ns
t_{DH}	Data hold time after PCLK transition		2.0			ns

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS301into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS301. Input frequencies beyond 3 MHz activate the SN65LVDS301.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles; over a random sample of 1,000 adjacent cycle pairs.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditons (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_{DD}	1ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, alternating 1010 serial bit pattern	f_{PCLK} = 4 MHz		9.0	11.4	mA
			f_{PCLK} = 6 MHz		10.6	12.6	
			f_{PCLK} = 15 MHz		16	18.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, typical power test pattern (see Table 5)	f_{PCLK} = 4 MHz		8.0		mA
			f_{PCLK} = 6 MHz		8.9		
			f_{PCLK} = 15 MHz		14.0		
	2ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, alternating 1010 serial bit pattern;	f_{PCLK} = 8 MHz		13.7	15.9	mA
			f_{PCLK} = 22 MHz		18.4	22.0	
			f_{PCLK} = 30 MHz		21.4	25.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, typical power test pattern (see Table 6)	f_{PCLK} = 8 MHz		11.5		mA
			f_{PCLK} = 22 MHz		16.0		
			f_{PCLK} = 30 MHz		19.1		
	3ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, alternating 1010 serial bit pattern	f_{PCLK} = 20 MHz		20.0	22.5	mA
			f_{PCLK} = 65 MHz		29.1	36.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at GND, typical power test pattern (see Table 7)	f_{PCLK} = 20 MHz		15.9		mA
			f_{PCLK} = 65 MHz		24.7		
	Standby Mode		V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, all inputs held static high or static low		0.61	10	µA
	Shutdown Mode				0.55	10	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
subLVDS output (D0+, D0–, D1+, D1–, D2+, D1–, CLK+, and CLK–)						
$V_{OC(SS)M}$	Steady-state common-mode output voltage	Output load see Figure 10	0.8	0.9	1.0	V
$V_{OCM(SS)}$	Change in steady-state common-mode output voltage		–10		10	mV
$V_{OCM(PP)}$	Peak-to-peak common mode output voltage				75	mV
$\|V_{OD}\|$	Differential output voltage magnitude $\|V_{Dx+} - V_{Dx-}\|$, $\|V_{CLK+} - V_{CLK-}\|$		100	150	200	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states		–10		10	mV
$Z_{OD(CLK)}$	Differential small-signal output impedance	TXEN at V_{DD}		210		Ω
I_{OSD}	Differential short-circuit output current	V_{OD} = 0 V, f_{PCLK} = 28 MHz			10	mA
I_{OS}	Short circuit output current(2)	V_O = 0 V or V_{DD}		5		
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{DD}(max), TXEN at GND	–3		3	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) All SN65LVDS301 outputs tolerate shorts to GND or V_{DD} without permanent device damage.

PRODUCT PREVIEW

INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
I_{IH}	High-level input current	$V_{IN} = 0.7 \times V_{DD}$	–200		200	nA
I_{IL}	Low-level input current	$V_{IN} = 0.3 \times V_{DD}$	–200		200	
C_{IN}	Input capacitance			1.5		pF

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$t_{R/F}$	20%-to-80% differential output signal rise time	See Figure 9 and Figure 10		250		500	ps
t_f	20%-to-80% differential output signal fall time	see figure 7-1 and figure 7-2;		250		500	ps
f_{BW}	PLL bandwidth (3dB cutoff frequency)	Tested from PCLK input to CLK output, See Figure 7(2)	f_{PCLK} = 22 MHz			$0.082 \times f_{PCLK}$	MHz
			f_{PCLK} = 65 MHz			$0.07 \times f_{PCLK}$	MHz
$t_{pd(L)}$	Propagation delay time, input to serial output (data latency Figure 8)	TXEN at V_{DD}, $V_{IH}=V_{DD}$, V_{IL}=GND, R_L=100 Ω	1-channel mode	$0.8/f_{PCLK}$	$1/f_{PCLK}$	$1.2/f_{PCLK}$	s
			2-channel mode	$1.0/f_{PCLK}$	$1.21/f_{PCLK}$	$1.5/f_{PCLK}$	s
			3-channel mode	$1.1/f_{PCLK}$	$1.31/f_{PCLK}$	$1.6/f_{PCLK}$	s
$t_H \times f_{CLK0}$	Output CLK duty cycle		1-channel and 3-channel mode	0.45	0.50	0.55	
			2-channel mode	0.49	0.53	0.58	
t_{GS}	TXEN Glitch suppression pulse width(3)	$V_{IH}=V_{DD}$, V_{IL}=GND, TXEN toggles between V_{IL} and V_{IH}, see Figure 14 and Figure 15		3.8		10	µs
t_{pwrup}	Enable time from power down (↑TXEN)	Time from TXEN pulled high to CLK and Dx outputs enabled and transmit valid data; see Figure 15			0.24	2	ms
t_{pwrdn}	Disable time from active mode (↓TXEN)	TXEN is pulled low during transmit mode; time measurement until output is disabled and PLL is Shutdown; see Figure 15			0.5	11	µs
t_{wakup}	Enable time from Standby (↕PCLK)	TXEN at V_{DD}; device in standby; time measurement from PCLK starts switching to CLK and Dx outputs enabled and transmit valid data; see Figure 15			0.23	2	ms
t_{sleep}	Disable time from standby (PCLK stopping)	TXEN at V_{DD}; device is transmitting; time measurement from PCLK input signal stops until CLK + Dx outputs are disabled and PLL is disabled; see Figure 15			0.4	100	µs

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) The Maximum Limit is based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).
(3) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

PRODUCT PREVIEW

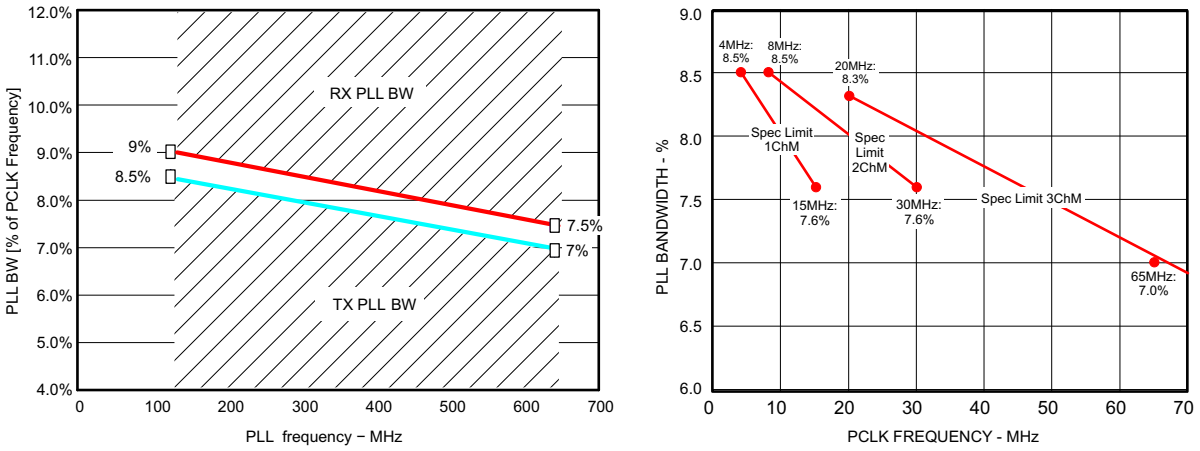


Figure 7. LVDS301 PLL Bandwidth (also showing the LVDS302 PLL bandwidth)

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PPOSX}	Output Pulse Position, serial data to ↑CLK; see (1)(2) and Figure 13	1ChM: x=0..29, f_{PCLK}=15 MHz; TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in Table 10 (3)	$\frac{x}{30\ f_{PCLK}}$ 330 ps		$\frac{x}{30\ f_{PCLK}}$ 330 ps	ps
		1ChM: x=0..29, f_{PCLK}=4 MHz to 15 MHz (4)	$\frac{x - 0.1845}{30\ f_{PCLK}}$		$\frac{x\ \ 0.1845}{30\ f_{PCLK}}$	
		2ChM: x = 0..14, f_{PCLK} = 30 MHz TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in Table 11 (3)	$\frac{x}{15\ f_{PCLK}}$ 330 ps		$\frac{x}{15\ f_{PCLK}}$ 330 ps	
		2ChM: x=0..14, f_{PCLK}= 8 MHz to 30 MHz (4)	$\frac{x - 0.1845}{15\ f_{PCLK}}$		$\frac{x + 0.1845}{15\ f_{PCLK}}$	
		3ChM: x=0..9, f_{PCLK}=65 MHz, TXEN at V_{DD}, V_{IH}=V_{DD}, VIL=GND, R_L=100 Ω, test pattern as in Table 12 (3)	$\frac{x}{10\ f_{PCLK}}$ 210 ps		$\frac{x}{10\ f_{PCLK}}$ 210 ps	
		3ChM: x=0..9, f_{PCLK}=20 MHz to 65 MHz (4)	$\frac{x\ \ 0.153}{10\ f_{PCLK}}$		$\frac{x\ \ 0.153}{10\ f_{PCLK}}$	

(1) This number also includes the high-frequency random and deterministic PLL clock jitter that is not traceable by the SN65LVDS302 receiver PLL; tPPosx represents the total timing uncertainty of the transmitter necessary to calculate the jitter budget when combined with the SN65LVDS302 receiver;

(2) The pulse position min/max variation is given with a bit error rate target of 10^{-12}; The measurement estimates the random jitter contribution to the total jitter contribution by multiplying the random RMS jitter by the factor 14; Measurements of the total jitter are taken over a sample amount of > 10^{-12} samples.

(3) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

(4) These Minimum and Maximum Limits are simulated only.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

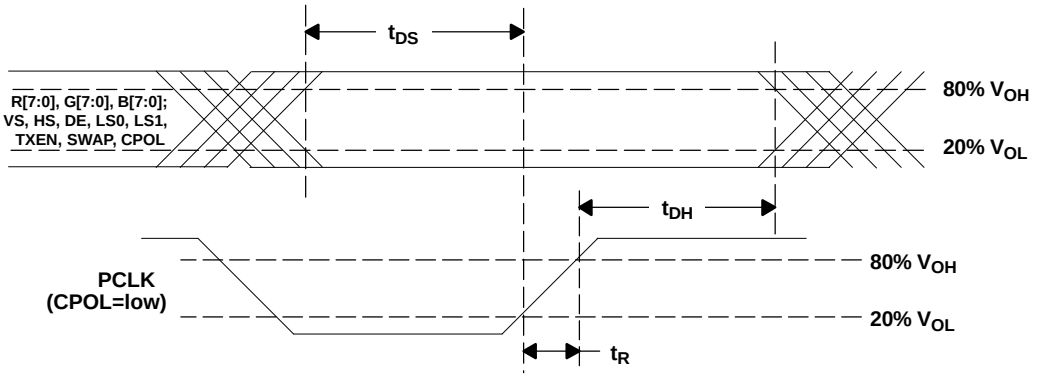


Figure 8. Setup/Hold Time

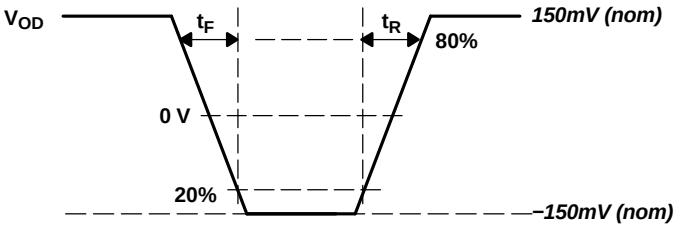
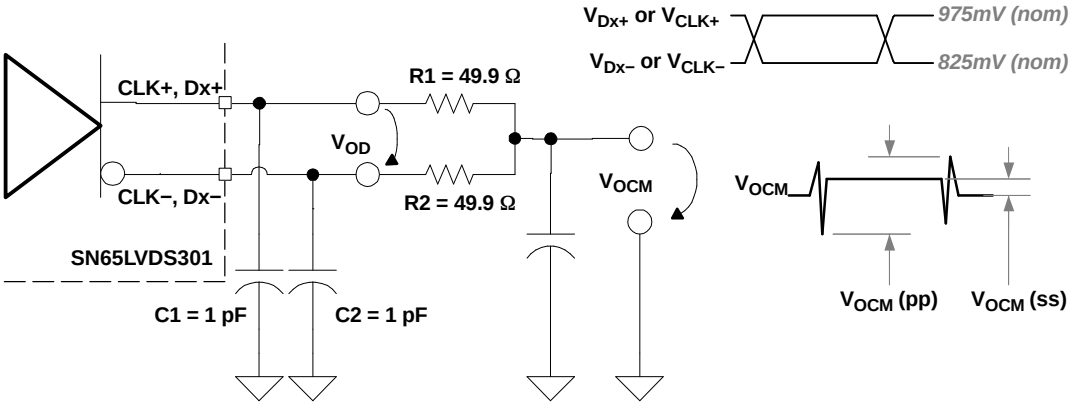


Figure 9. Rise and Fall Time Definitions



NOTES:

A. 20 MHz output test pattern on all differental outputs (CLK, D1, D3, and D2):
this is achieved by: 1. Divice is sey to 3-channel-mode;
2. f_{PCLK} = 20 MHz
3. Inputs R[7:3] = B[7:3] connected to V_{DD}, all other data inputs set to GND.

B. C1, C2 and C3 includes instrumentation and fixture capacitance; tolerance ± 20%; C, R1 and R2 tolerance ± 1%.

C. The measurement of V_{OCM} (pp) and V_{OC}(ss) are taken with test equipment bandwidth >1 GHz.

Figure 10. Driver Output Voltage Test Circuit and Definitions

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION (continued)

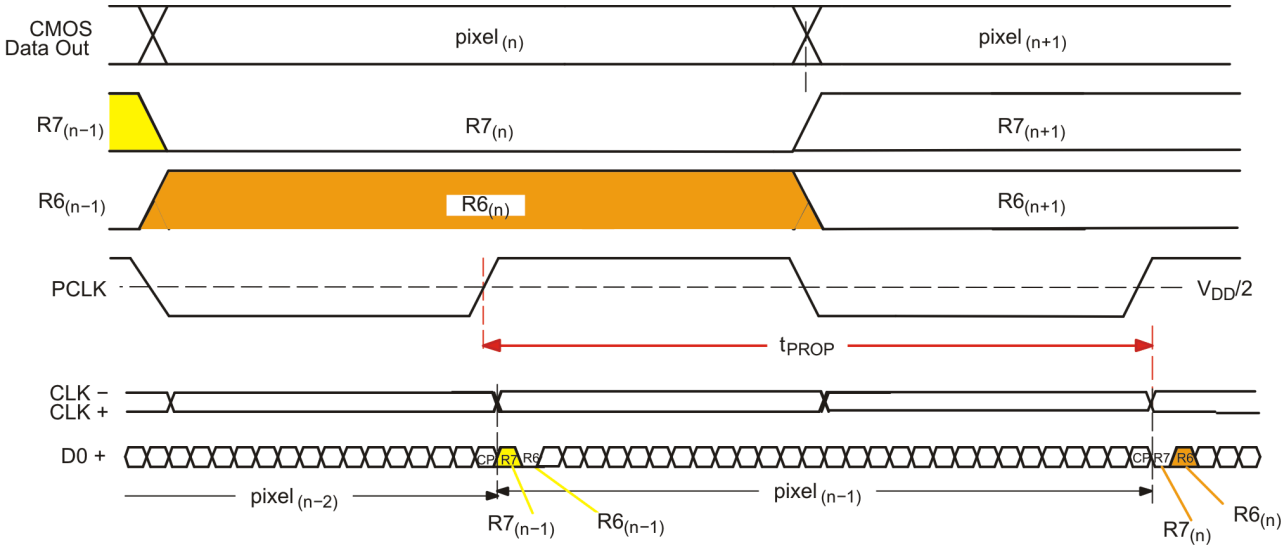


Figure 11. $t_{pd(L)}$ Propagation Delay Input to Output (LS0=LS1=0; CPOL=1)

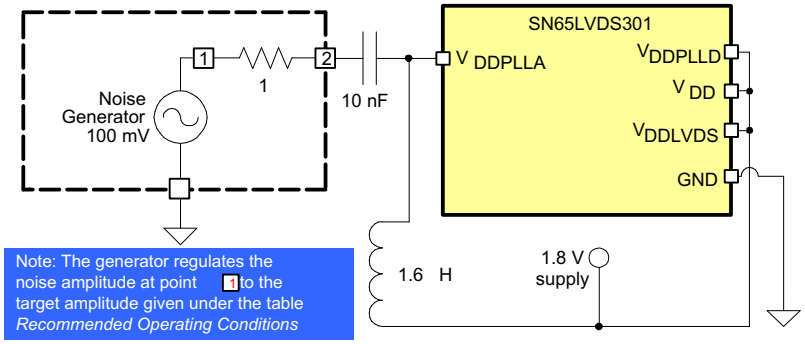


Figure 12. Power Supply Noise Test Set-Up

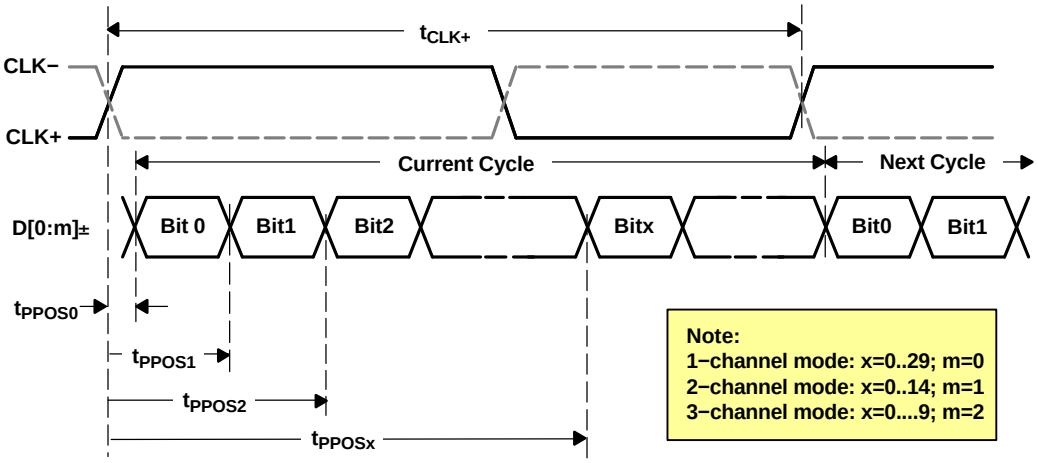


Figure 13. $t_{SK(0)}$ SubLVDS Output Pulse Position Measurement

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION (continued)

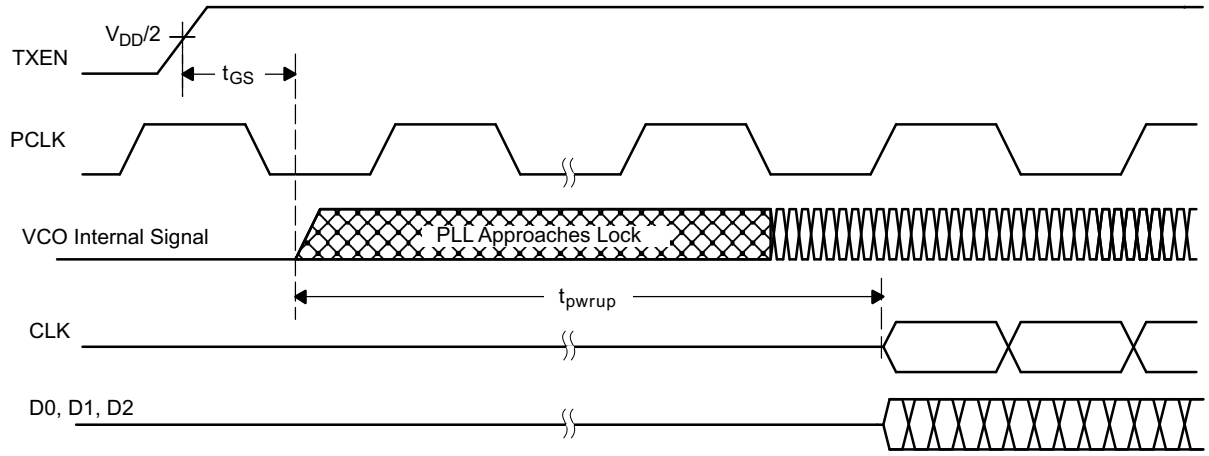


Figure 14. Transmitter Behavior While Approaching Sync

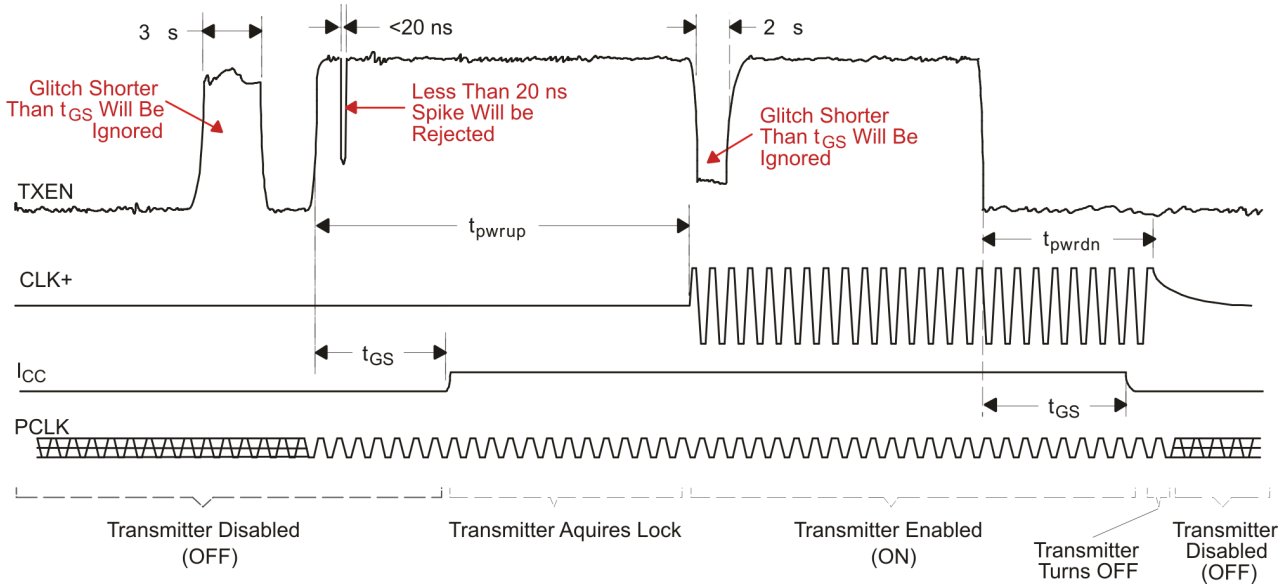


Figure 15. Transmitter Enable Glitch Suppression Time

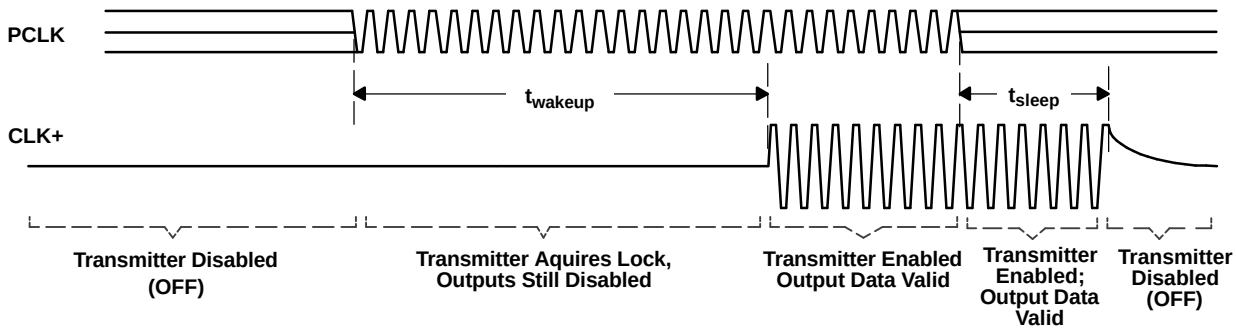


Figure 16. Standby Detection

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION (continued)

Power Consumption Tests

Table 4 shows an example test pattern word.

Table 4. Example Test Pattern Word

Word	R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

Typical IC Power Consumption Test Pattern

The typical power consumption test patterns consists of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 5. Typical IC Power Consumption Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Table 6. Typical IC Power Consumption Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x03F03F1
3	0xBFFBFF1
4	0x1D71D71
5	0x4C74C71
6	0xC45C451
7	0xA3aA3A5
8	0x5555553

Table 7. 3-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xFFFFFF1
2	0x0000001
3	0xF0F0F01
4	0xCCCCCC1
5	0xAAAAAA7

Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS301 is tested using the two different test pattern shown in table. test patterns consists of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 8. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xAAAAAA5
2	0x5555555

Table 9. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000000
2	0xFFFFFF7

Output Skew Pulse position & Jitter Performance

The following test patterns are used to measure the output skew pulse position and the jitter performance of the SN65LVDS301. The pattern stresses the interconnect particularly to test for ISI, very long run-lengths of consecutive bits, incorporates very high and low data rates, and maximizes switching noise. Each pattern is self-repeating for the duration of the test.

Table 10. Transmit Jitter Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

Table 11. Transmit Jitter Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x000FFF3
3	0x8008001
4	0x0030037
5	0xE00E001
6	0x00FF001
7	0x007E001
8	0x003C001
9	0x0018001
10	0x1C7E381
11	0x3333331
12	0x555AAA5
13	0x6DBDB61
14	0x7777771
15	0x555AAA3
16	0xAAAAAA5
17	0x5555553
18	0xAAA5555
19	0x8888881
20	0x9242491
21	0xAAA5571
22	0xCCCCCC1
23	0xE3E1C71
24	0xFFE7FF1
25	0xFFC3FF1
26	0xFF81FF1
27	0xFE00FF1
28	0x1FF1FF1
29	0xFFCFFC3
30	0x7FF7FF1
31	0xFFF0007
32	0xFFFFFF1

Table 12. Transmit Jitter Test Pattern, 3-Channel Mode(1)

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000001
3	0x0000003
4	0x0101013
5	0x0303033
6	0x0707073
7	0x1818183
8	0xE7E7E71
9	0x3535351
10	0x0202021
11	0x5454543
12	0xA5A5A51
13	0xADADAD1
14	0x5555551
15	0xA6A2AA3
16	0xA6A2AA5
17	0x5555553
18	0x5555555
19	0xAAAAAA1
20	0x5252521
21	0x5A5A5A1
22	0xABABAB1
23	0xFDFCFD1
24	0xCAAACA1
25	0x1818181
26	0xE7E7E71
27	0xF8F8F81
28	0xFCFCFC1
29	0xFEFEFE1
30	0xFFFFFF1
31	0xFFFFFF5
32	0xFFFFFF5

(1) The jitter test pattern stresses the interconnect particularly to test for ISI, very long run-lengths of consecutive bits, incorporates very high and low data rates, and maximizes switching noise. Each pattern is self-repeating for the duration of the test.

TYPICAL CHARACTERISTICS

POWERDOWN, STANDBY SUPPLY CURRENT vs TEMPERATURE

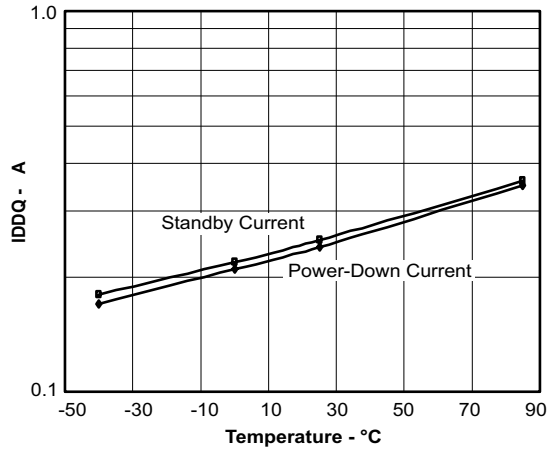


Figure 17.

SUPPLY CURRENT IDD vs TEMPERATURE

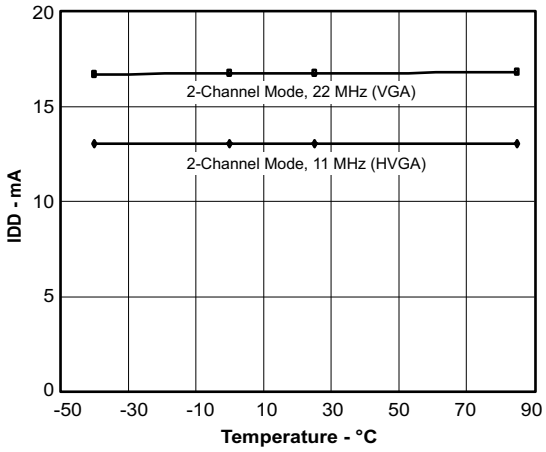


Figure 18.

SUPPLY CURRENT vs PCLK FREQUENCY

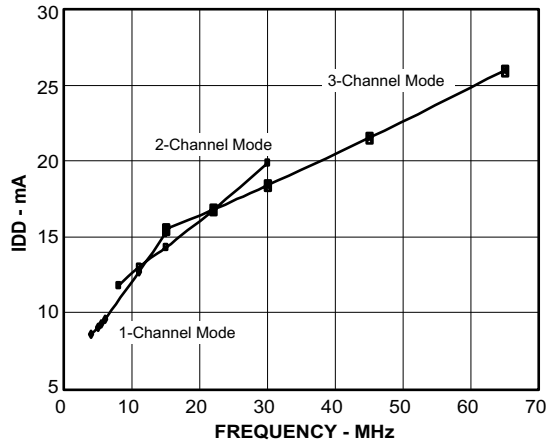


Figure 19.

DIFFERENTIAL OUTPUT SWING vs PCLK FREQUENCY

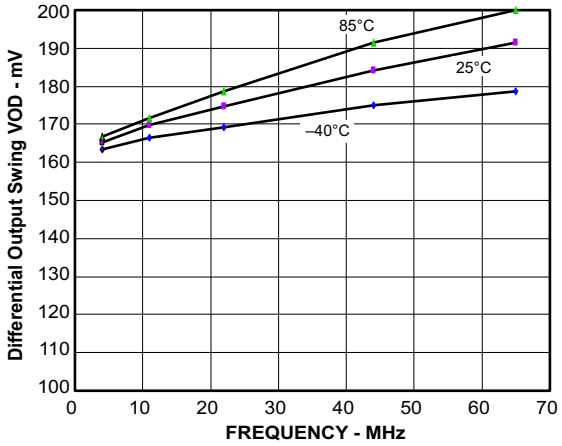


Figure 20.

PLL BANDWIDTH

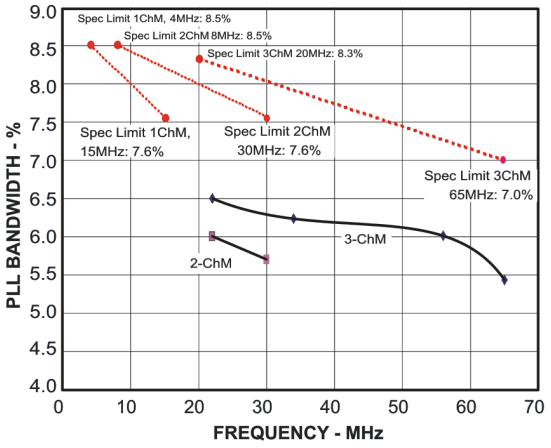


Figure 21.

CYCLE-TO-CYCLE OUTPUT JITTER vs PCLK FREQUENCY

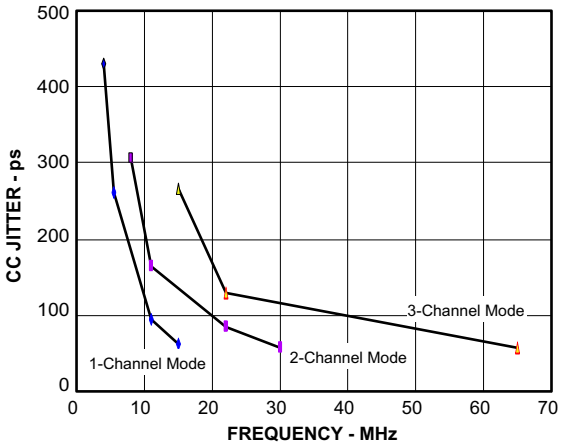


Figure 22.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

CYCLE-TO-CYCLE OUTPUT JITTER vs TEMPERATURE

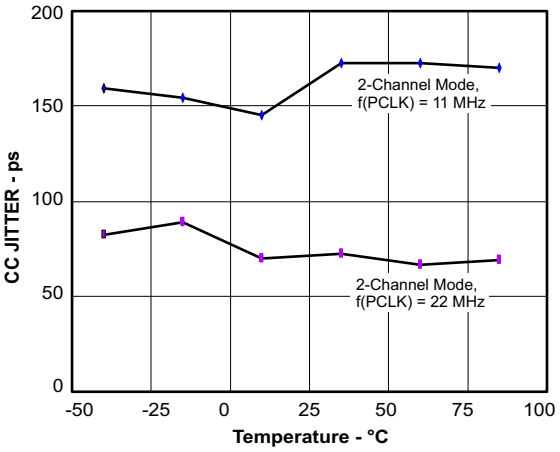


Figure 23.

OUTPUT PULSE POSITION vs TEMPERATURE

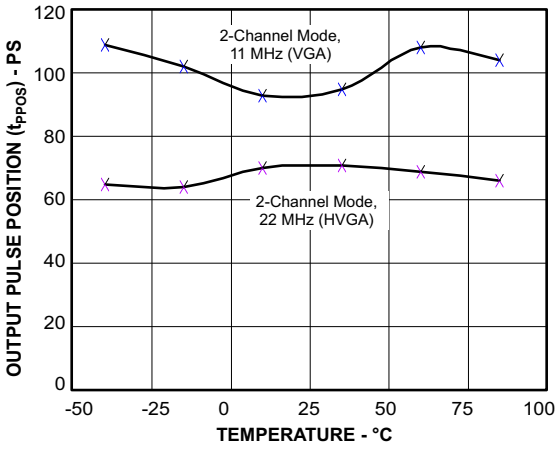


Figure 24.

DATA EYE PATTERN, 2-CHANNEL MODE

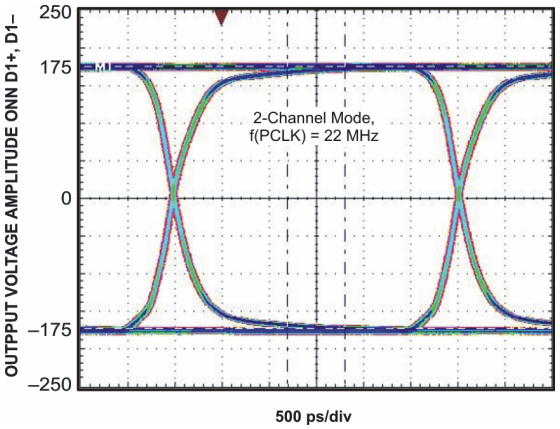


Figure 25.

DATA EYE PATTERN, 3-CHANNEL MODE

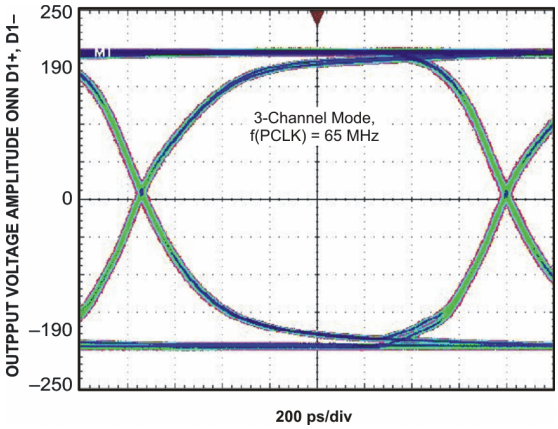


Figure 26.

PLL PHASE NOISE

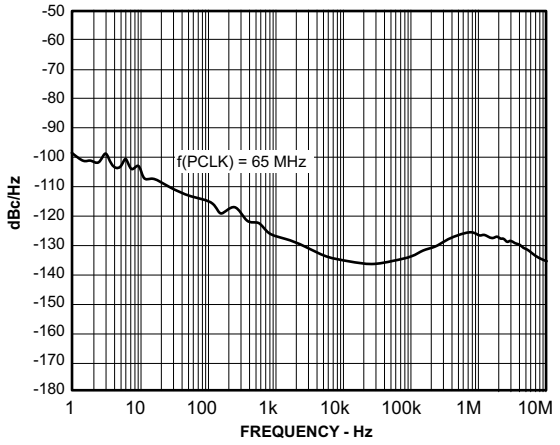


Figure 27.

OUTPUT RETURN LOSS

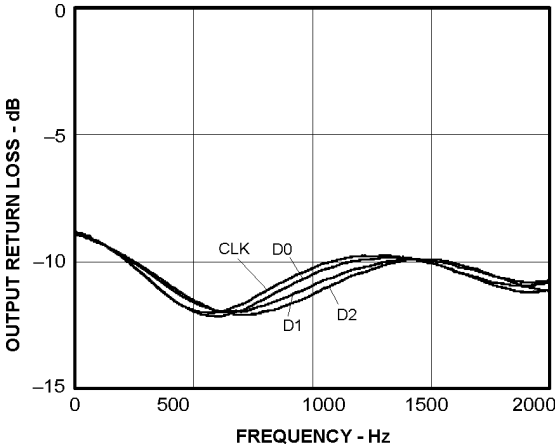


Figure 28.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

OUTPUT COMMON MODE NOISE REJECTION

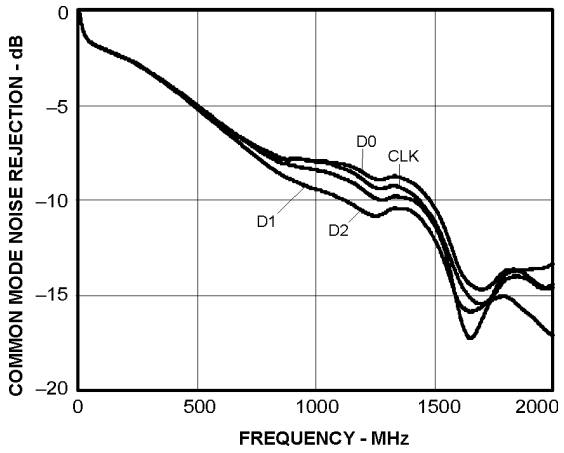


Figure 29.

CROSSTALK

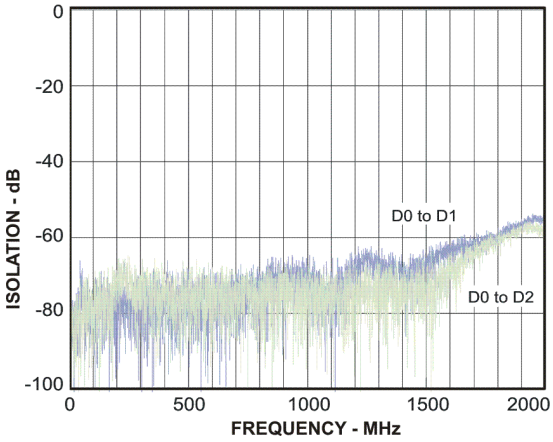


Figure 30.

GTEM SAE J1752/3 EMI TEST[A]

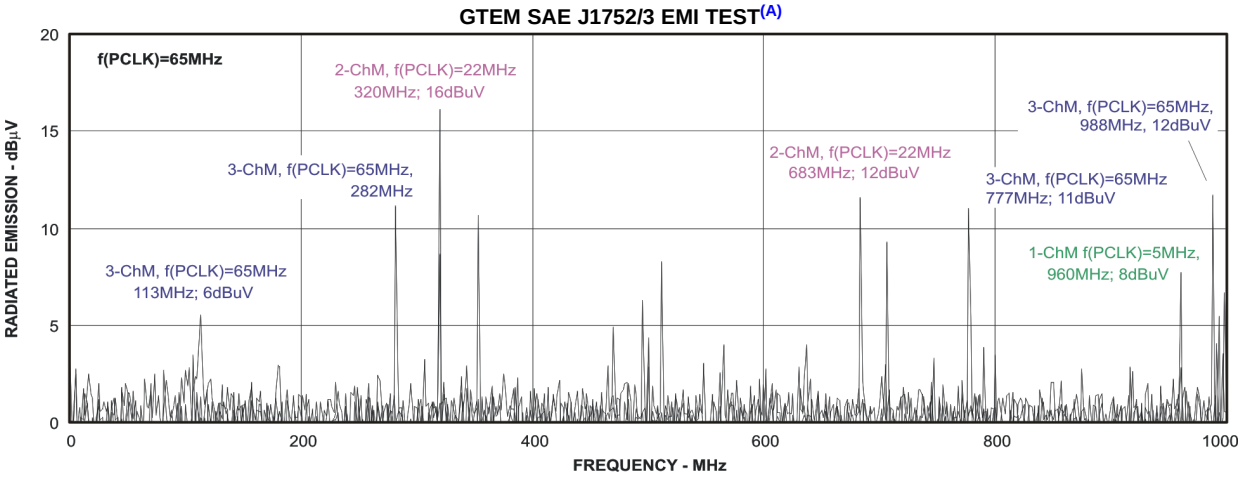


Figure 31.

A. Figure 31 shows a superimposed image of three EMI measurements with the device operating at f(PCLK)=5MHz, f(PCLK)=22MHz, and f(PCLK)=65MHz. This excellent EMI performance meets the system requirements of dense, mobile designs with a noise floor of ~2dBµV (-105dBm) and all spurs being smaller than 16dBµV (-101dBm). The test was performed in compliance with the SAE J1752/3 EMI test guidelines.

PRODUCT PREVIEW

APPLICATION INFORMATION

Decoupling Recommendation

The SN65LVDS301 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS301 often shares a power supply with the application processor. The SN65LVDS301 can operate with power supply noise as specified in *Recommend Device Operating Conditions*. To minimize the power supply noise floor, provide good decoupling near the SN65LVDS301 power pins. The use of four ceramic capacitors (2×0.01 µF and 2×0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS301. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power inputs pins must be minimized. Placing the capacitor underneath the SN65LVDS301 on the bottom of the pcb is often a good choice.

VGA Application

Figure 32 shows a possible implementation of a VGA display. The LVDS301 interfaces to the SN65LVDS302, which is the corresponding receiver device to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes ~10% blanking overhead and 60 Hz display refresh rate. The application assumes 24-bit color resolution. It is also shown, how the application processor provides a powerdown (reset) signal for both serializer and the display driver. The signal count over the FPC could be further decreased by using the standby option on the SN65LVDS302 and pulling RXEN high with a 30 kΩ resistor to V_{DD}.

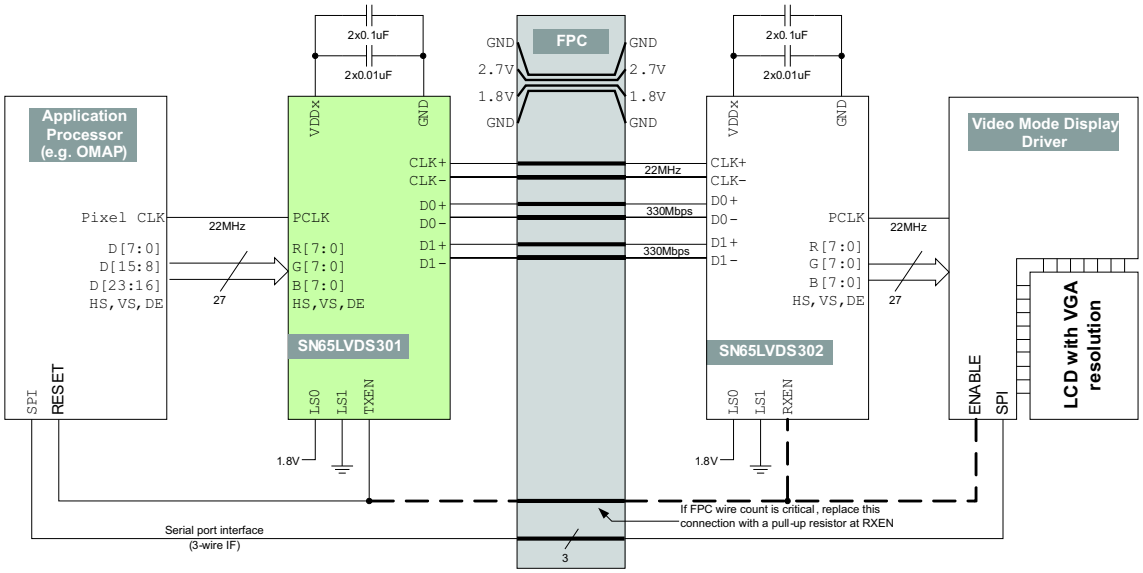


Figure 32. Typical VGA Display Application

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

Dual LCD-Display Application

The example in Figure 33 shows a possible application setup driving two video mode displays from one application processor. The data rate of 330 Mbps at a pixel clock rate of 5.5 MHz corresponds to QVGA resolution at 60 Hz refresh rate and 10% blanking overhead.

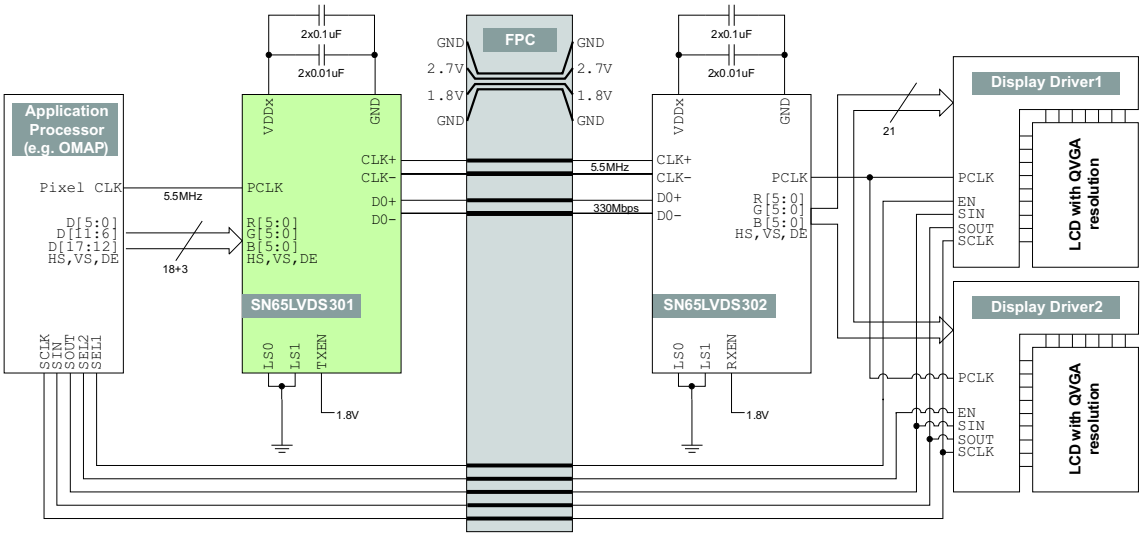


Figure 33. Example Dual-QVGA Display Application

Typical Application Frequencies

The SN65LVDS301 supports pixel clock frequencies from 4 MHz to 65 MHz over 1, 2, or 3 data lanes. Table 13 provides a few typical display resolution examples and shows the number of data lanes necessary to connect the LVDS301 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60-Hz. The actual refresh rate may differ depending on the application-processor clock implementation.

Table 13. Typical Application Data Rates & Serial Lane Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate	Pixel Clock Frequency [MHz]	Serial Data Rate Per Lane		
					1-ChM	2-ChM	3-ChM
176x220 (QCIF+)	38,720	20%	90 Hz	4.2 MHz	125 Mbps		
240x320 (QVGA)	76,800		60 Hz	5.5 MHz	166 Mbps		
640x200	128,000			9.2 MHz	276 Mbps	138 Mbps	
352x416 (CIF+)	146,432			10.5 MHz	316 Mbps	158 Mbps	
352x440	154,880			11.2 MHz	335 Mbps	167 Mbps	
320x480 (HVGA)	153,600			11.1 MHz	332 Mbps	166 Mbps	
800x250	200,000			14.4 MHz	432 Mbps	216 Mbps	
640x320	204,800			14.7 MHz	442 Mbps	221 Mbps	
640x480 (VGA)	307,200			22.1 MHz		332 Mbps	221 Mbps
1024x320	327,680			23.6 MHz		354 Mbps	236 Mbps
854x480 (WVGA)	409,920			29.5 MHz		443 Mbps	295 Mbps
800x600 (SVGA)	480,000			34.6 MHz			346 Mbps
1024x768 (XGA)	786,432			56.6 MHz			566 Mbps

PRODUCT PREVIEW

Calculation Example: HVGA Display

This example calculation shows a typical Half-VGA display with these parameters:

Display Resolution:	320 x 480
Frame Refresh Rate:	58.4 Hz
Vertical Visible Pixel:	480 lines
Vertical Front Porch:	20 lines
Vertical Sync:	5 lines
Vertical Back Porch:	3 lines
Horizontal Visible Pixel:	320 columns
Horizontal Front Porch:	10 columns
Horizontal Sync:	5 columns
Horizontal Back Porch:	3 columns

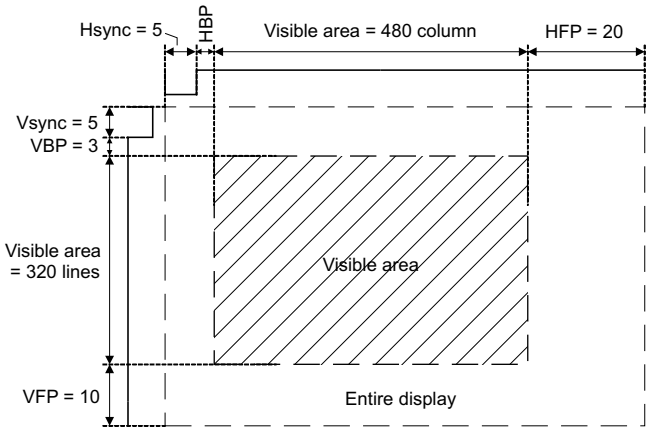


Figure 34. HVGA Display Parameters

Calculation of the total number of pixel and Blanking overhead:

Visible Area Pixel Count:	480 × 320 = 153600 pixel
Total Frame Pixel Count:	(480+20+5+3) × (320+10+5+3) = 173304 pixel
Blanking Overhead:	(173304-153600) ÷ 153600 = 12.8 %

The application requires following serial-link parameters:

Pixel Clk Frequency:	173304 × 58.4 Hz = 10.1 MHz
Serial Data Rate:	1-channel mode: 10.4 MHz × 30 bit/channel = 304 Mbps
	2-channel mode: 10.4 MHz × 15 bit/channel = 152 Mbps

PRODUCT PREVIEW

PACKAGING INFORMATION

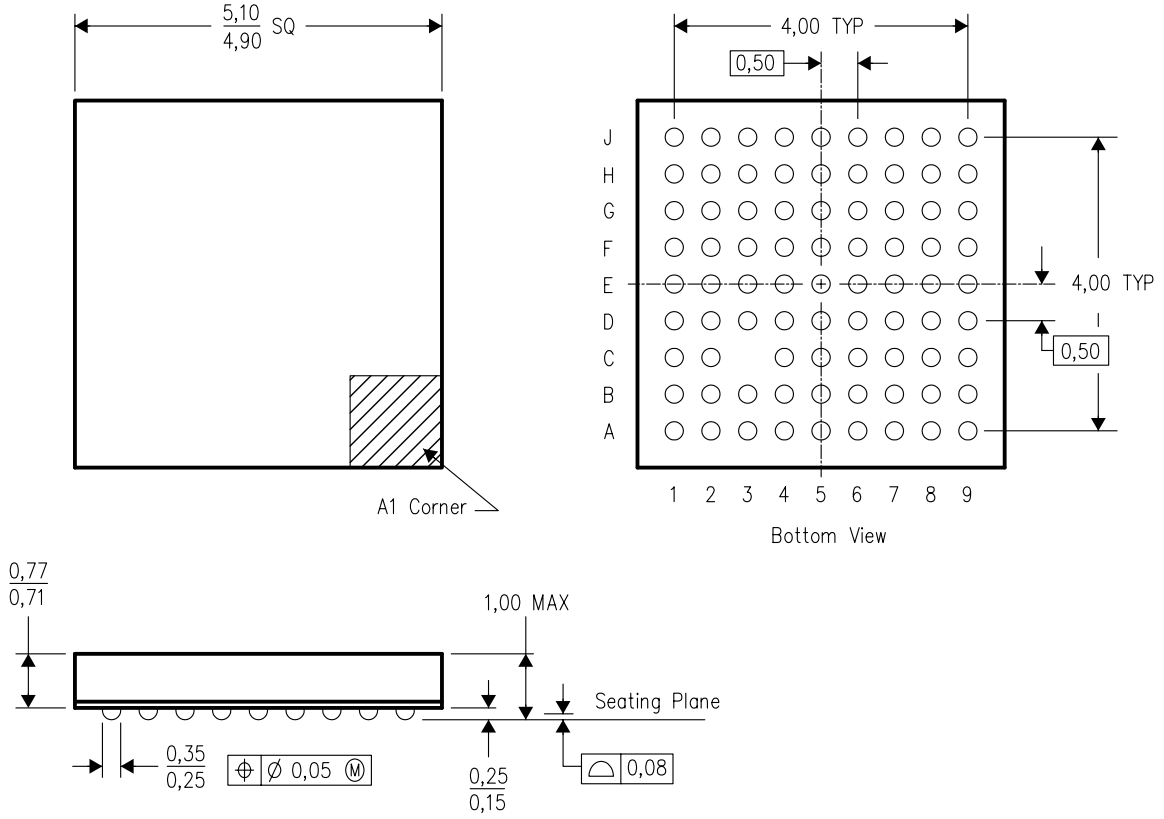
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS301ZQE	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80	184	TBD	Call TI	Call TI
SN65LVDS301ZQER	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–4/D 10/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

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