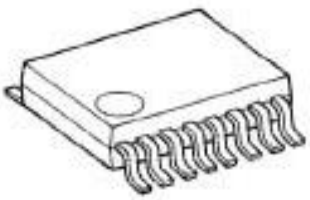
TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

T A 1 3 2 6 F N G

UHF Band RF Modulator IC for VTRs

The TA1326FNG is a UHF band RF modulator IC that features PLL-based RF carrier and audio intercarrier oscillation.

The TA1326FNG is compatible with PAL and NTSC television systems and is lower in cost than TA1243 or TA1297 Series devices.



SSOP16-P-225-0.65B

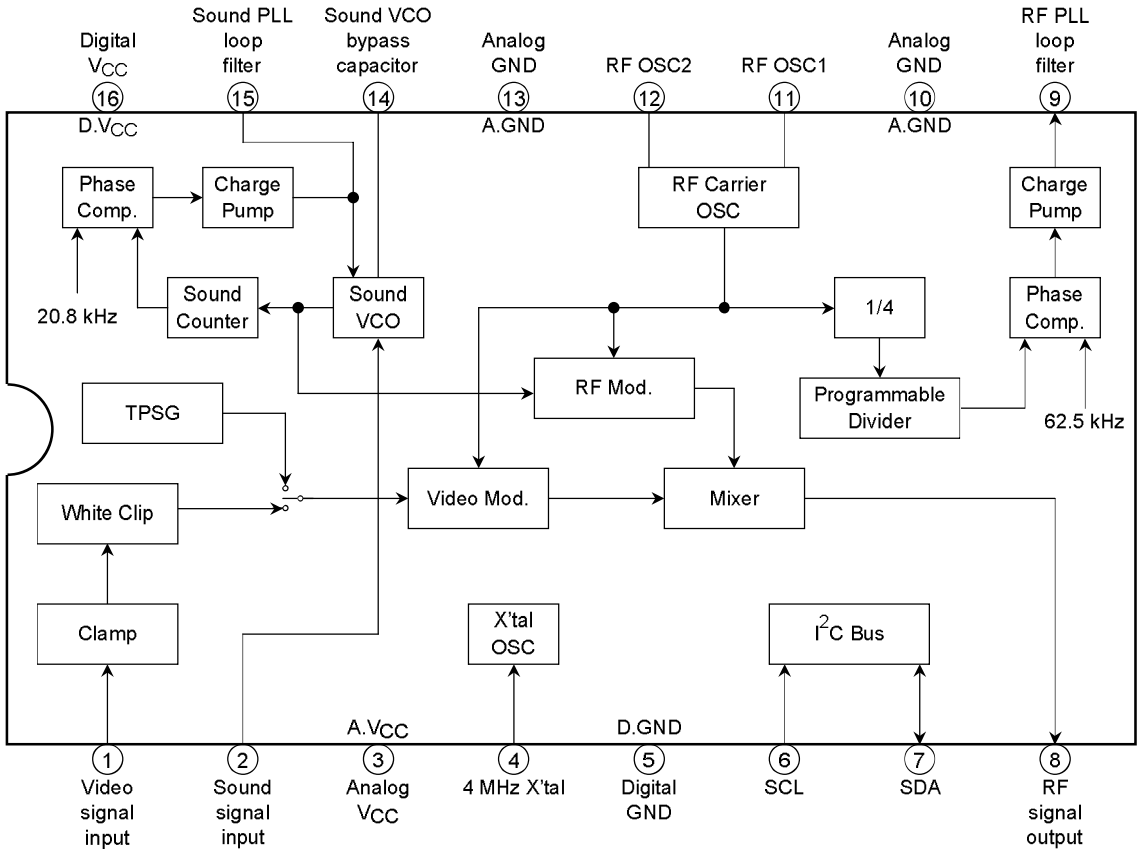
Weight: 0.07 g (typ.)

Features

- PLL-based RF oscillator for full UHF band operation (channels 21~69)
- PLL-based audio intercarrier oscillator which can support both PAL and NTSC television systems without any adjustment
  Formats supported: M/G/H/I/D
- Mode control using I^2C bus
  RF carrier frequency (10 bits, in 1-MHz steps)
  Audio intercarrier frequencies (4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz)
  P/S ratio setting (−10dB to −17dB in 1dB steps)
- Test pattern generator
- White Clip Through Mode
- Muted RF output on power-on and as required
- Terminal of Package is improved to Lead-Free.

Pins numbered 2 and 7 of this product are sensitive to electrostatic discharge. When handling this product, protect the environment to avoid electrostatic discharge.

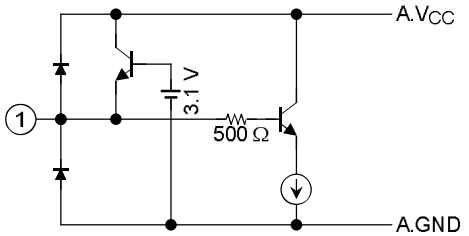
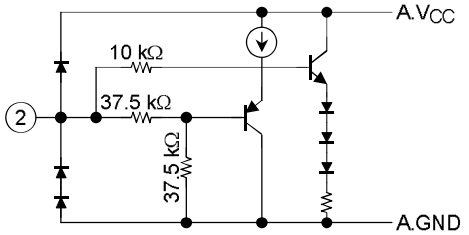
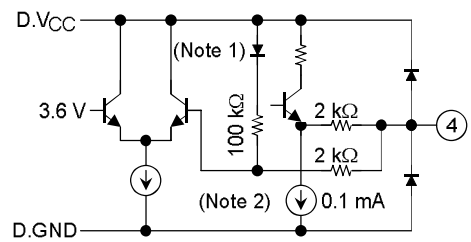
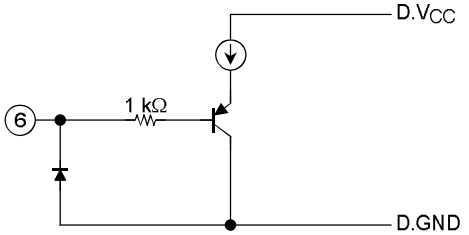
Block Diagram

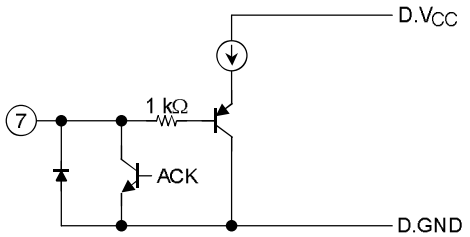
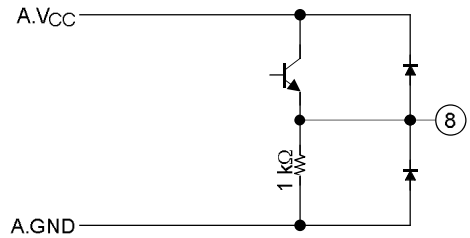
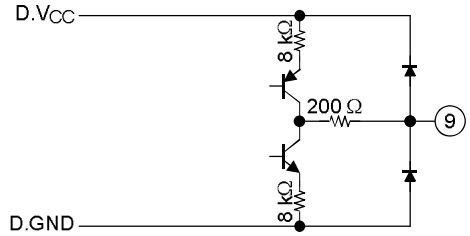
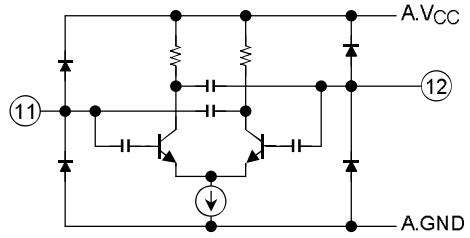
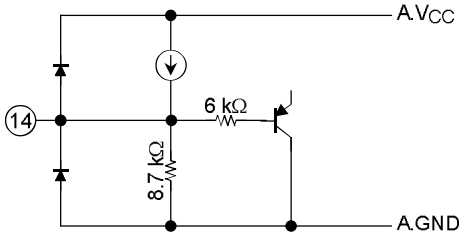


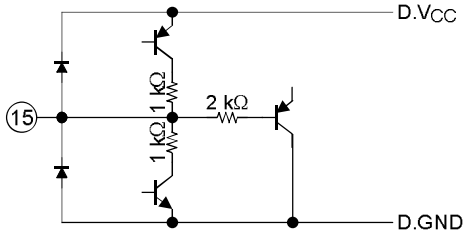
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Pin Description (V_{CC} = 5.0 V, Ta = 25°C)

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.

Pin No.	Name	DC Voltage (typ.)	AC Voltage (typ.)	Interface	Note
1	Video signal input	2.4 V (sync tip)	500 mVp-p (80% modulation)		Sync tip clamp input. It is used by AC coupling. Video modulation depth is set by level of signal input on this pin. White clip level for IC is set internally for DC, but it will change by the high frequency-factor.
2	Sound signal input	0 V (Normal Mode)	350 mVp-p (100% FM modulation)		Sound modulation depth is set by level of sound signal input on this pin. Sound pre-emphasis is applied before this pin. This pin is also used for switching test mode. Normally this pin is used at 0 V DC (used by AC coupling). H: Test Mode L (open): Normal Mode
3	Analog V_{CC}	(5 V)	—	—	Analog power supply
4	4-MHz X'tal	2.7 V (Internal Oscillation Mode) 4.3 V (External Input Mode)	—	 Note 1: Internal Oscillation Mode OFF Note 2: External Input Mode OFF	As reference signal, either 4-MHz crystal resonator can be connected to this pin for internal oscillation or external signal can be input. External Input Mode can be selected using I^2C bus or by pulling up this pin using external resistor in Internal Oscillation Mode. 3.8 V or higher : external input 3.4 V or lower : internal oscillation (in Internal Oscillation Mode)
5	Digital GND	(0 V)	—	—	Digital ground
6	SCL	L: ≤ 1.5 V H: ≥ 2.0 V	—		Pin connected to I^2C bus serial clock line. Data transfer rate conforms to Fast Mode standard.

Pin No.	Name	DC Voltage (typ.)	AC Voltage (typ.)	Interface	Note
7	SDA	L: ≤ 1.5 V H: ≥ 2.0 V	—		Pin connected to I²C bus serial data line. Data transfer rate conforms to Fast Mode standard.
8	RF signal output	3.7 V	81dBμV		RF signal output pin. Low-impedance emitter-follower output
9	RF PLL loop filter	—	—		RF oscillation frequency is compared with I²C bus RF setting frequency, and the error is outputted by Charge pump. LPF for high frequency rejection is connected to this terminal. The signal after a high frequency rejection is amplified with common-emitter amplifier, and the voltage for frequency control impressed to variable capacitor is generated. The reference frequency is 62.5 kHz.
10	Analog GND	(0 V)	—	—	Analog GND
11	RF OSC1	3.5 V	—		Differential common-emitter Colpitts oscillator. Toshiba recommends use of a Clapp oscillator as external LC resonance circuit to reduce effects of IC parasitic capacitance and others.
12	RF OSC2	3.5 V	—		
13	Analog GND	(0 V)	—	—	Analog GND
14	Sound VCO bypass capacitor	—	—		Bypass capacitor pin used by sound VCO to reduce bias noise. The smaller the external capacitance, the worse the sound S/N.

Pin No.	Name	DC Voltage (typ.)	AC Voltage (typ.)	Interface	Note
15	Sound PLL loop filter	—	—		Sound VCO oscillation frequency is compared with I²C bus intercarrier sound setting frequency, and the error is outputted by Charge pump. LPF for high frequency rejection is connected to this terminal. And the voltage for sound VCO control is generated. The reference frequency is 20.8 kHz.
16	Digital V_{CC}	(5 V)	—	—	Digital power supply

I²C-Bus Data Format

	MSB							LSB	ACK
Address Byte ADR	1	1	0	0	1	0	1	0	ACK
Control Byte 1 C1	1	(Note 3)	(Note 3)	(Note 3)	PS2	PS1	PS0	(Note 3)	ACK
Control Byte 2 C2	WO	PSA	(Note 3)	FA1	FA0	(Note 3)	(Note 3)	(Note 3)	ACK
Prog.Data Byte 1 PD1	0	TPSG	N9	N8	N7	N6	N5	N4	ACK
Prog.Data Byte 2 PD2	N3	N2	N1	N0	RM1	RM0	0	TEST	ACK

Note 3: Don't care

Bus data transmission

- ADR + C1 + C2 + PD1 + PD2
- ADR + PD1 + PD2 + C1 + C2
- ADR + C1 + C2
- ADR + PD1 + PD2

1. PS2~PS0: Picture-to-sound ratio setting

P/S Ratio	PS2	PS1	PS0
–10dB	0	0	0
–11dB	0	0	1
–12dB	0	1	0
–13dB	0	1	1
–14dB	1	0	0
–15dB	1	0	1
–16dB	1	1	0
–17dB	1	1	1

2. WO: White Clip Off Mode

1: Disables white clip function, e.g. when modulation characteristics for near-100% modulation are being checked.
0: Enables white clip function (default).

3. PSA: Power Save Mode

1: Disables power saving (default).
0: Enables power saving. The device waits for data from the bus with all blocks other than the bus decoder turned off.

In Power Save Mode, the device retains all data values as long as V_{CC} is applied. Turning V_{CC} off and on again will trigger a power-on reset, causing all data values to be initialized.

4. FA1~FA0: Audio intercarrier frequency

FA1	FA0	Audio Intercarrier Frequency	Frequency Deviation
0	0	4.5 MHz	±25 kHz
0	1	5.5 MHz	±50 kHz
1	0	6.0 MHz	±50 kHz
1	1	6.5 MHz	±50 kHz

5. TPSG: Test Pattern Signal Generator Mode

1: Enabled
0: Disabled (default)

6. N9~N0 (NA): Programmable divider data

The RF VCO oscillation frequency is calculated using the following formula.

$$f_{VCO} = 62.5\ \text{kHz} \times 16 \times N + 250\ \text{kHz}$$
$$N = 512 \times N9 + 256 \times N8 + 128 \times N7 + 64 \times N6 + 32 \times N5 + 16 \times N4 + 8 \times N3 + 4 \times N2 + 2 \times N1 + N0$$

The frequency varies in steps of 1 MHz. The +250-kHz term in the formula is hard-wired into the IC. The divider N is obtained by subtracting 250 kHz from the frequency setting.

7. Reference Signal Mode (RM1~RM0)

RM1	RM0	Reference Signal Mode
0	0	External input mode
0	1	Internal oscillation mode
1	0	Test mode
1	1	Test mode

(1) External input mode
Mode in which external 4-MHz reference signal is input. Even if a crystal resonator is connected, it cannot operate.

(2) Internal oscillation mode
Mode in which 4-MHz crystal resonator is connected and reference signal is generated.
As with Toshiba TA1297 Series devices, an external reference signal can be input by using a resistor to pulling up the crystal oscillator pin.

(3) Test mode
Usually, this mode is not used.

8. TEST: Control of test mode

1: Test mode
0: Normal mode

Power-on Reset Mode Specifications

Turning on the device triggers a power-on reset. The device operates in the following state until it receives data from the bus. In this mode, power saving is enabled and no RF signal is output.

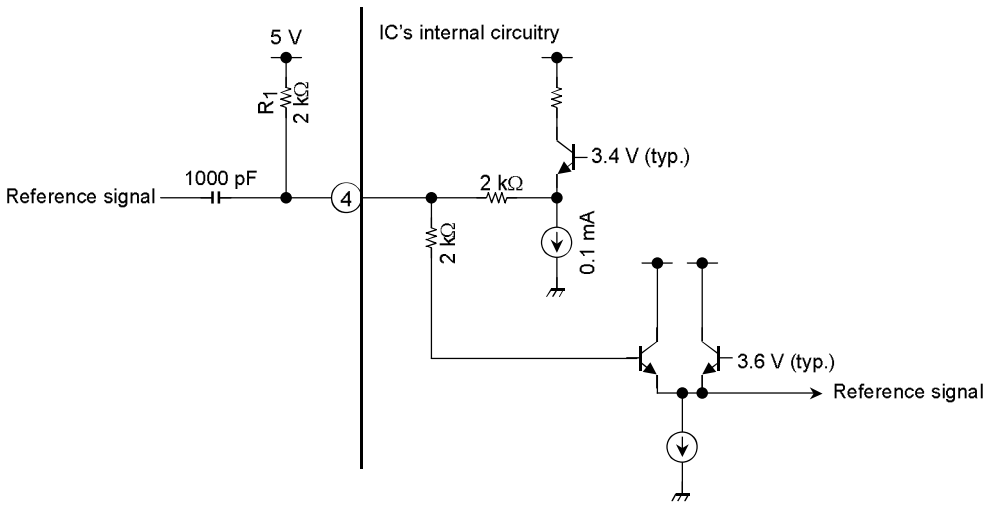
- VCO oscillation frequency: 591.25 MHz (CCIR 36ch)
- Broadcasting format: G (sound intercarrier frequency: 5.5 MHz, FM deviation: ±50 kHz)
- P/S ratio: −13dB
- White clip: ON
- Power saving: ON
- TPSG: OFF
- Reference signal: internal oscillation mode
- Test mode: Normal mode

		MSB							LSB	ACK
Address Byte	ADR	1	1	0	0	1	0	1	0	ACK
Control Byte 1	C1	1	(Note 4)	(Note 4)	(Note 4)	0	1	1	(Note 4)	ACK
Control Byte 2	C2	0	0	(Note 4)	0	1	(Note 4)	(Note 4)	(Note 4)	ACK
Prog.Data Byte 1	PD1	0	0	1	0	0	1	0	0	ACK
Prog.Data Byte 2	PD2	1	1	1	1	0	1	0	0	ACK

Note 4: Don't care

External 4MHz Input Mode (Please refer to Section 7, *Reference Signal Mode.*)

Connecting a resistor (R_1) between pin 4 and V_{CC} allows input of an external reference signal in this mode.



In this case, configure R_1 and the external circuitry so as to ensure that a voltage of at least 3.8 V is applied to pin 4 and that the sine-wave reference signal has an amplitude of at least 100 mVp-p.

Maximum Ratings (Ta = 25°C)

CAUTION

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	6	V
Power dissipation (Note 5)	P_D	810	mW
Input terminal voltage	V_{IN}	GND − 0.3~V_{CC} + 0.3	V
Operating temperature	T_{opr}	−20~75	°C
Storage temperature	T_{stg}	−55~150	°C

Note 5: Power dissipation in the IC alone. If the device is operated at Ta > 25°C, this parameter must be derated by 6.5 mW per 1°C.

Electrical Characteristics (V_{CC} = 5.0 V, Ta = 25°C, f_p = 591.25 MHz)

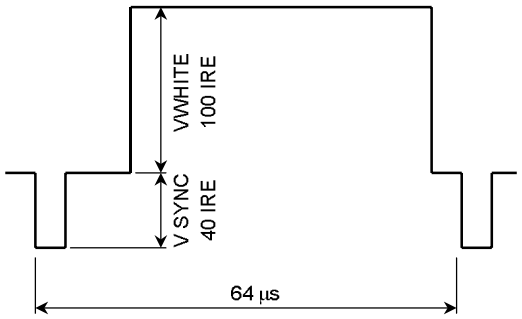
	No.	Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Entire IC	1-1	Supply voltage	Vcc	4.5	5.0	5.5	V	
	1-2-1	Supply current 1 (analog V_{CC} + digital V_{CC})	I_{CC1}	35	52	60	mA	5-V power supply
	1-2-2	Supply current 2 (analog V_{CC} + digital V_{CC})	I_{CC2}	4	7	10	mA	5-V power supply in Power Save Mode
	1-3	Operating frequency range	f_{op}	471.25	—	855.25	MHz	f_p frequency
Video Block	2-1	Video RF output level	$V_{O\ (fp)}$	78	81	84	dBμV	50-Ω termination, staircase (B/W) signal, 0.5-Vp-p input
	2-2	Video modulation depth	mp	76	80	84	%	White signal: 0.5 Vp-p input
	2-3	White clipping level	mp (max)	90	94	98	%	White signal: 1.0 Vp-p input
	2-4	Differential gain	DG	—	±2	±5	%	10-step staircase signal: 0.5-Vp-p input (chroma signal = 20 IRE), 9th step
	2-5	Differential phase	DP	—	±2	±5	°	10-step staircase signal: 0.5-Vp-p input (chroma signal = 20 IRE), 9th step
	2-6	Video S/N ratio	mp (S/N)	50	52	—	dB	0.1 MHz~5 MHz, unweighted, 50% WHITE signal input
	2-7	Video frequency response	f_p	—	±2	±3	dB	0.1 MHz~5 MHz, referenced to 1 MHz
	2-8	Average picture level drift	mp (APL)	—	±0.5	±3.0	%	10%~90% APL, referenced to 50%, variation in video modulation depth
	2-9	Sync crush level	Δsync	—	2	5	%	{1 – (Vsync/Vwhite) × (100/40)}
	2-10	Chroma beat	V_C	—	–75	–70	dB	4.43-MHz sine wave: 0.5-Vp-p input, referenced to video carrier level, P/S ratio = –13dB
	2-11-1	Spurious RF second-order harmonic	V_{2fp}	—	–30	–25	dB	Referenced to video carrier level
	2-11-2	Spurious RF third-order harmonic	V_{3fp}	—	–20	–15	dB	Referenced to video carrier level
	2-12	Spurious video signal harmonic	V_{pH}	—	–51	–46	dB	1-MHz sine wave: 0.5-Vp-p input Referenced to fp + 1 MHz fp + 2 MHz
	2-13-1	Prescaler spurious(×1/2)	$V_{PR1/2}$	—	–10	0	dBμV	fp × 1/2
	2-13-2	Prescaller spurious (×3/2)	$V_{PR3/2}$	—	10	15	dBμV	fp × 3/2
	2-14	Video carrier frequency accuracy	Δfp	—	—	±100	kHz	Series capacitance of crystal: 6 pF

	No.	Characteristics	Symbol	Min	Typ.	Max	Unit	Note
TPSG Block	3-1	TPSG modulation depth	mp (TPSG)	75	80	85	%	TPSG Mode
	3-2	TPSG V/S ratio	V/S	2.0	2.4	2.8	%	TPSG Mode
	3-3-1	TPSG horizontal sync signal cycle	Tsync	62	64	66	μs	TPSG Mode
	3-3-2	TPSG horizontal sync signal width	Wsync	3.6	4.0	4.4	μs	TPSG Mode
	3-4	TPSG white signal width	Wwhite	3.6	4.0	4.4	μs	TPSG Mode
	3-5-1	TPSG SYNC-1st signal time	W1	22	24	26	μs	TPSG Mode
	3-5-2	TPSG SYNC-2nd signal time	W2	38	40	42	μs	TPSG Mode
Sound Block	4-1	P/S ratio	$R_{P/S}$	–15	–13	–11	dB	P/S ratio: –13dB set-up, staircase (B/W) signal: 0.5-Vp-p input
	4-2-1	Minimum variable range of P/S ratio	$\Delta R_{P/}$ Smin	–19	–17	–15	dB	P/S ratio: –17dB set-up, staircase (B/W) signal: 0.5-Vp-p input
	4-2-2	Maximum variable range of P/S ratio	$\Delta R_{P/}$ Smax	–12	–10	–8	dB	P/S ratio: –10dB set-up, staircase (B/W) signal: 0.5-Vp-p input
	4-3-1	Sound modulation sensitivity (5.5 MHz/6.0 MHz/6.5 MHz)	βFM1	0.257	0.285	0.313	KHz/ mV	1-kHz sine wave: 350 mVp-p input βFM = Δf (kHz)/ 350 (mV)
	4-3-2	Sound modulation sensitivity (4.5 MHz)	βFM2	0.129	0.143	0.156	KHz/ mV	1-kHz sine wave: 350 mVp-p input βFM = Δf (kHz)/ 350 (mV)
	4-4-1	Sound S/N ratio (5.5 MHz/6.0 MHz/6.5 MHz)	S/N (FM1)	55	59	—	dB	1-kHz sine wave input, ±50 kHz Dev. = 0dB Inter Carrier demod., De-Emph = IN
	4-4-2	Sound S/N ratio (4.5 MHz)	S/N (FM2)	51	56	—	dB	1-kHz sine wave input, ±25 kHz Dev. = 0dB Inter Carrier demod., De-Emph = IN
	4-5	Sound distortion	THD	—	0.25	0.5	%	1-kHz sine wave: ±50 (25) kHz Dev.
	4-6	Sound frequency responce	f_S	—	±1	±2	dB	100 Hz~15 kHz, 1-kHz reference
	4-7-1	Sound 2nd harmonic level	V_{SH1}	—	–70	–65	dB	P/S ratio = –13dB set-up, video carrier level reference
	4-7-2	Sound 3rd harmonic level	V_{SH2}	—	–70	–65	dB	P/S ratio = –13dB set-up, video carrier level reference
	4-8	Sound carrier frequency accuracy	Δf_S	—	—	±750	Hz	X'tal series capacitance: 6 pF

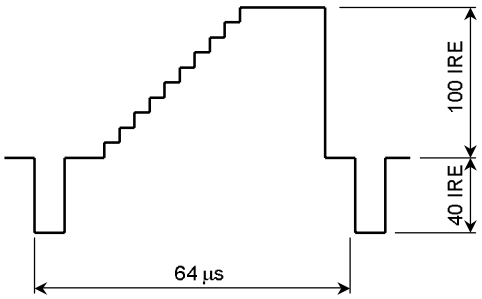
	No.	Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Logic Block	5-1	SCL clock frequency	f_{SCL}	0	—	400	kHz	
	5-2	Bus-free time between stop and start conditions	t_{BUF}	1.3	—	—	μs	After this period, the first clock pulse is generated.
	5-3	Hold time (repeated) start condition	$t_{HD;\ STA}$	0.6	—	—	μs	
	5-4	Low period for the SCL clock	t_{LOW}	1.3	—	—	μs	
	5-5	High period for the SCL clock	t_{HIGH}	0.6	—	—	μs	
	5-6	Set-up time for a repeated start condition	$t_{SU;\ STA}$	0.6	—	—	μs	
	5-7	Data hold time	$t_{HD;\ DAT}$	0	—	0.9	μs	
	5-8	Data set-up time	$t_{SU;\ DAT}$	100	—	—	ns	
	5-9	Rise time for both SDA and SCL signals	t_R	20	—	300	ns	
	5-10	Fall time for both SDA and SCL signals	t_F	20	—	300	ns	
	5-11	Set-up time for stop condition	$t_{SU;\ STO}$	0.6	—	—	μs	
	5-12	Capacitive load for each bus line	Cb	—	—	400	pF	
	5-13	Input voltage Low level for both SDA and SCL lines	V_L	0	—	1.5	V	
	5-14	Input voltage High level for both SDA and SCL lines	V_H	2.0	—	V_{CC}	V	
	5-15	Maximum Low level output voltage on SDA line	V_{ACK}	0	—	0.4	V	I sync = 3 mA
	5-16	Threshold voltage for power-on reset	V_{RESET}	2.6	3.4	4.0	V	
	5-17	Threshold voltage for External Reference Signal Input Mode	V_{EXT}	3.4	3.6	3.8	V	Pin 4 DC voltage
	5-18	Threshold voltage for test mode	V_{TEST}	3.1	3.8	4.5	V	Pin 2 DC voltage
	6-1	Negative resistance of X'tal oscillator	R_{XO}	−1	—	—	kΩ	
	6-2	Input signal level of external reference signal	V_{EXREF}	100	—	—	mVp-p	External Reference Input Mode

Input Waveforms

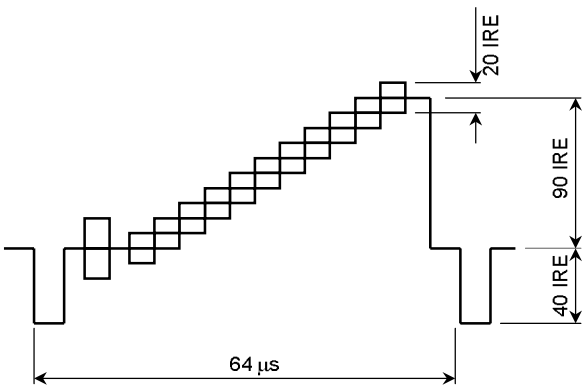
White signal



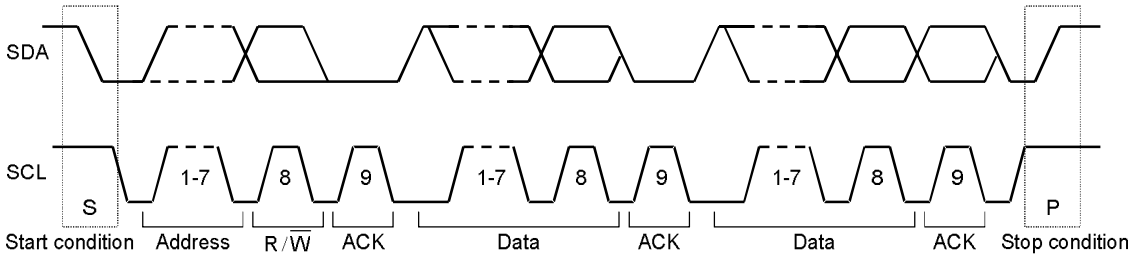
Staircase (B/W) signal APL50%



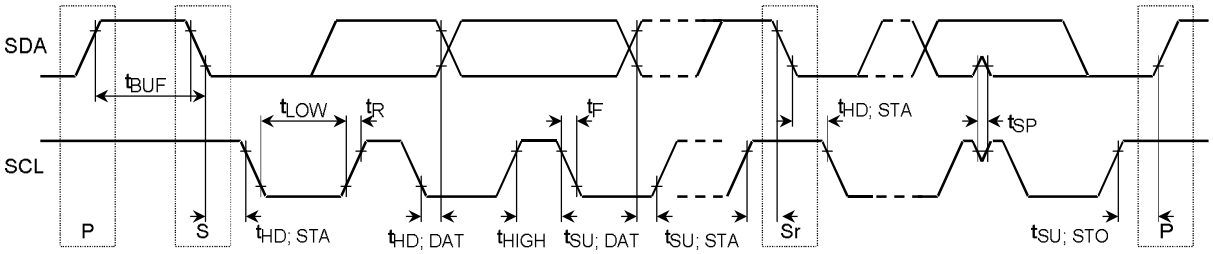
Staircase (sub-carrier 20 IRE) signal APL 50%



Data transfer on I^2C-Bus

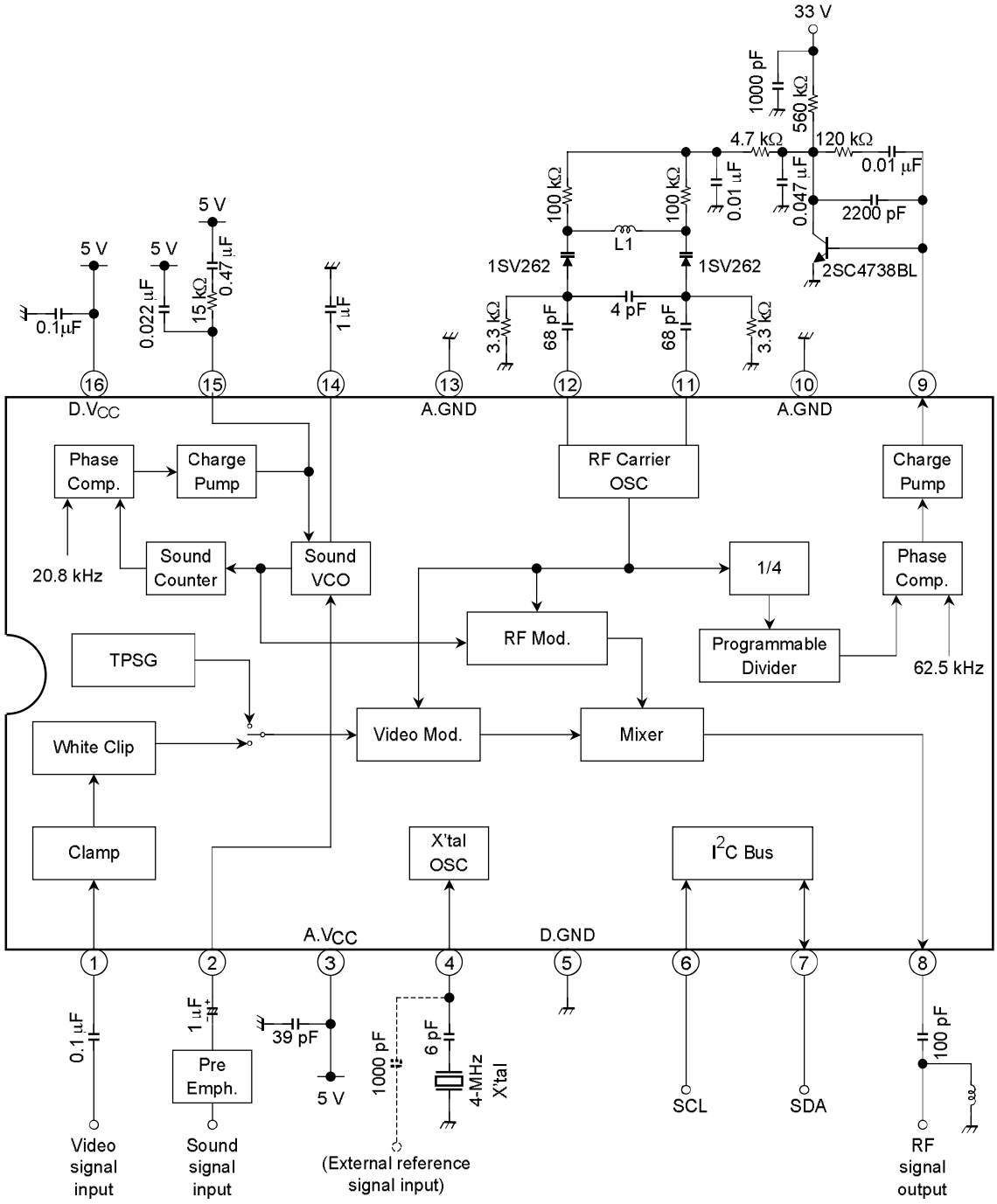


Timing requirements for I^2C-Bus



Timing charts may be simplified for explanatory purpose.

Test and Application Circuit



L1: Coil diameter = 3.2 mm, wire diameter = 0.4 mm, 2.5 turns

Handling Precautions

1. Using a human charge model (C = 100 pF, R = 1.5 kΩ, test repeated three times), the product's electrostatic resistance was determined to be low in the following cases:
   (1) When a positive voltage is applied across pin 2 and any GND pin
   (2) When a positive voltage is applied across pin 7 and any V_{CC} pin and a GND pin
   Accordingly, please handle the product with care.

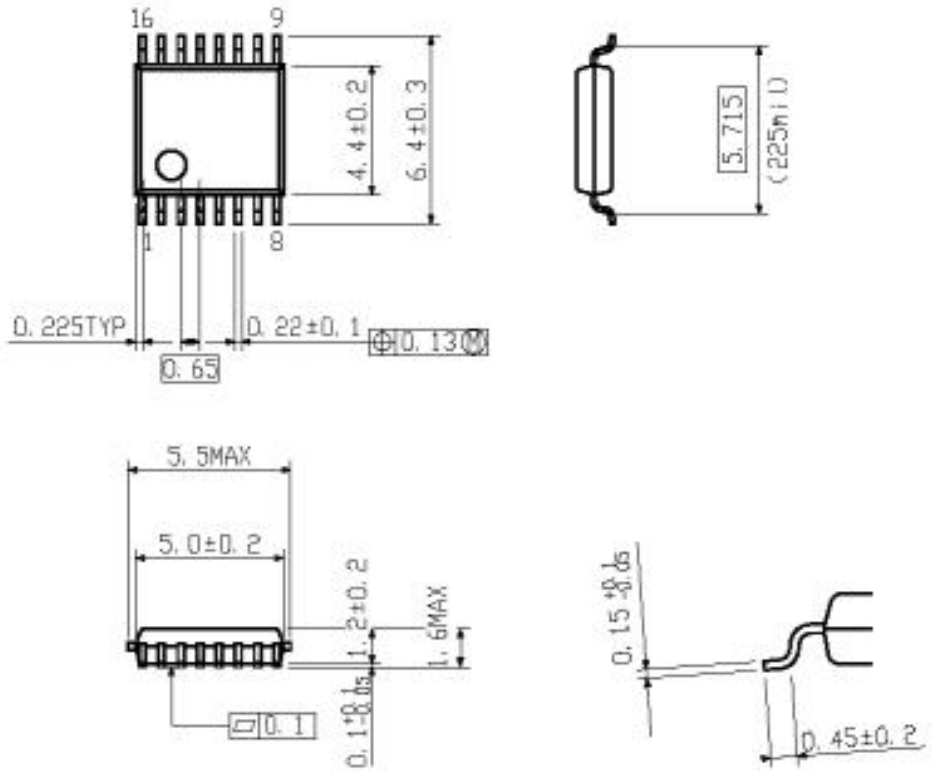
2. Do not drive the device's power supply voltage High or Low until it is attached to an inspection board or similar test assembly. Attaching the device to, or removing it from the inspection board while it is powered on may damage the device or degrade its characteristics. The power supply voltage should not be applied suddenly. Any overshoot or chattering in the power supply may result in degradation of the IC's characteristics. A filter or similar protective component should be inserted on the power supply line.

3. The sample peripheral circuits described in this document are merely intended as examples to enable the operation of the device to be evaluated. None of the peripheral circuit configurations shown or circuit constants specified are intended to be incorporated into application systems or used in designs for mass-produced equipment. Toshiba Corporation cannot assume responsibility for any damage arising from the use of any of these circuits. This is because the high-frequency characteristics of a device can vary according to a number of factors, including factors relating to the external components and the mounting pattern used. Therefore, the user must design external circuits according to the requirements of the specific application system, using this document as a reference only. The user must also test the application circuit's characteristics thoroughly. This document only guarantees device quality and characteristics as described herein; Toshiba Corporation cannot assume responsibility for any user's product design or application implementation.

4. Before attempting to use this product, the user should refer to the latest edition of the **Toshiba Semiconductor Reliability Handbook, Integrated Circuits** in order to gain a better understanding of the general principles governing the quality and reliability of Toshiba products and to learn how Toshiba seeks to enhance the management and control of product quality and reliability. The **Toshiba Semiconductor Reliability Handbook, Integrated Circuits** is also available on the semiconductor products information page of the **Toshiba Electronic Components and Materials** website at the following URL:
   < http://www.semicon.toshiba.co.jp/eng/prd/common/index.html>.

(Last updated: Jul. 2003)

Package Dimensions



Weight: 0.07 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
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