

# IrDA Transceiver with Encoder/Decoder

## FEATURES

- Micropower in the Sleep Mode, (2 $\mu$ A)
- 3V to 5V Operation
- Wide Dynamic Receiver Range from 200nA to 50mA Typical
- Direct Interface to IrDA Compatible UARTs or Super I/O ICs
- Supports IrDA Standard to 115.2kbps Data Rates
- Transmitter Output Stage Capable to 500mA Sink Current
- IrDA Compliant Modulation & Demodulation Scheme
- Direct Interface to Standard UART
- 16 Pin SSOP, SOIC and DIL Package

## DESCRIPTION

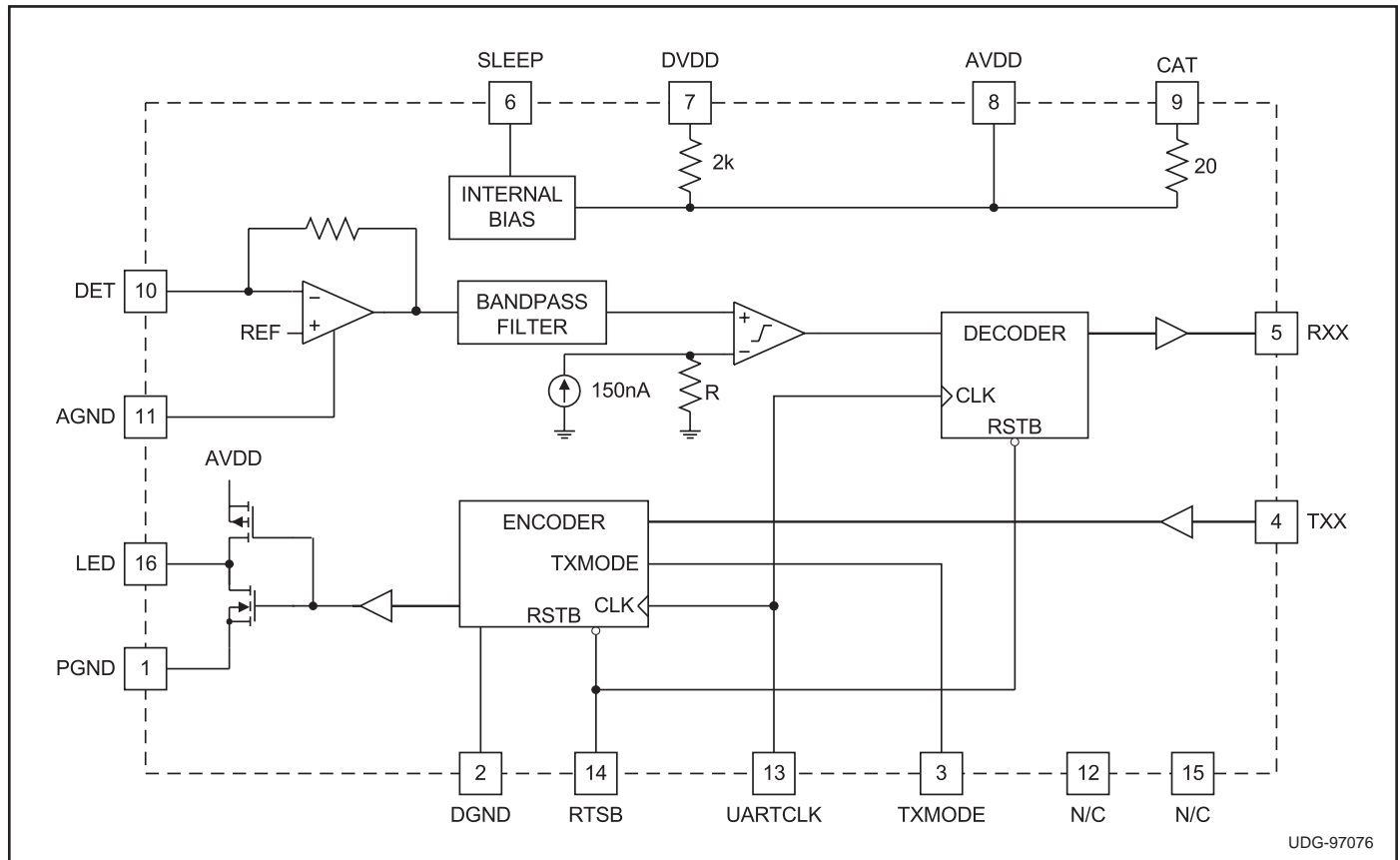
The UCC5343 IrDA Transceiver with Encoder/Decoder supports the Physical Layer specifications of the IrDA standard. Additional functionality is provided by data format translation between standard UART and IrDA formats. The UCC5343 is readily interfaced to a standard UART.

The Receiver has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses into a UART. The receiver is capable of detecting input currents ranging from 200nA to greater than 50mA. The receiver signal path is frequency limited by an internal bandpass filter to reduce interference from other sources of IR energy.

The output of the receiver is designed for direct interface to standard UARTs and Super I/O devices up to 115.2kbps. Internal resistors are provided for decoupling the pin diode supply, minimizing the number of required external components.

The UCC5343 has low current consumption in the active mode, making it excellent for applications with low power requirements. The transmitter section has a low impedance open drain MOSFET output. It is capable of sinking 300mA from an output LED at 3V and 500mA at LED at 5V.

## BLOCK DIAGRAM

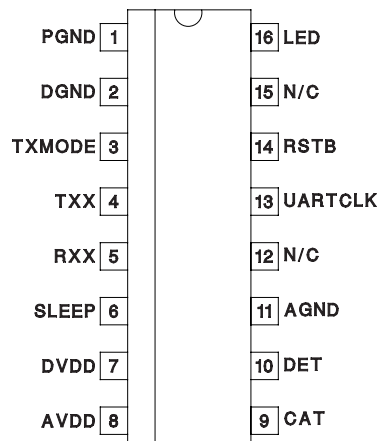


UDG-97076

**ABSOLUTE MAXIMUM RATINGS**

AVDD, DVDD, CAT . . . . . –0.3V to 7V  
 SLEEP, DET, TXX, LED,  
 DVDD, CAT . . . . . –0.3mA to AVDD + 0.3mA  
 IRXX . . . . . –10mA to 10 mA  
 IDET . . . . . 250mA  
 ILED . . . . . 1A  
 Power Supply . . . . . TBA  
 Storage Temperature . . . . . –65°C to +150°C  
 Junction Temperature . . . . . –55°C to +150°C  
 Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are positive with respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

**CONNECTION DIAGRAM****SSOP-16, SOIC-16 and DIL-16 (Top View)  
M Package, D and N Packages**

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, 0°C < T<sub>A</sub> < 70°C T<sub>A</sub> = 0°C to 70°C, AVDD = 3V to 5.5V, C<sub>AVDD</sub> = 100nF, C<sub>DVDD</sub> = 100nF, C<sub>CAT</sub> = 4.7μF + 100nF, C<sub>RXX</sub> = 40pF, C<sub>DET</sub> < 56pF. T<sub>A</sub> = T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Current Section</b>					
I <sub>DD</sub>	No Output Load, SLEEP ≤ 0.5V		280	450	μA
	SLEEP > AVDD – 0.5V		1	3	μA
R <sub>VDD</sub>	AVDD to DVDD	1.0	2	3.0	kΩ
R <sub>CAT</sub>	AVDD to CAT	15	20	32	Ω
<b>Receiver Section</b>					
Input Referred Noise	(Note 1)		10		$\frac{pA}{\sqrt{Hz}}$
Detection Threshold			200	400	nA
DetectionThreshold Signal to Noise Ratio	IDET = 200nA (Note 1)		11.8		
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 200nA Peak to 20mA Peak and 0 to 200μADC, 1.6μS Peak f <sub>UARTCLK</sub> = 2MHz		8.95		μS
RXX Output (VOL)	IRXX = 800μA		200	400	mV
RXX Output (VOH)	IRXX = –100μA, DVDD - RXX		200	400	mV
RXX Rise Time	10% to 90% of DVDD		150	200	nS
RXX Fall Time	90% to 10% of DVDD		100	150	nS
<b>Transmitter Section</b>					
I <sub>TXX</sub>	TXX = 0 to AVDD	–1		1	μA
TXX (VIH)	DVDD = 5V	0.7 • DVDD		DVDD	V
TXX (VIL)	DVDD = 5V	0		0.3 • DVDD	V
LED	TXX = 0, AVDD = 4.5V, ILED = 500mA		0.3	0.6	V
	TXX = 0, AVDD = 3V, ILED = 300mA		0.3	0.6	V
<b>Encoder Transmit Section</b>					
Encoder Output Pulse Width	TXMODE = VDD	1.41		2.23	μS

Note 1: Guaranteed by Design. Not 100% tested in production.

## PIN DESCRIPTIONS

**AGND:** Ground pin for analog circuits.

**AVDD:** Supply pin for analog circuits. Bypass to AGND with 100nF or 1 $\mu$ F capacitor.

**CAT:** This pin is a filtered supply for PIN diode cathode. Internally connected to AGND with a 20 $\Omega$  resistor. Bypass to a GND with a 4.7 $\mu$ F electrolytic capacitor and a 100nF ceramic capacitor.

**DET:** This is the input to the receiver amplifier. Connect pin diode anode to this pin.

**DGND:** Ground pin for digital circuits.

**DVDD:** Supply pin for digital circuits. Internally connected to AVDD through 2k resistor. This pin must be bypassed to DGND with a 100nF or 1 $\mu$ F ceramic capacitor.

**LED:** LED pin is the output of the transmitter section of the chip. The signal on this pin is the IrDA encoded version of the UART transmit signal.

**PGND:** Ground pin for the transmitter power device. This pin should be connected to the circuit board ground plane.

**RSTB:** This active low input signal is used to reset the encoder and decoder sections of the chip. This signal must be provided by the system during startup.

**RXX:** RXX is the demodulated receive signal. Normally this pin is tied to SIN signal of UART. TTL/CMOS compatible output from the receiver stage to an IrDA UART. This output is digitally decoded (pulse stretched).

**SLEEP:** Sleep mode select pin. A logic high on SLEEP pin puts the chip into a low current mode.

**TXMODE:** TXMODE is used to select the modulation mode. If TXMODE is set high (1) the signal on TXD pin will have the output pulse width of 1.6 $\mu$ S. If TXMODE is set low (0), the output will have the pulse width of 3/16 of the UARTCLK frequency.

If TXMODE pin is left floating, the output will default to 1.6 $\mu$ S pulse width.

**TX:** Input from the UART. This pin is normally tied to SOUT signal of UART.

**UARTCLK:** Input of the system clock. This frequency must set at 16 times the IrDA data rate, and must be available from the UART.

## APPLICATION INFORMATION

Figures 1 and 2 outline the IrDA SIR encoding scheme. The encoding scheme relies on a clock being present. The clock must be set to 16 times the data transmission baud rate. The encoder sends a pulse for every space (0) that is sent. On a high to low transition of TXD signal, the generation of the pulse is delayed for 7 clock cycles of

the 16XCLK before the pulse is set high for 3/16 of a bit time or 1.6 $\mu$ s the pulse width is selected by TXMODE. For consecutive spaces, pulses with 1 bit time delay are generated in series. If a logic 1 (mark) is sent, the encoder does not generate a pulse.

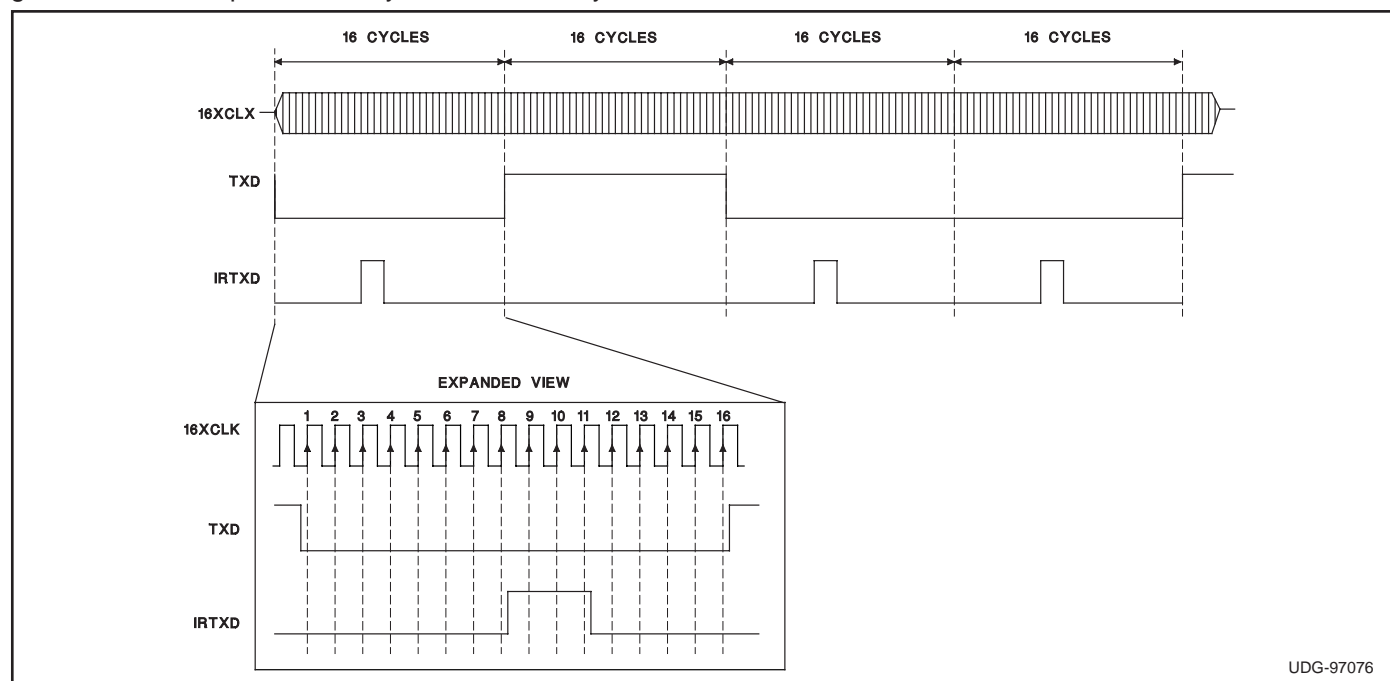
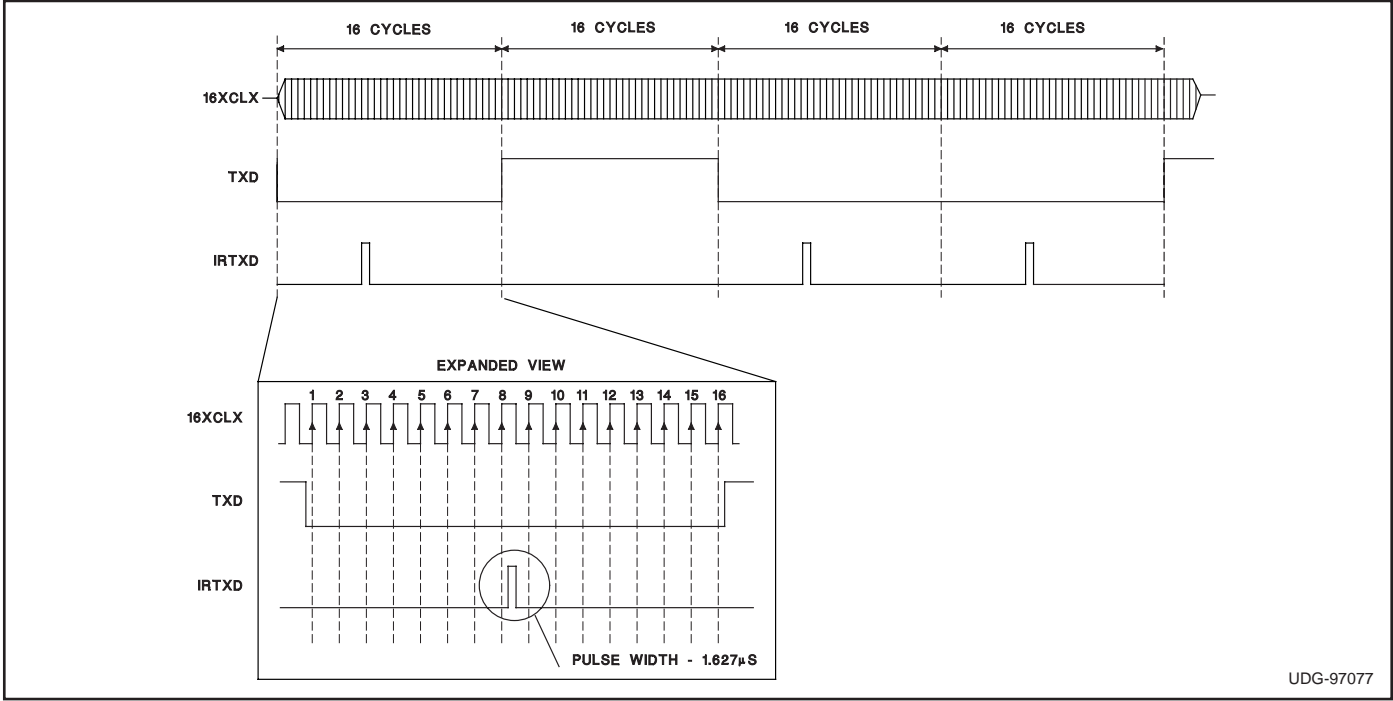


Figure 1. IrDA Encoder Timing Diagram

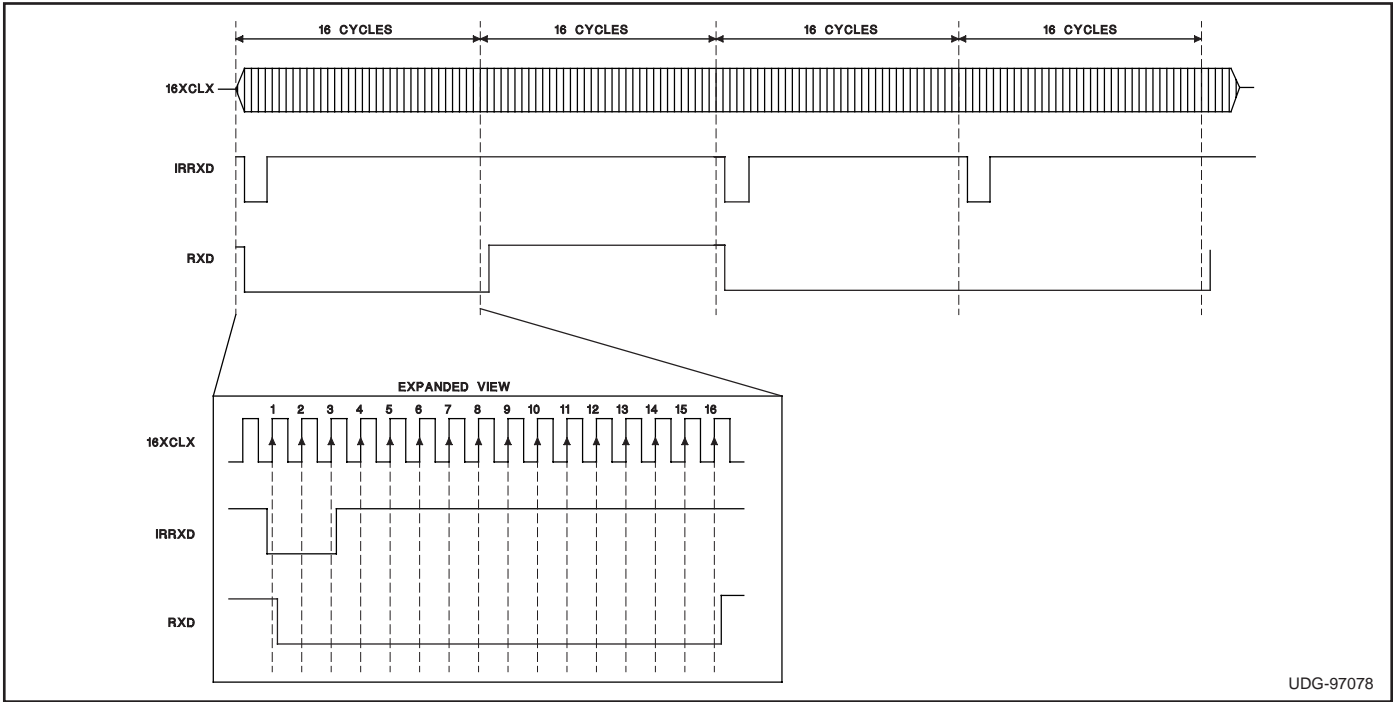
# APPLICATION INFORMATION (cont.)



**Figure 2. IrDA Encoder Timing Diagram (1.6µs Pulse Width)**

The IrDA SIR decoding modulation method performs a pulse stretching function. Every high to low transition of the IRRXD line signifies an arrival of a 3/16th pulse. This pulse needs to be stretched to accommodate 1 bit time (or 16 of 16XCLK cycles). Every pulse that is received

is translated into a space (0) on the RXD output. If a series of pulses separated by 1 bit time are received, then the result is a 1 bit time low pulse for every 3/16 pulse received. The decoding scheme is shown in Figure 3.



**Figure 3. IrDA Decoder Timing Diagram**

## APPLICATION INFORMATION (cont.)

### Ground Plane

There are 3 ground connections shown on the application drawing. They represent the sensitive analog ground, the dirty digital ground, and the high current transmitter ground. These 3 points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provision to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

### DET Considerations

The DET circuit board trace should be surrounded with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 100nF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

### Analog Power Supply De-coupling

The UCC5343 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs from the AVDD supply and draws high peak currents (~ 500 mA in a typical application). A bulk capacitor may be required physically close to the AVDD and AGND pins if the connection length to the power supply is long or if the supply is or appears to be relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit.

### Digital Power Supply

DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass cap handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2k resistor will allow, an external resistor can shunt it. This technique should always be accompanied by increasing the value of the de-coupling capacitor on DVDD and AVDD.

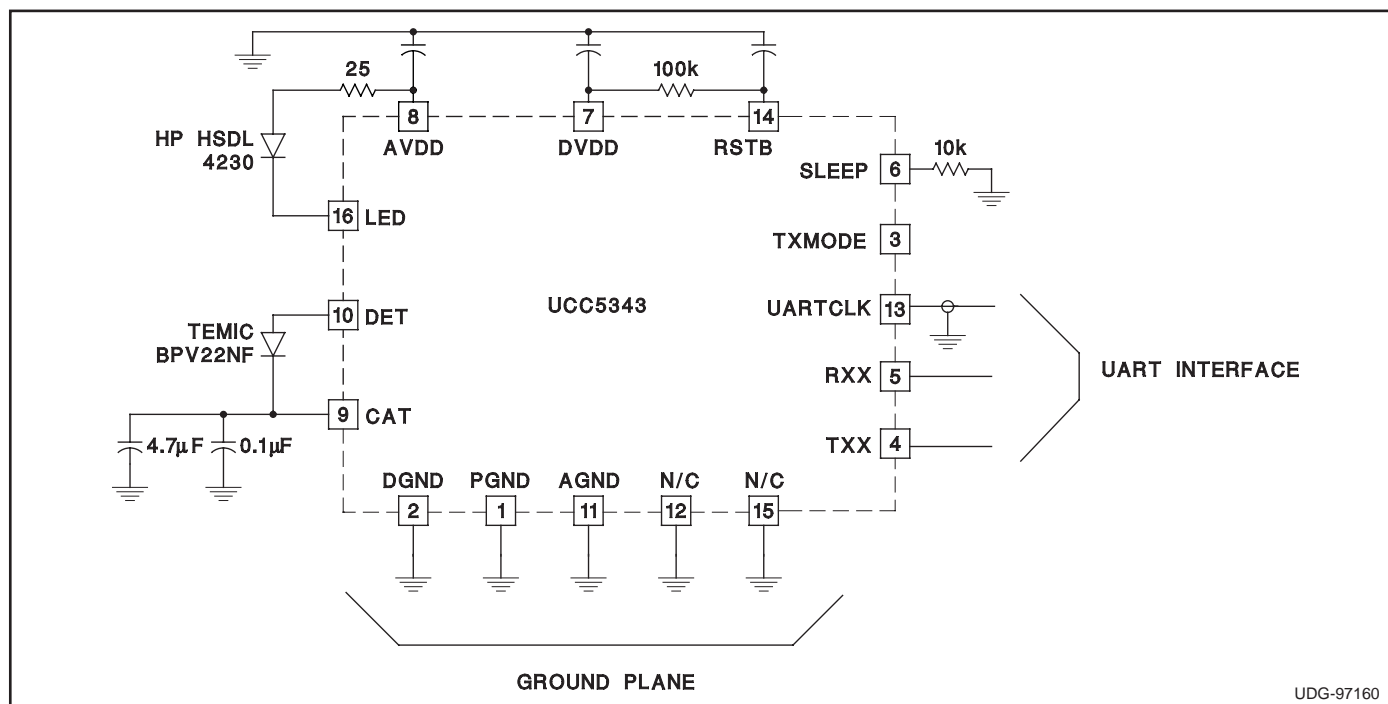


Figure 4. IrDA Transceiver with UART Encoder/Decoder Logic

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