www.ti.com

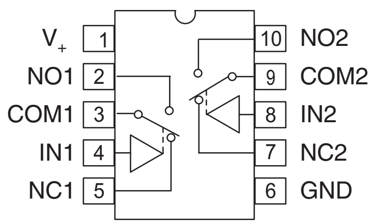
FEATURES

- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (0.3 Ω Max)**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 3.6-V Single-Supply Operation**
- **Control Inputs Are 1.8-V Logic Compatible**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

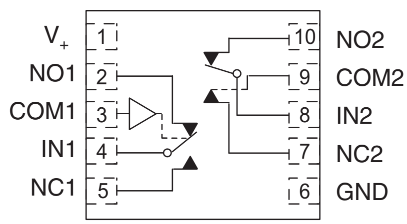
APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio and Video Signal Routing**
- **Low-Voltage Data-Acquisition Systems**
- **Communication Circuits**
- **Modems**
- **Hard Drives**
- **Computer Peripherals**
- **Wireless Terminals and Peripherals**

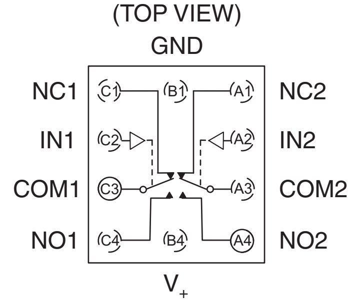
MSOP PACKAGE
(TOP VIEW)



SON PACKAGE
(TOP VIEW)



NanoFree™ PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS3A24159 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	NanoFree™ (DSBGA) – YZP	Reel of 3000	TS3A24159YZPR	PREVIEW
	VSSOP – DGS (MSOP)	Reel of 2500	TS3A24159DGSR	L8R
	QFN – DRC (SON)	Reel of 3000	TS3A24159DRCR	ZWS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

SUMMARY OF CHARACTERISTICS[(1)]

Configuration	Dual 2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	0.3 Ω Max
ON-state resistance match (Δr_{on})	0.05 Ω Max
ON-state resistance flatness ($r_{on(flat)}$)	0.04 Ω Max
Turn-on/turn-off time (t_{ON}/t_{OFF})	20 ns/12 ns
Break-before-make time (t_{BBM})	10 ns
Charge injection (Q_C)	9 pC
Bandwidth (BW)	23 MHz
OFF isolation (O_{ISO})	–72 dB
Crosstalk (X_{TALK})	–96 dB
Total harmonic distortion (THD)	0.003%
Power-supply current (I_+)	15 nA
Package options	10-pin MSOP, SON, WCSP

(1) V_+ = 2.7 V, T_A = 25°C

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[3]		–0.5	3.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[3][4][5]		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–300	300	mA
	ON-state peak switch current[6]		–500	500	
V_I	Digital input voltage range		–0.5	3.6	V
I_{IK}	Digital input clamp current[3][4]	V_I < 0	–50		mA
I_+	Continuous current through V+			100	mA
I_{GND}	Continuous current through GND		–100		mA
θ_{JA}	Package thermal impedance[7]	DGS package		165	°C/W
		DRC package		56.5	
		YZP package		TBD	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 3-V Supply(1)

V_+ = 2.7 to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.2	0.3	Ω
				Full				0.35	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.26	0.3	Ω
				Full				0.34	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.01	0.05	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V		0.13		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 10	25°C			0.01	0.04	Ω
				Full				0.05	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 11	25°C	3.6 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch ON, See Figure 12	25°C	3.6 V	–10		10	nA
				Full		–100		100	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.4			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 3.6 V or 0		25°C	3.6 V	–40	5	40	nA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3-V Supply(1) (Continued)

V_+ = 2.7 to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	3 V		20	35	ns
				Full	2.7 V to 3.6 V			40	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	3 V		12	25	ns
				Full	2.7 V to 3.6 V			30	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	3 V	1	10	25	ns
				Full	2.7 V to 3.6 V	0.5		30	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	3 V		9		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 13	25°C	3 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 13	25°C	3 V		224		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 13	25°C	3 V		250		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 13	25°C	3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	SeeFigure 16	25°C	3 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	3 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	3 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	3 V		0.003		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND		25°C	3.6 V		15	100	nA
				Full				1	µA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			0.35	Ω
				Full				0.45	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V				Ω
				Full				0.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.01	0.05	Ω
				Full			0.05	0.05	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.05		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.03	0.08	
				Full				0.1	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 11	25°C	2.7 V	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch ON, See Figure 12	25°C	2.7 V	–10		10	nA
				Full		–100		100	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.25			V
Input logic low	V_{IL}			Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	V_I = 2.7 V or 0		25°C	2.7 V	–40	5	40	nA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply(1) (Continued)

V_+ = 2.3 to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	2.5 V		23	45	ns
				Full	2.3 V to 2.7 V			50	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	2.5 V		17	27	ns
				Full	2.3 V to 2.7 V			30	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.5 V	2	14	30	ns
				Full	2.3 V to 2.7 V	1		35	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 19	25°C	2.5 V		8		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 13	25°C	2.5 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 13	25°C	2.5 V		250		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 13	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	2.5 V		–72		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	2.5 V		–96		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V		0.003		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND		25°C	2.7 V		10	100	nA
				Full				700	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.4	0.9	Ω
				Full				0.8	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.3	0.45	Ω
				Full				0.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.02	0.04	Ω
				Full				0.05	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le (V_{NO}$ or $V_{NC}) \le V_+$, I_{COM} = –2 mA,	Switch ON, See Figure 10	25°C	1.65 V		0.13		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C			0.08	0.15	
				Full				0.2	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 11	25°C	1.95	–10		10	nA
				Full		–50		50	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, See Figure 12	25°C	1.95 V	–10		10	nA
				Full		–100		100	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1			V
Input logic low	V_{IL}			Full				0.4	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		25°C	1.95 V	–40	5	40	nA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply[1] (Continued)

V_+ = 1.65 to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	1.8 V		53	75	ns
				Full	1.65 V to 1.95 V			30	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	25°C	1.8 V		24	35	ns
				Full	1.65 V to 1.95 V			40	
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.8 V	2	30	40	ns
				Full	1.65 V to 1.95 V	1		50	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, SeeFigure 19	25°C	1.8 V		5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 13	25°C	1.8 V		90		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 13	25°C	1.8 V		250		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		23		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	1.8 V		–73		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	1.8 V		–97		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	1.8 V		0.005		%
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND		25°C	1.95 V		100	50	nA
				Full				700	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

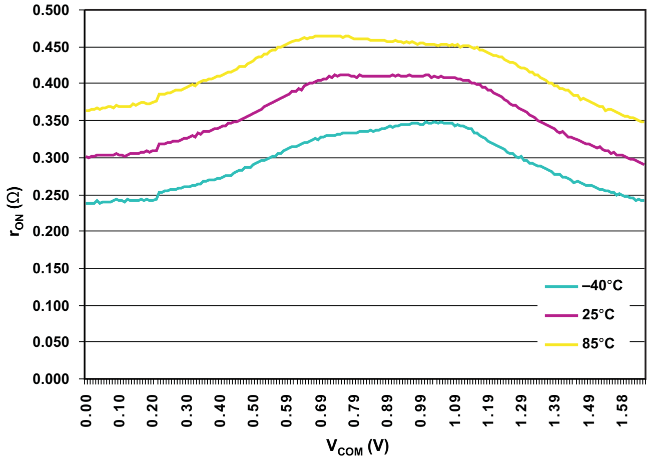


Figure 1. r_{ON} vs V_{COM} (V+ = 1.65 V)

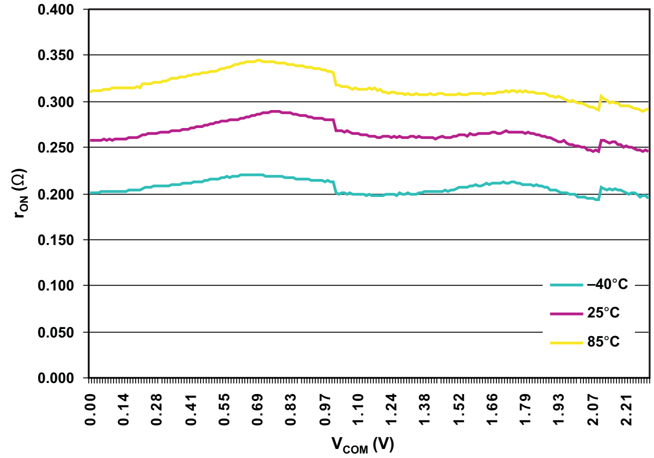


Figure 2. r_{ON} vs V_{COM} (V_+ = 2.3 V)

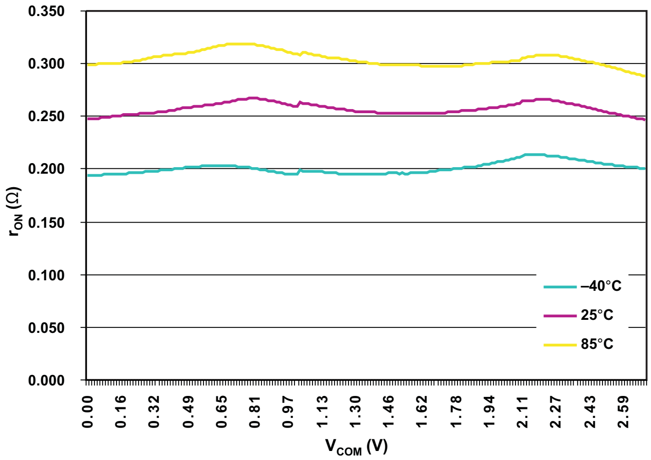


Figure 3. r_{ON} vs V_{COM} (V_+ = 2.7 V)

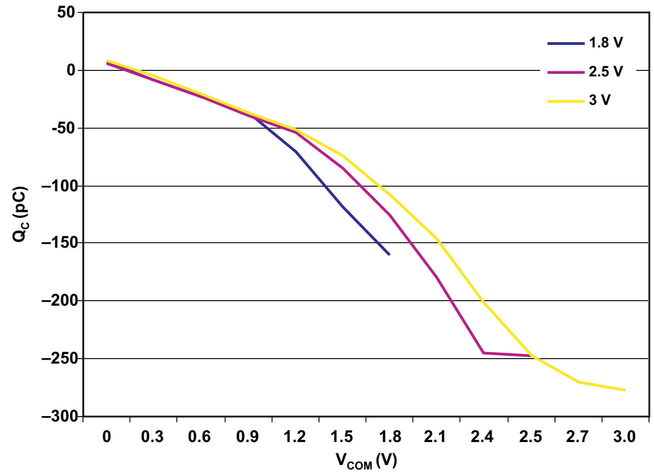


Figure 4. Charge Injection (Q_C) vs V_{COM} (T_A = 25°C)

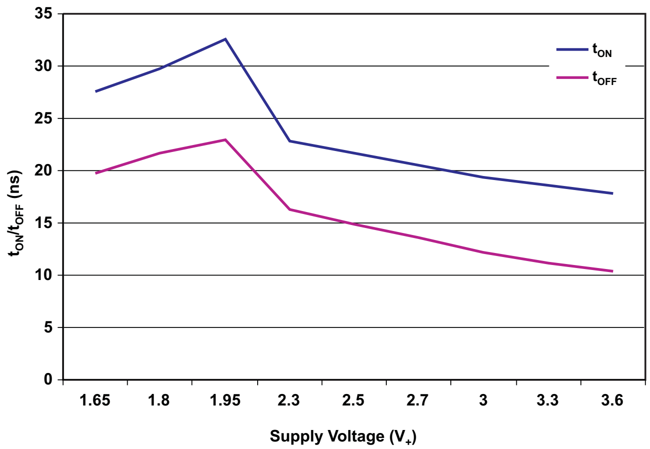


Figure 5. t_{ON} and t_{OFF} vs Supply Voltage (T_A = 25°C)

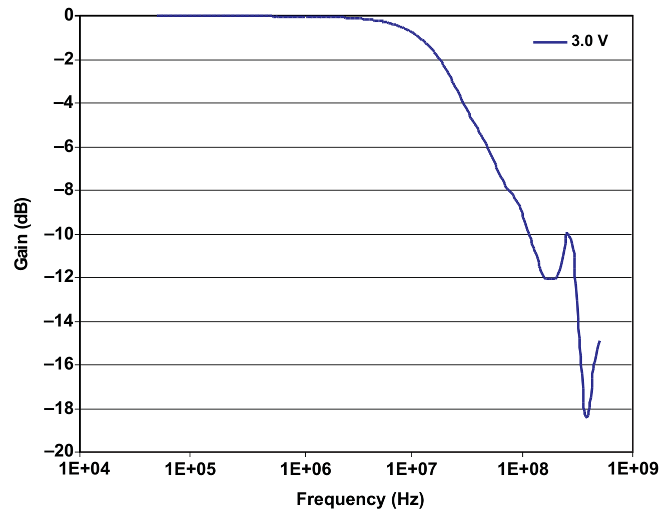


Figure 6. Bandwidth

TYPICAL PERFORMANCE (continued)

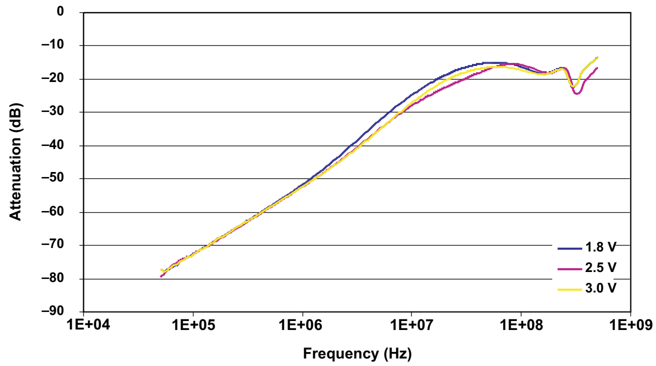


Figure 7. OFF Isolation

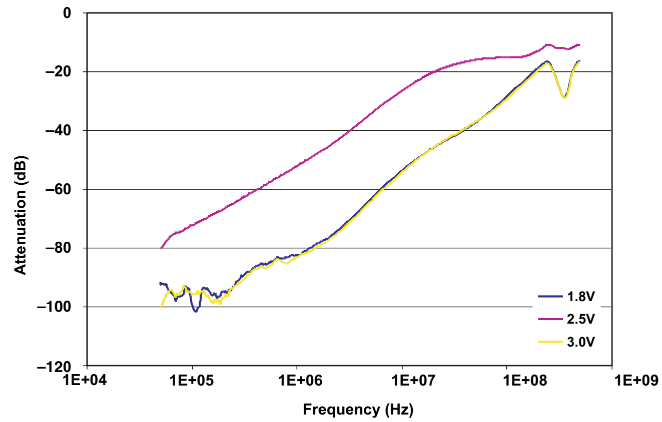


Figure 8. Crosstalk

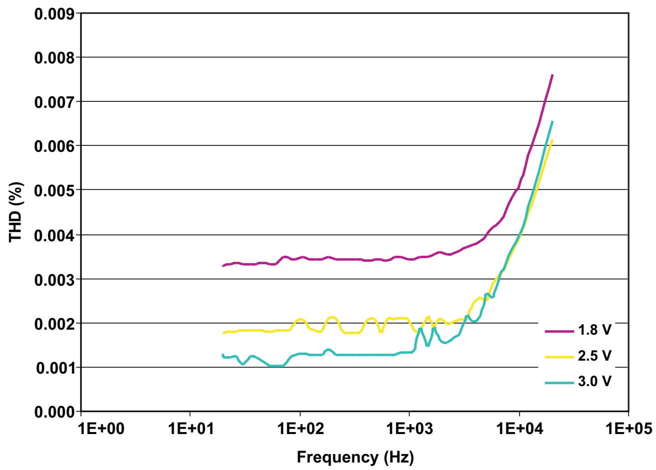


Figure 9. Total Harmonic Distortion vs Frequency

PARAMETER MEASUREMENT INFORMATION

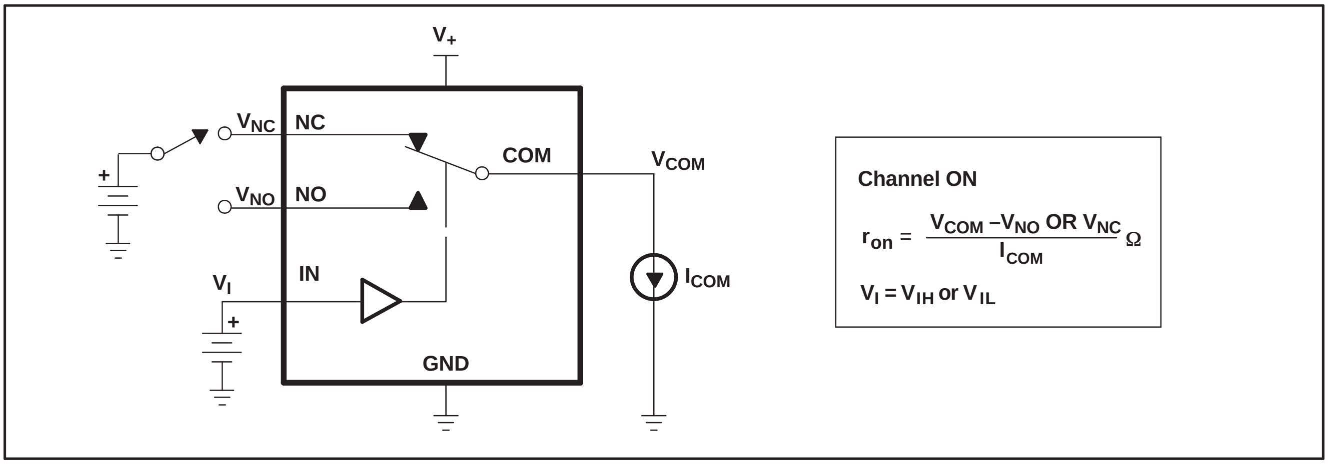


Figure 10. ON-State Resistance

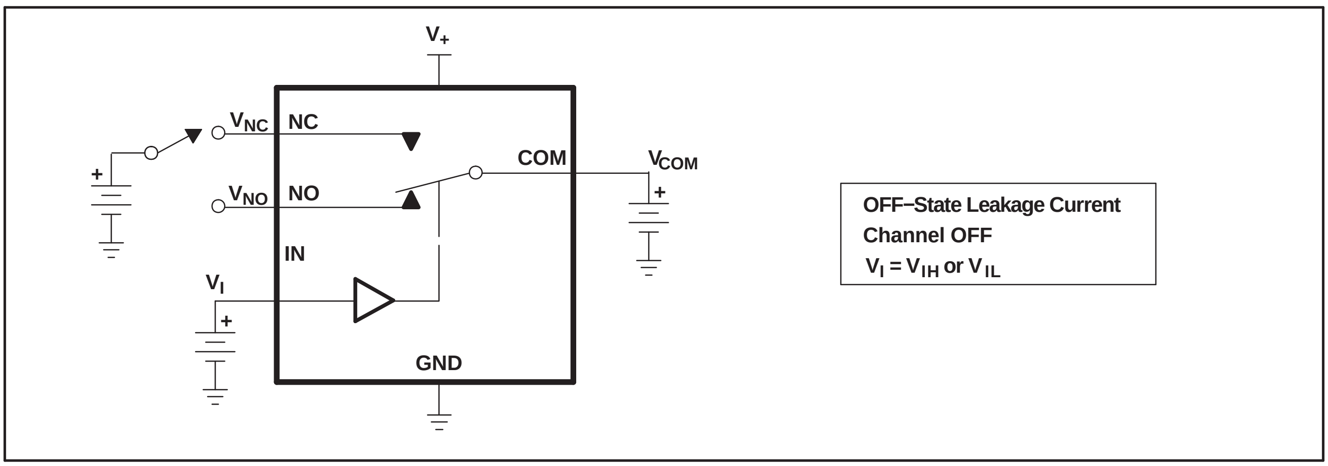


Figure 11. OFF-State Leakage Current
($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

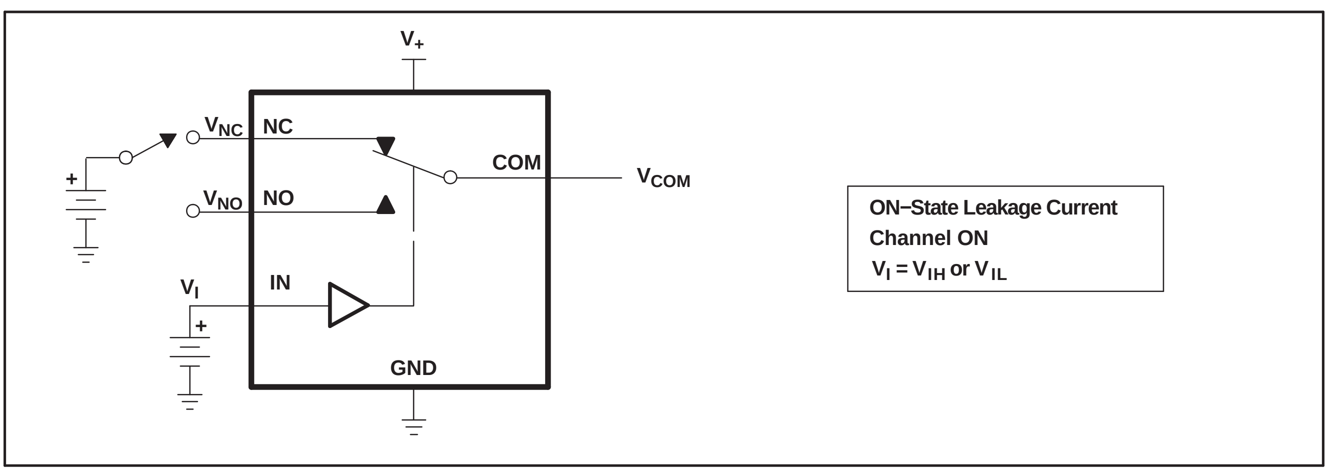


Figure 12. ON-State Leakage Current
($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

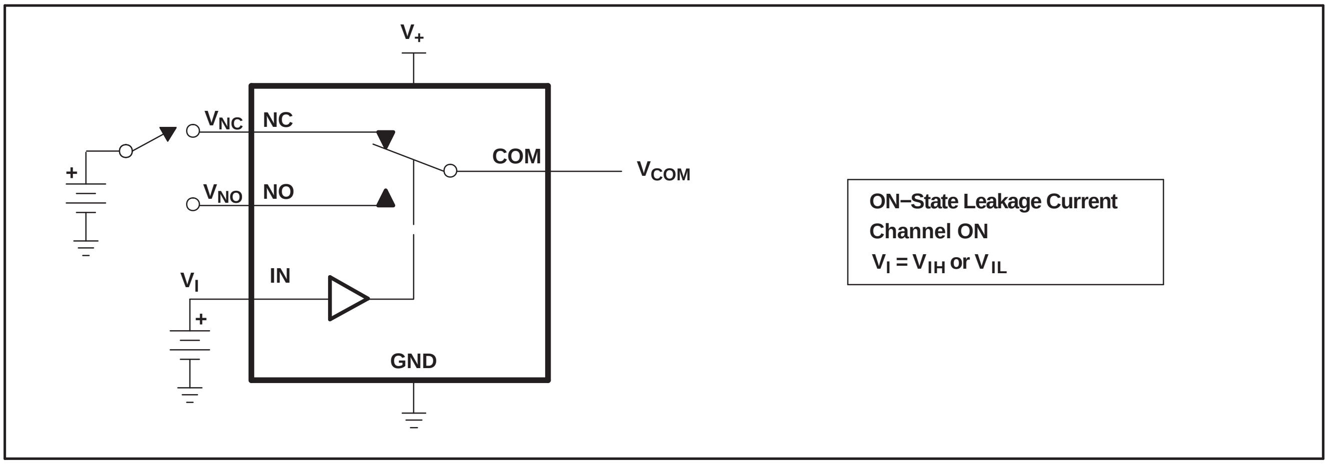
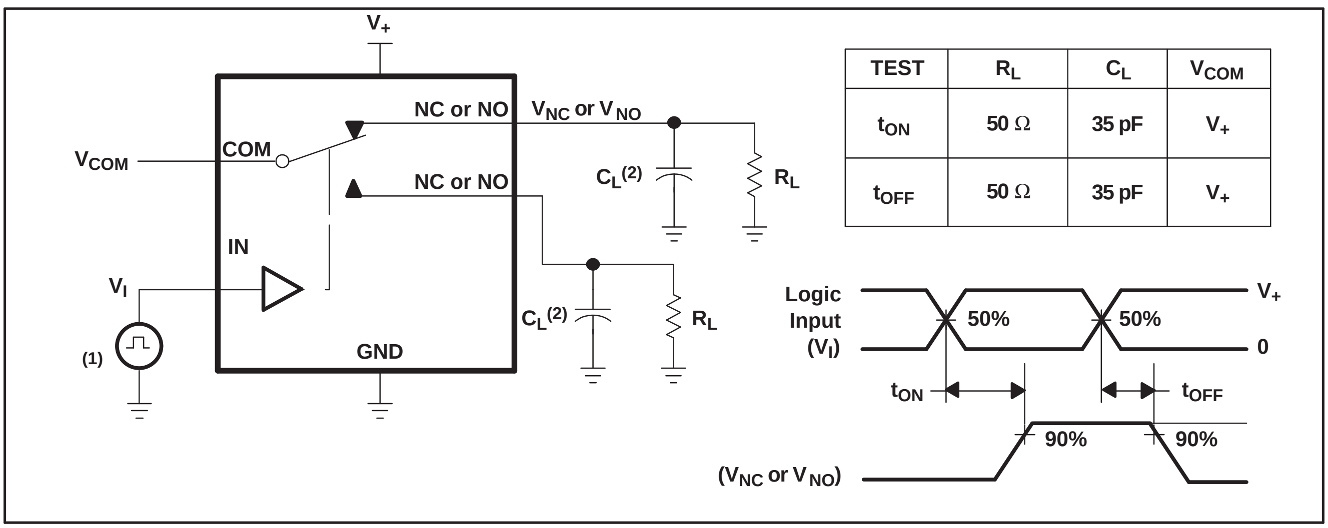


Figure 13. Capacitance
(C_I, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



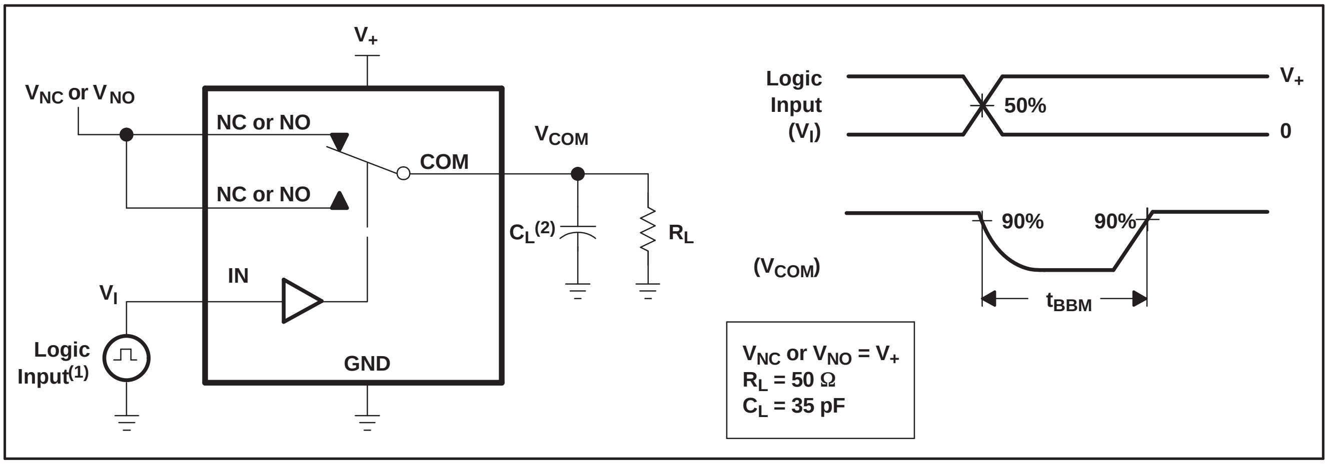
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 14. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

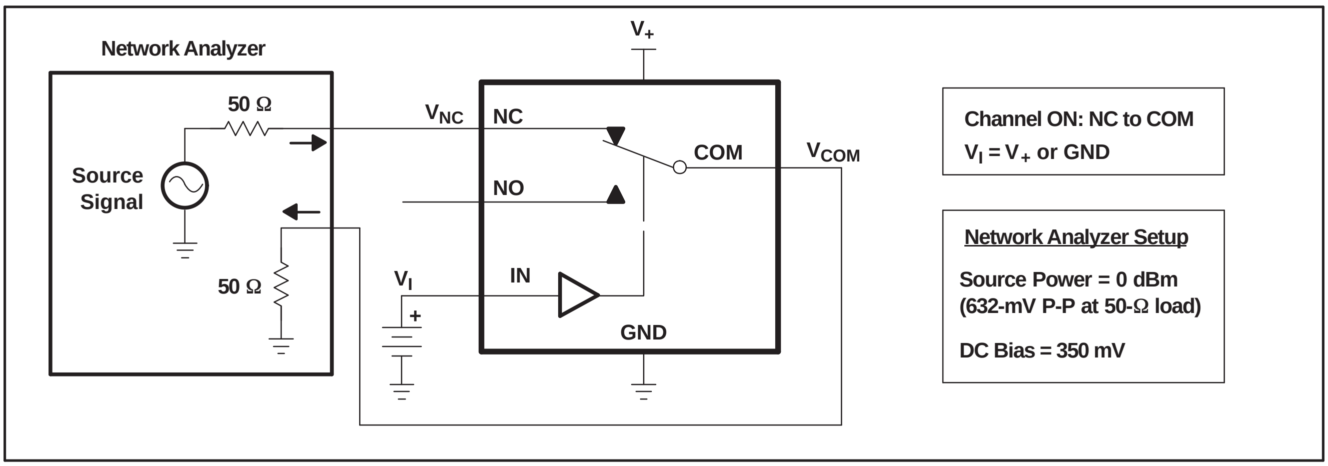


Figure 16. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

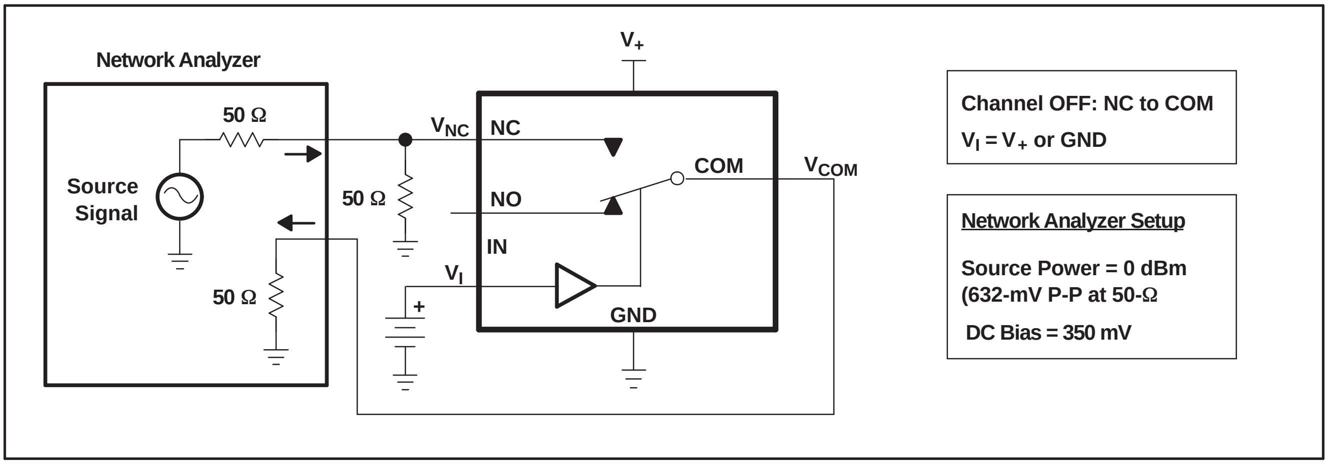


Figure 17. OFF Isolation (O_{ISO})

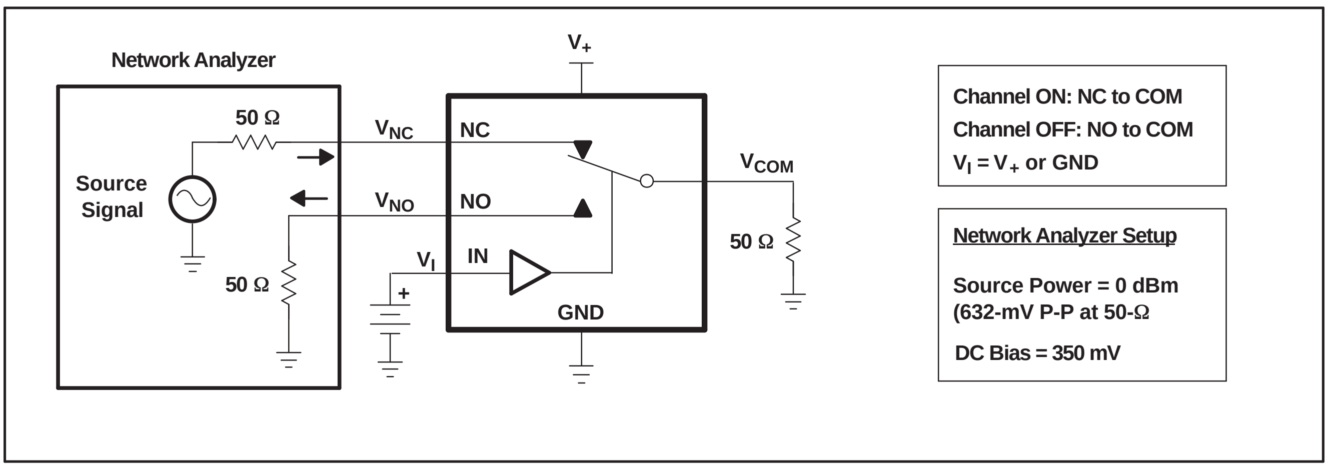
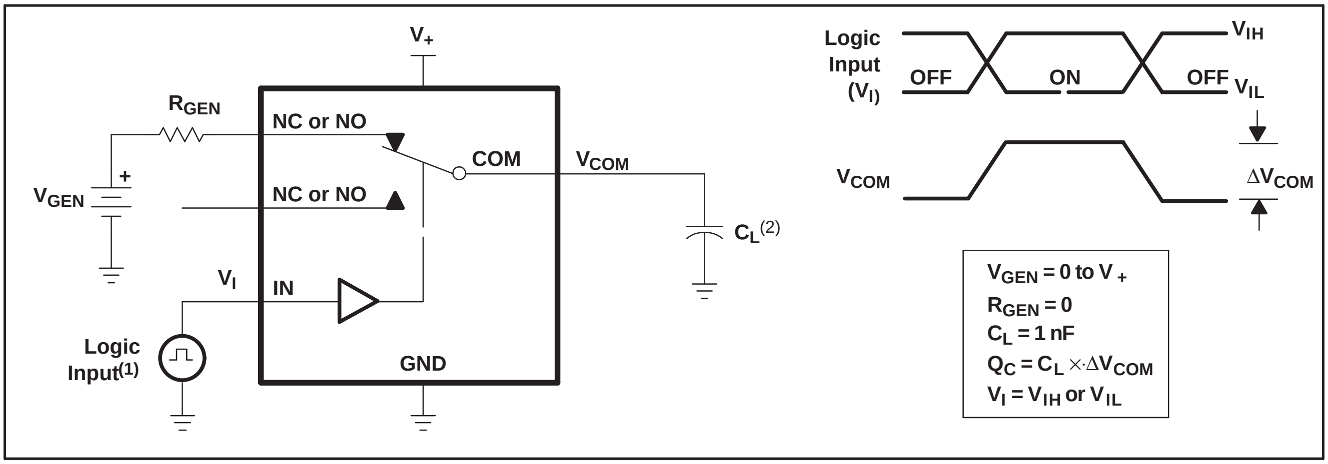


Figure 18. Crosstalk (X_{TALK})

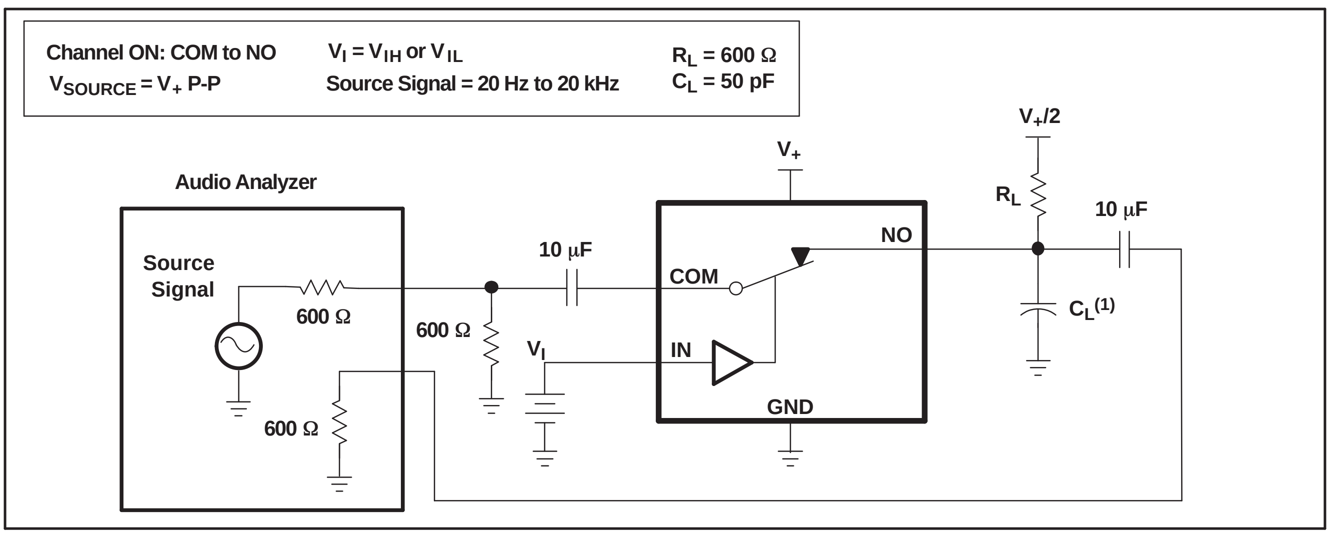
PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS3A24159DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3A24159DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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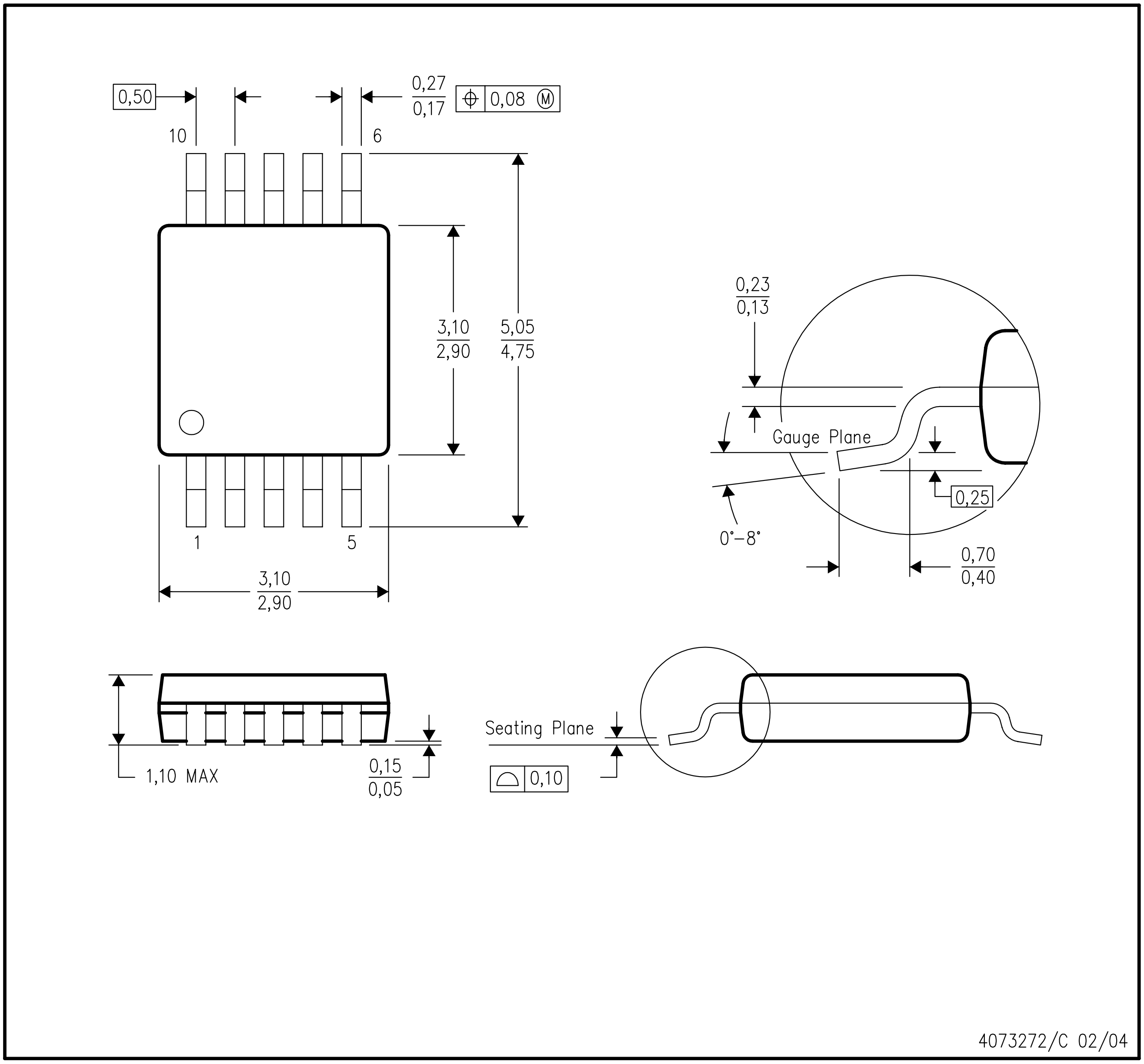
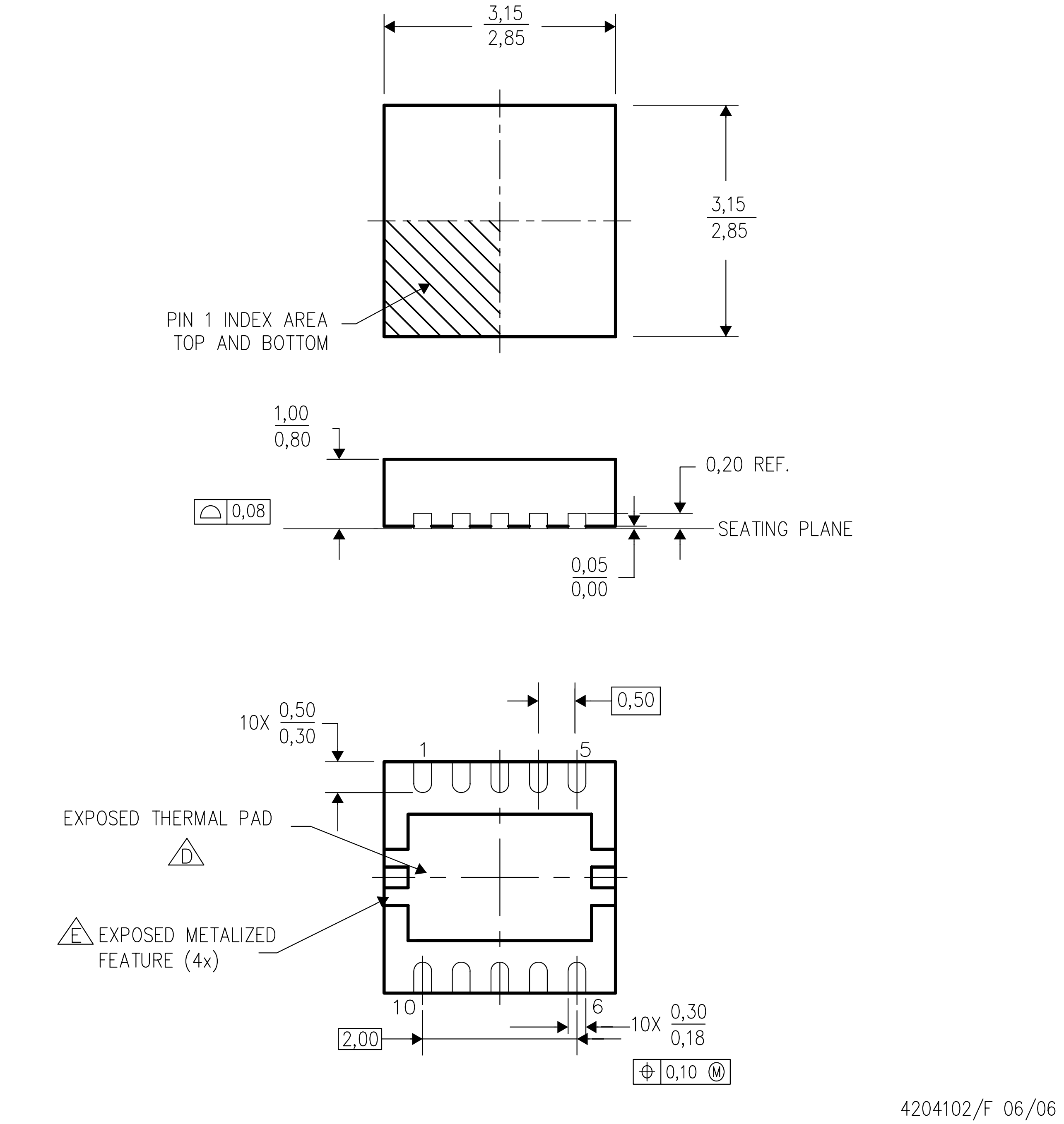
DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



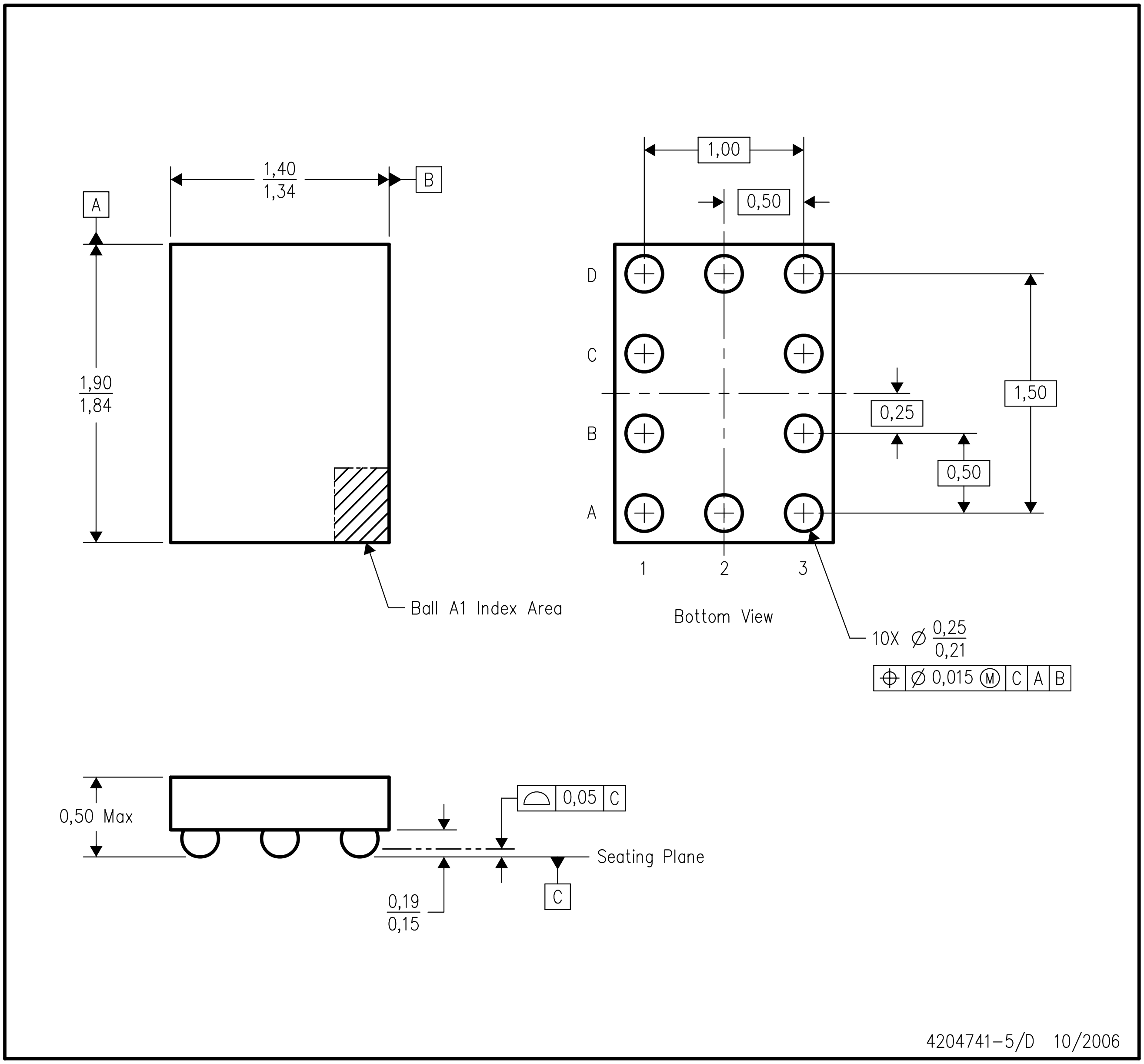
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

DRC (S-PDSO-N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

YZP (R–XBGA–N10) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is a lead–free solder ball design.

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