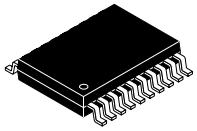
TEXAS INSTRUMENTS



SLOS386 – NOVEMBER 2001

2-W STEREO AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS

FEATURES

- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2-W/Ch Output Power Into 3-Ω Load From 5-V Supply**
- **Fully Differential Input**
- **Low Supply Current . . . 6-mA Typical**
- **Depop Circuitry**

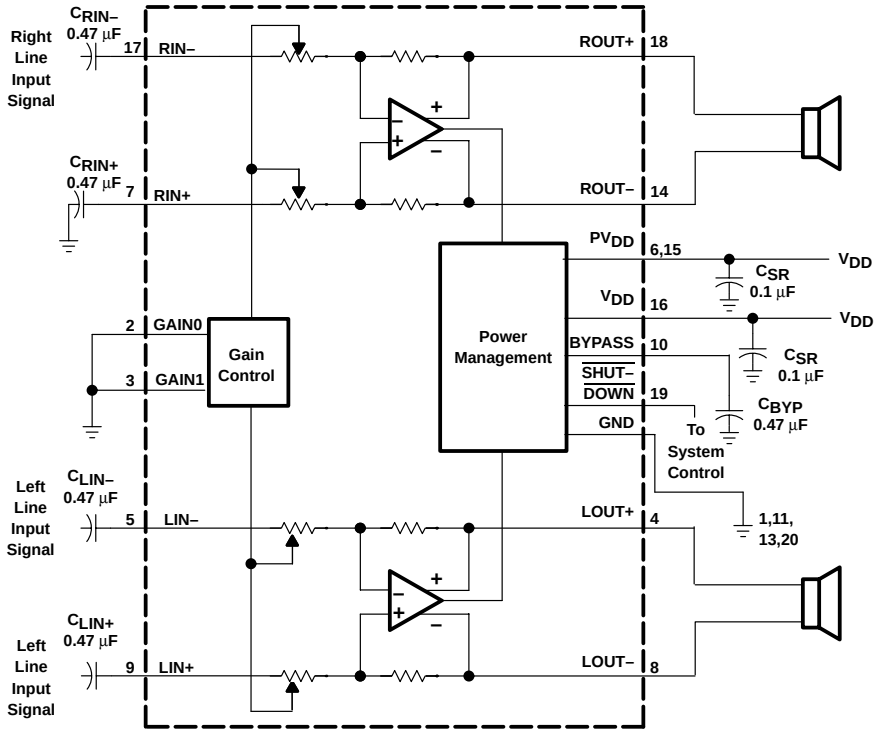
APPLICATIONS

- **Notebook Computers, PDAs, and Other Portable Audio Devices**

DESCRIPTION

The TPA6017A2 is a stereo audio power amplifier in a 20-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. Internal gain control minimizes the number of external components needed, simplifying the design, and freeing up board space for other features.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). Gain settings of 6 dB, 10 dB, 15.6 dB, and 21.6 dB (inverting) are provided.



Application Circuit

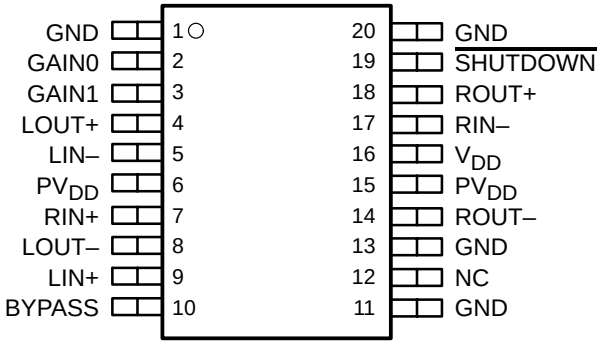
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA6017A2PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6017A2PWPR).

PWP PACKAGE
(TOP VIEW)

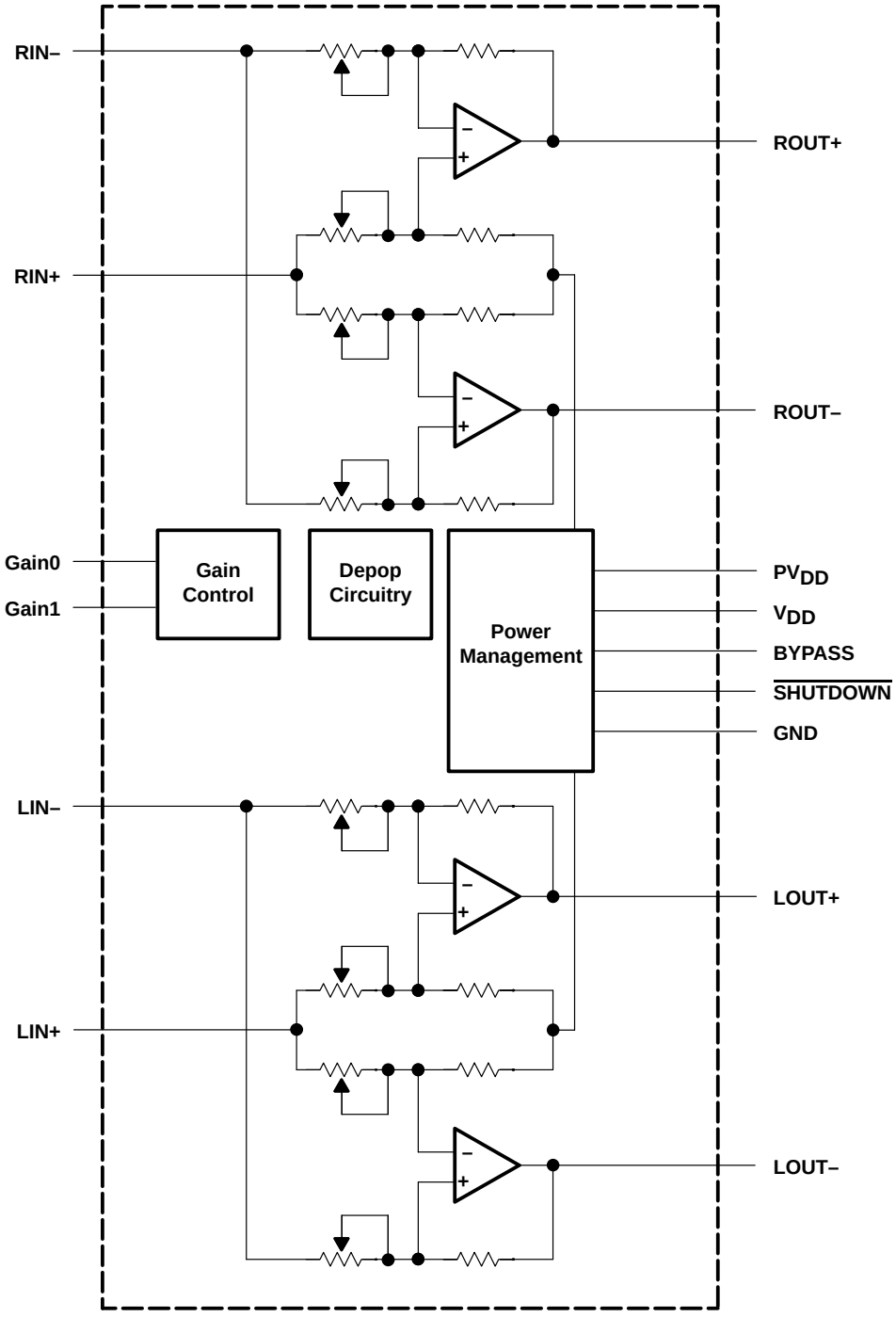


NC – No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	10	—	Tap to voltage divider for internal midsupply bias generator
GAIN0	2	I	Bit 0 of gain select
GAIN1	3	I	Bit 1 of gain select
GND	1, 11, 13, 20	—	Ground
LIN–	5		Left channel negative differential input
LIN+	9	I	Left channel positive differential input
LOUT–	8	O	Left channel negative output
LOUT+	4	O	Left channel positive output
NC	12	—	No connection
PV_{DD}	6, 15	I	Supply voltage terminal
ROUT–	14	O	Right channel negative output
ROUT+	18	O	Right channel positive output
RIN–	17	I	Right channel negative differential input
RIN+	7	I	Right channel positive differential input
$\overline{\text{SHUTDOWN}}$	19	I	Places IC in shutdown mode when held low
V_{DD}	16	I	Supply voltage terminal

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ See the Texas Instruments document, *PowerPAD™ Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD™* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$		0.8	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = –2 V/V			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.5 V to 5.5 V		77		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			1	µA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current	$\overline{\text{SHUTDOWN}}$ = 2 V		6	10	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0.8 V		150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 15 kHz		0.75%		
B_{OM}	Maximum output power bandwidth	THD = 5%		>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF		–68		dB
SNR	Signal-to-noise ratio			105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz, No filtering		16		μV_{RMS}
				–96		dBV
Z_I	Input impedance			See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–6, 9–11, 14–16,
		vs Frequency	2, 3, 7, 8, 12, 13
V_n	Output noise voltage	vs Bandwidth	17
	Supply ripple rejection ratio	vs Frequency	18
	Crosstalk	vs Frequency	19
	Shutdown attenuation	vs Frequency	20
SNR	Signal-to-noise ratio	vs Frequency	21
	Closed loop response		22–24
P_O	Output power	vs Load resistance	25
P_D	Power dissipation	vs Output power	26
		vs Ambient temperature	27

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

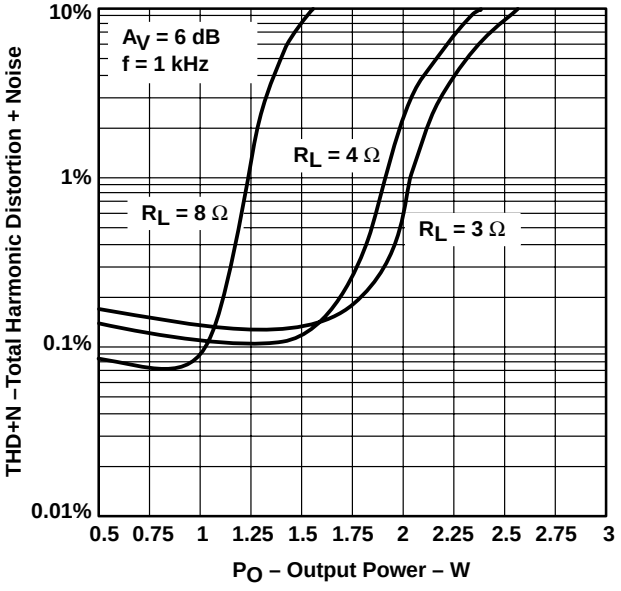


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

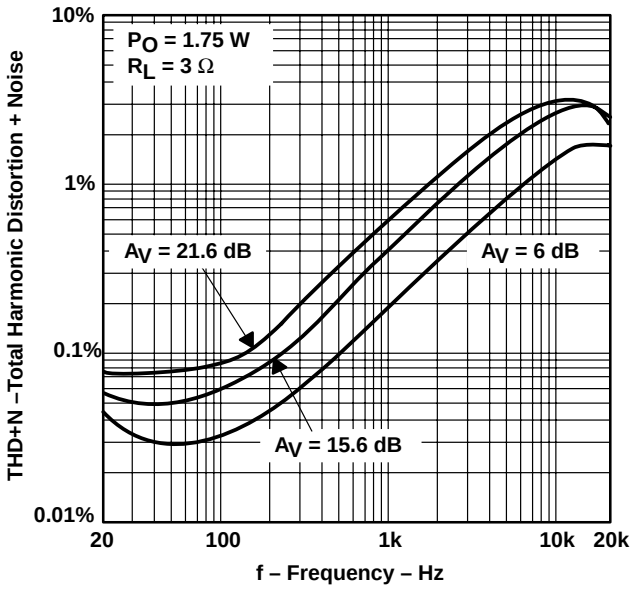


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

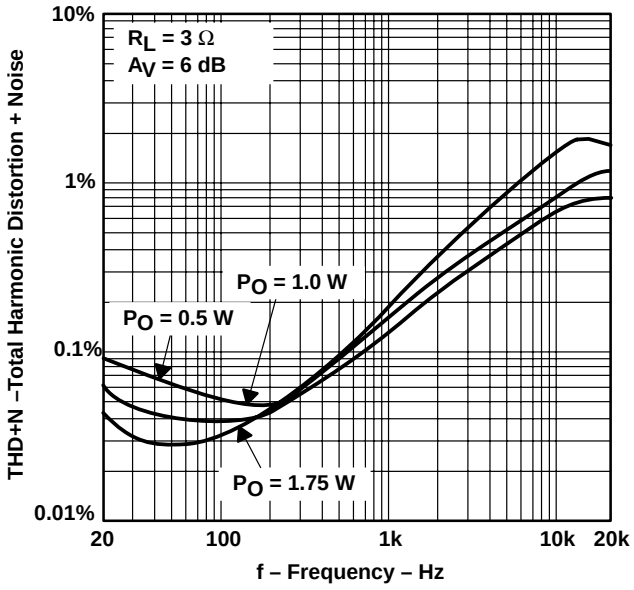


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

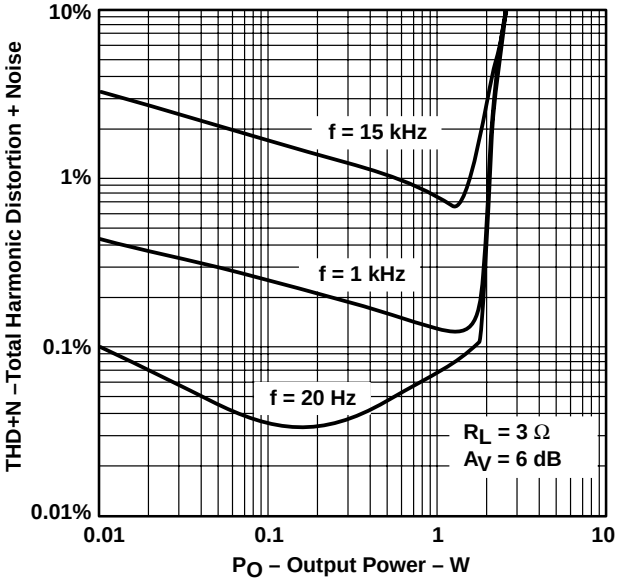


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

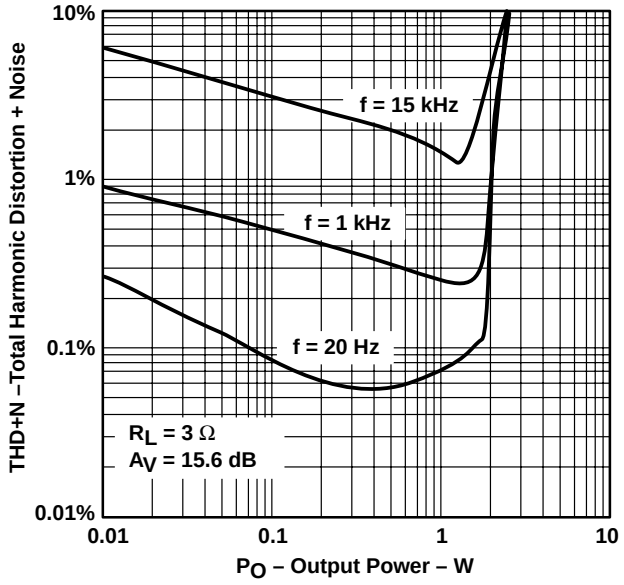


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

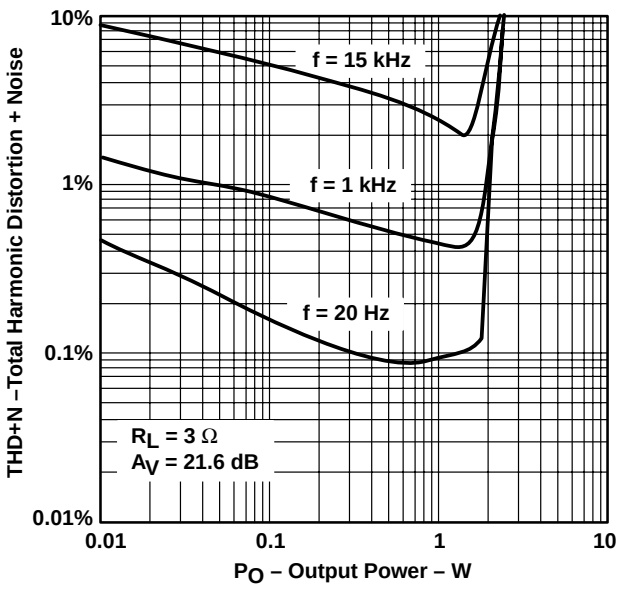


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

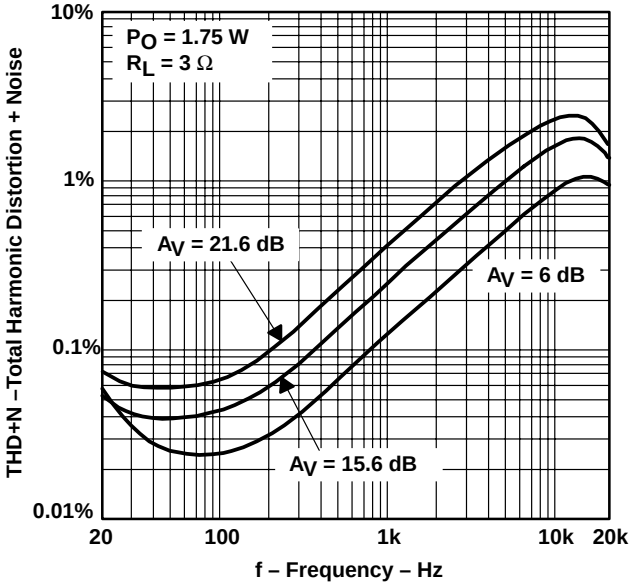


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

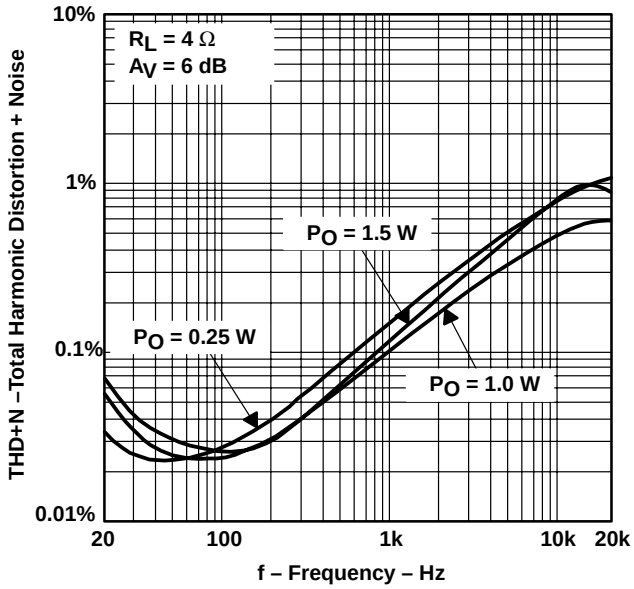


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

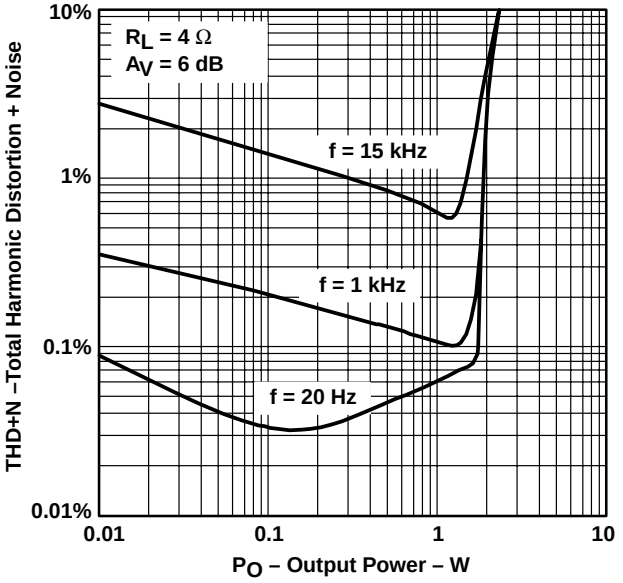


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

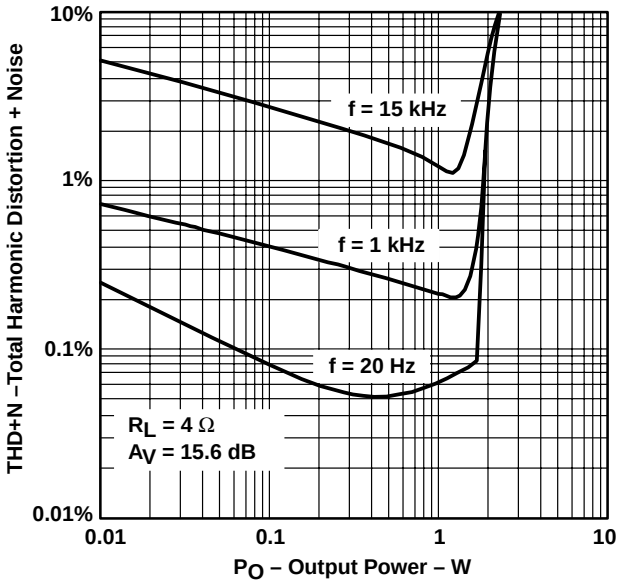


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

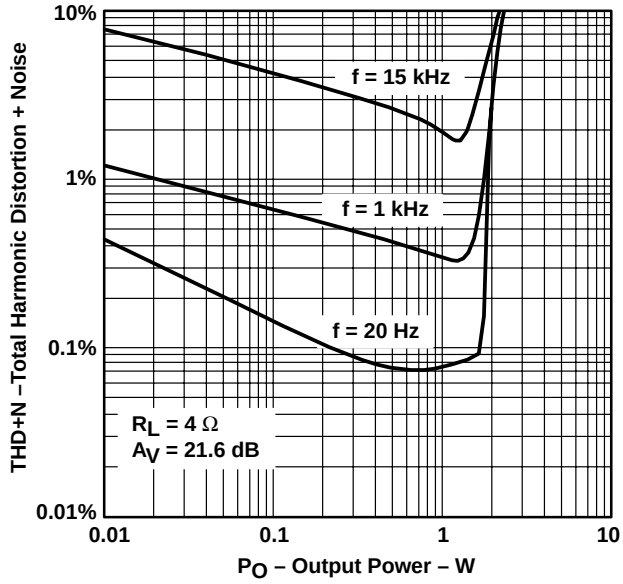


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

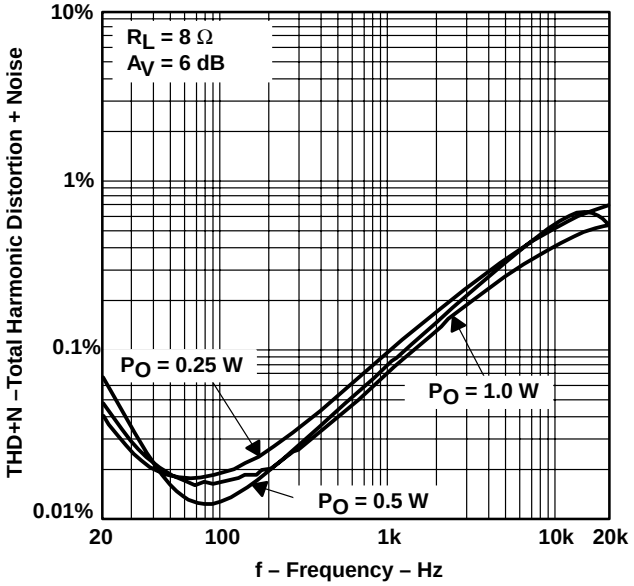


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

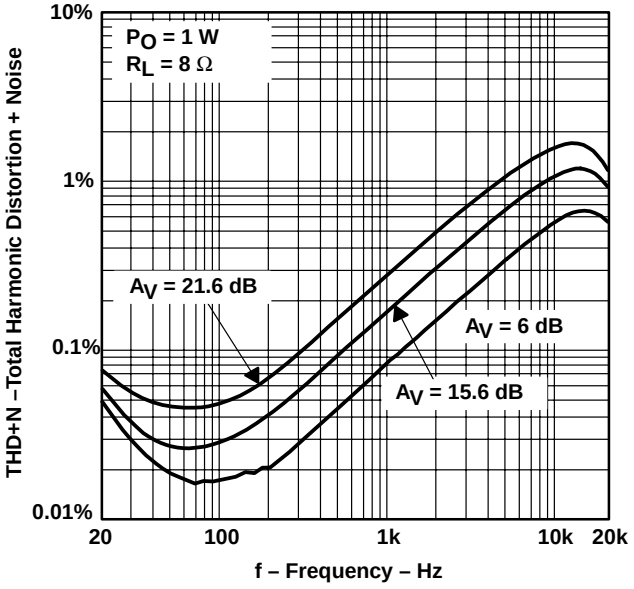


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

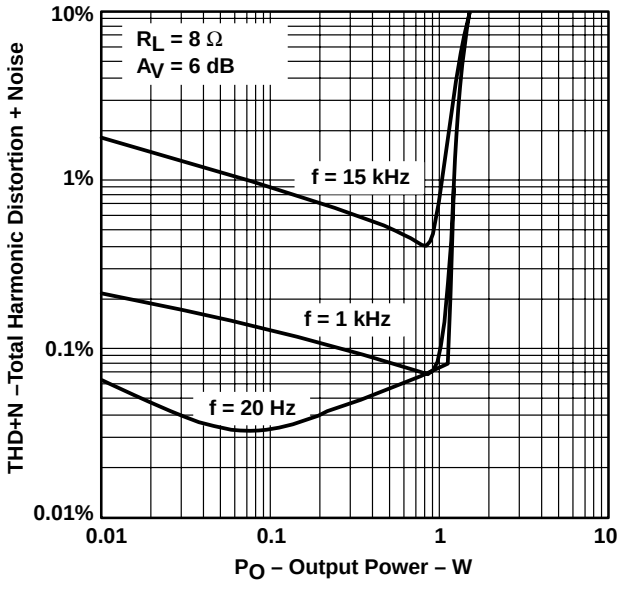


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

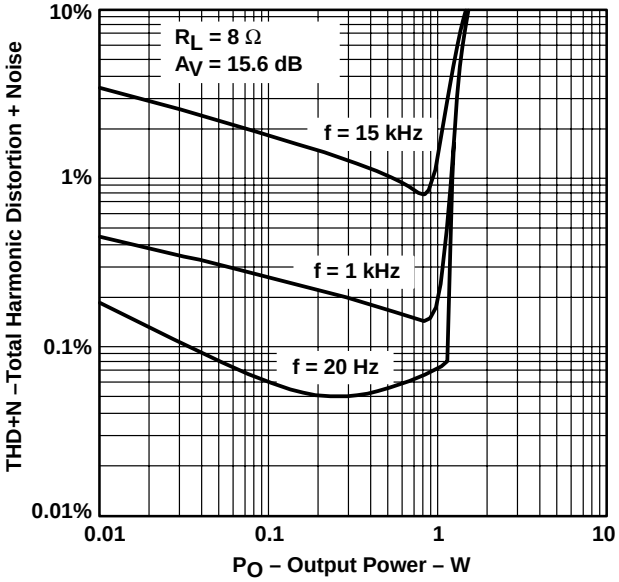


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

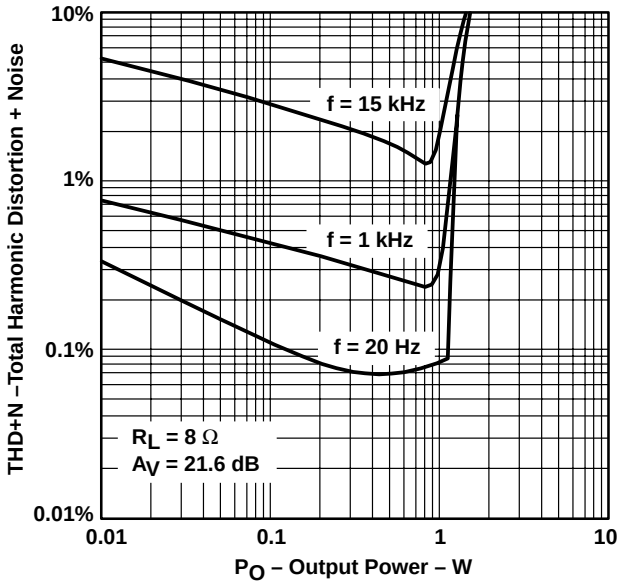


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

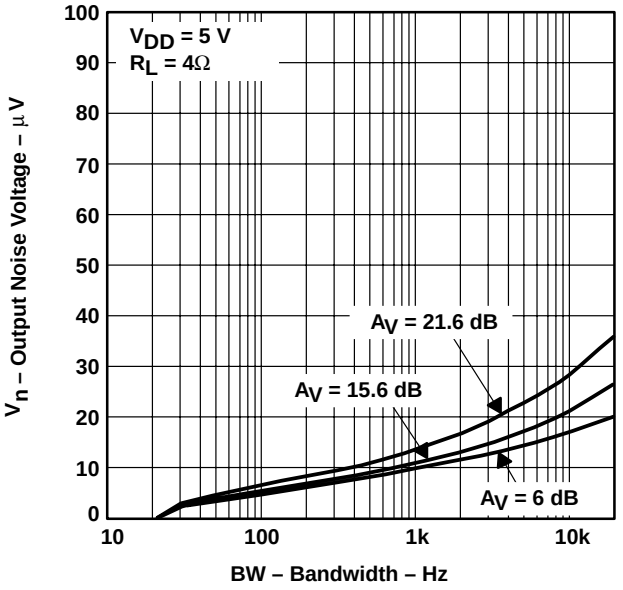


Figure 17

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

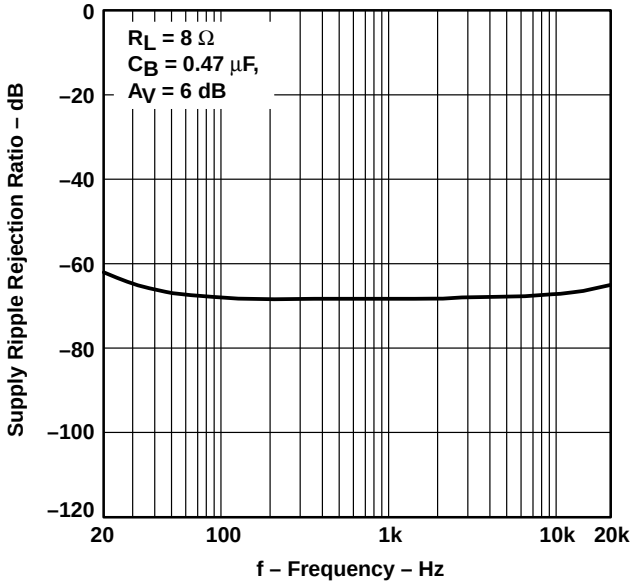


Figure 18

CROSSTALK
vs
FREQUENCY

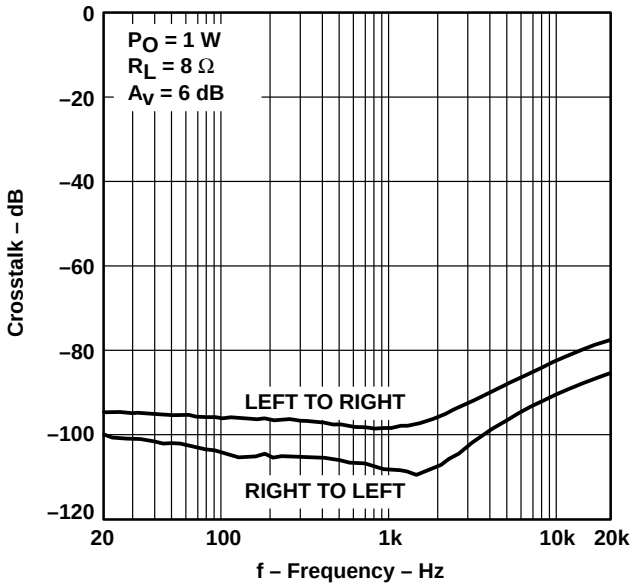


Figure 19

SHUTDOWN ATTENUATION
vs
FREQUENCY

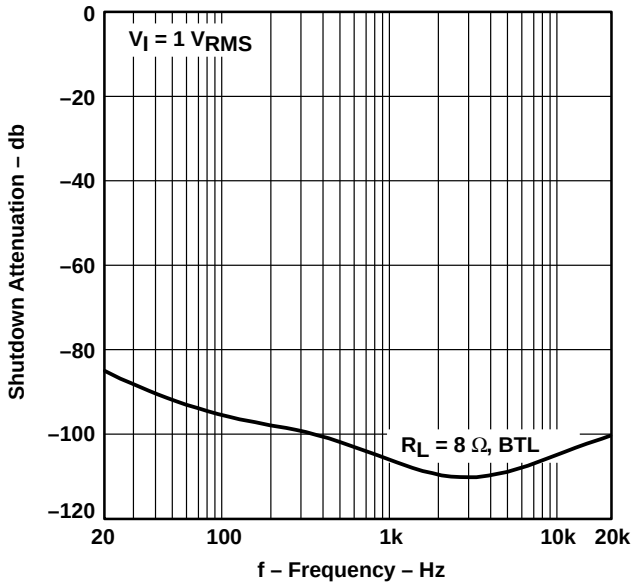


Figure 20

TYPICAL CHARACTERISTICS

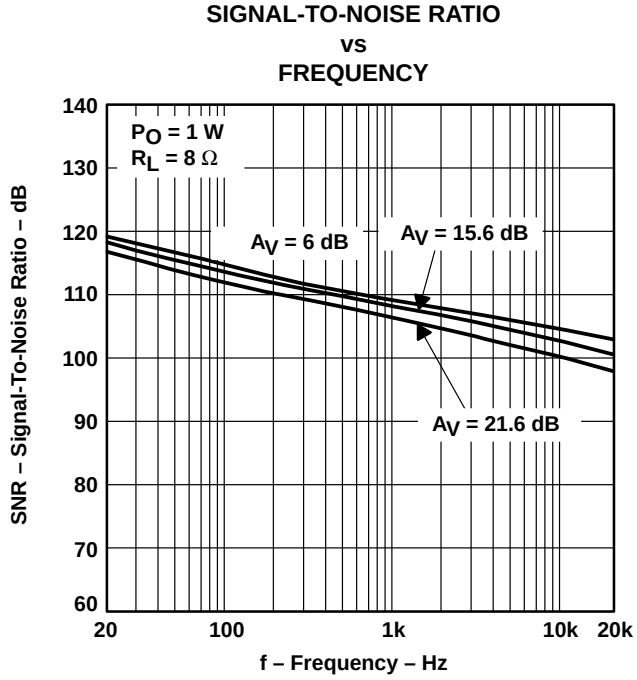


Figure 21

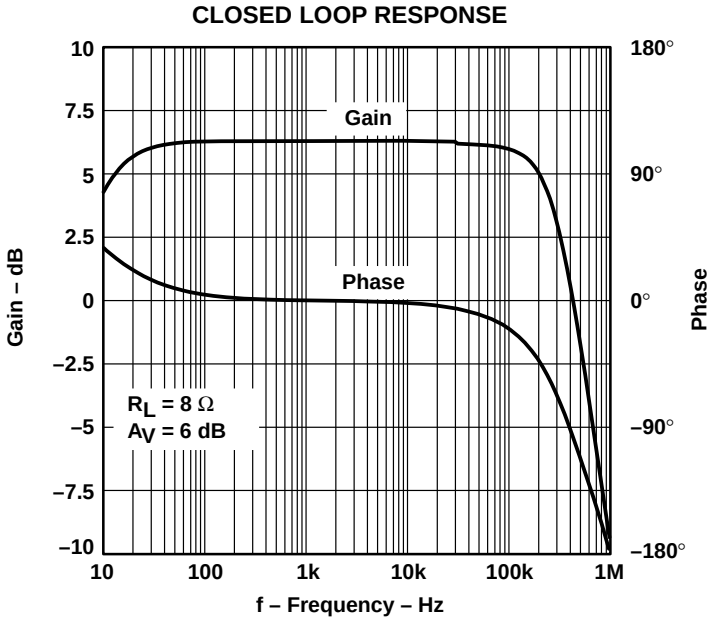


Figure 22

TYPICAL CHARACTERISTICS

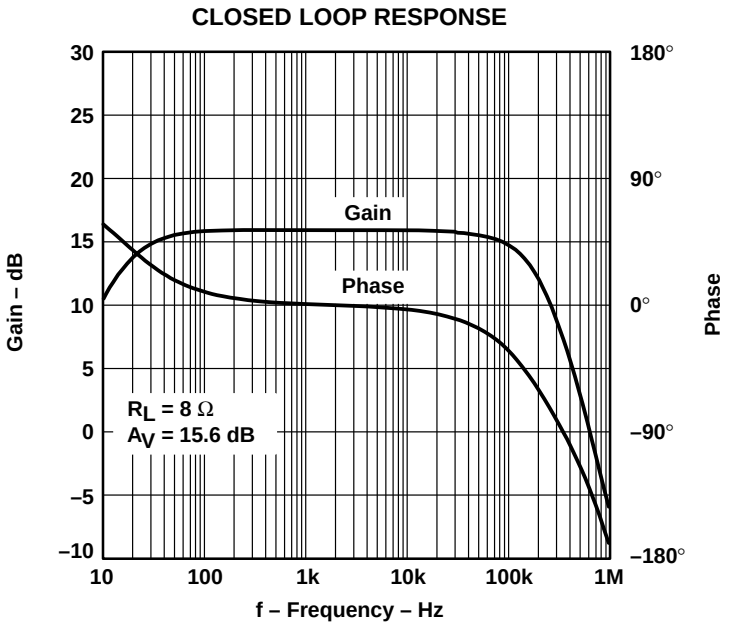


Figure 23

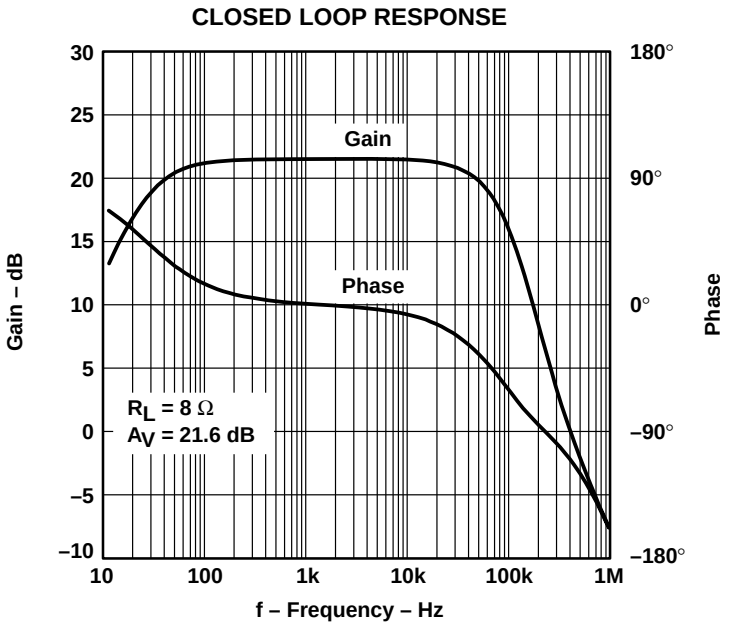


Figure 24

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

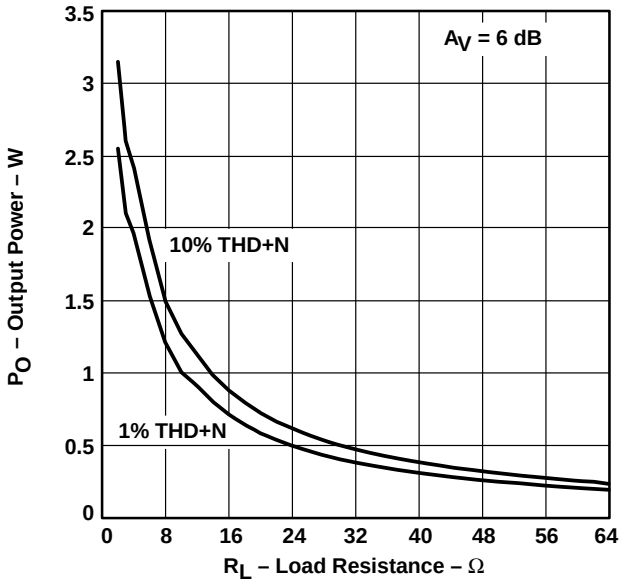


Figure 25

POWER DISSIPATION vs OUTPUT POWER

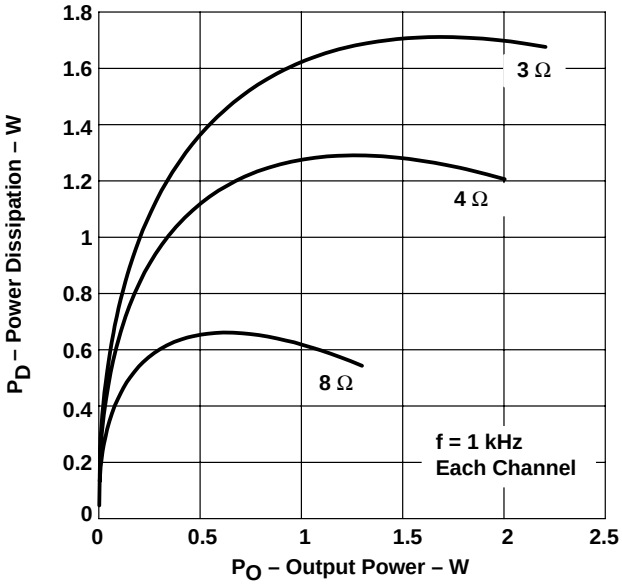


Figure 26

POWER DISSIPATION vs AMBIENT TEMPERATURE

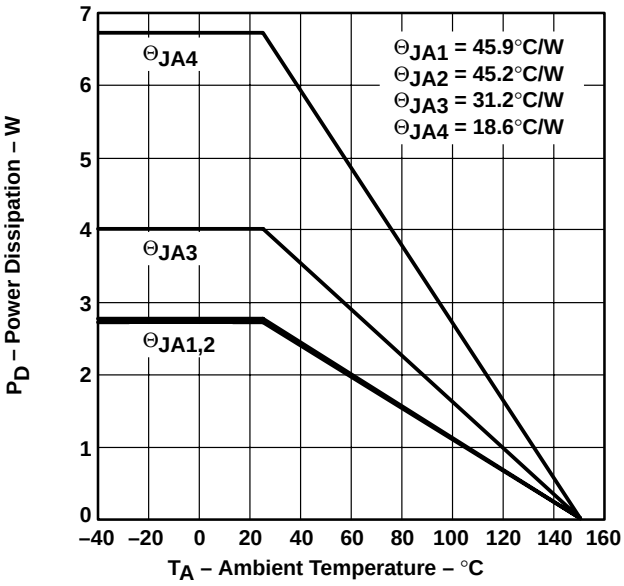


Figure 27

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 28) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface-mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD™ package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD™ package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

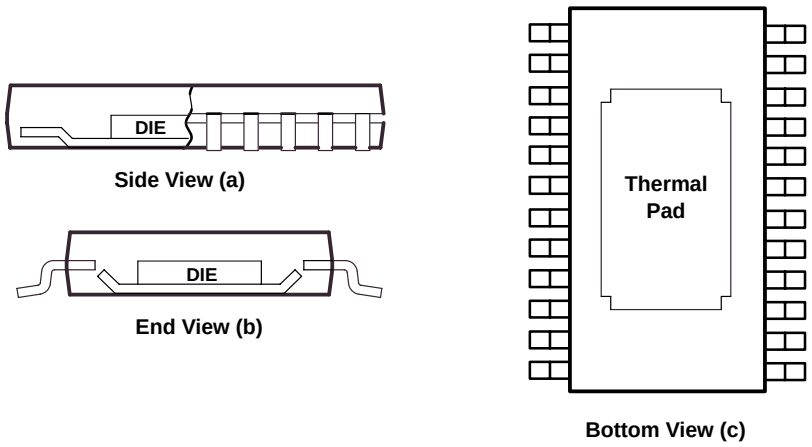
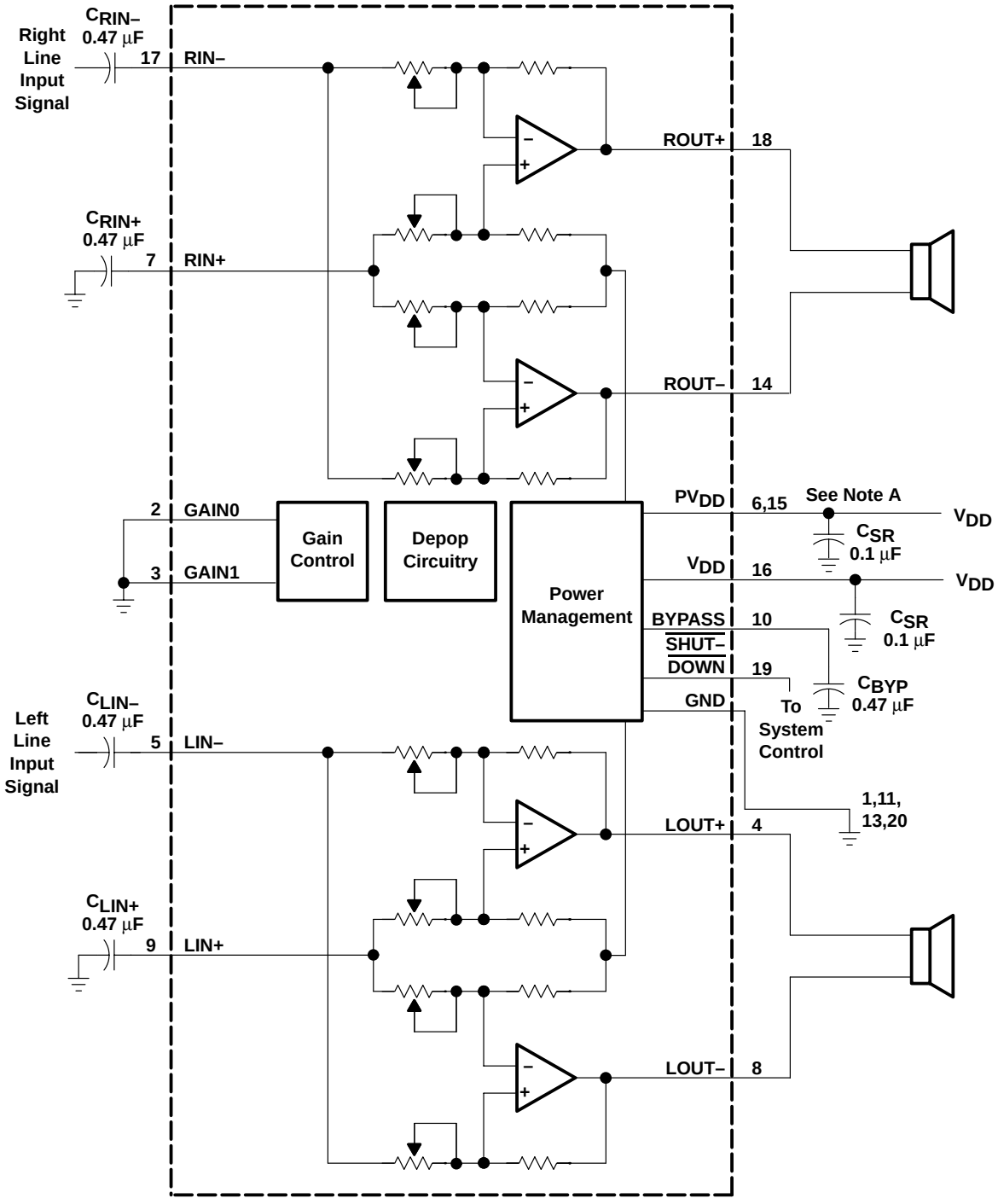


Figure 28. Views of Thermally Enhanced PWP Package

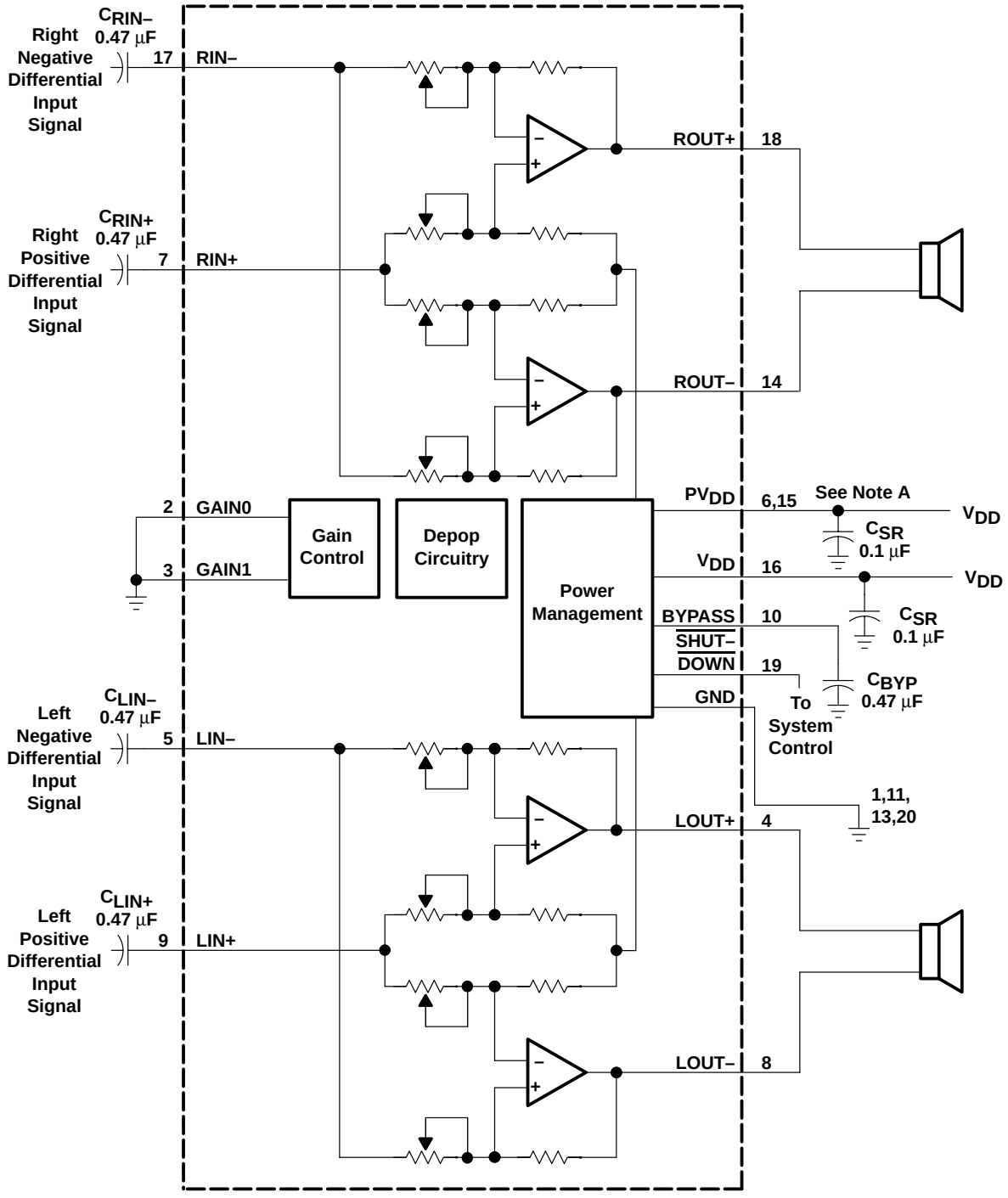
APPLICATION INFORMATION



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 29. Typical TPA6017A2 Application Circuit Using Single-Ended Inputs

APPLICATION INFORMATION



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA6017A2 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

shutdown modes

The TPA6017A2 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA6017A2 is set by two input terminals, GAIN0 and GAIN1.

Table 1. Gain Settings

GAIN0	GAIN1	$A_{V(inv)}$	INPUT IMPEDANCE
0	0	6 dB	90 kΩ
0	1	10 dB	70 kΩ
1	0	15.6 dB	45 kΩ
1	1	21.6 dB	25 kΩ

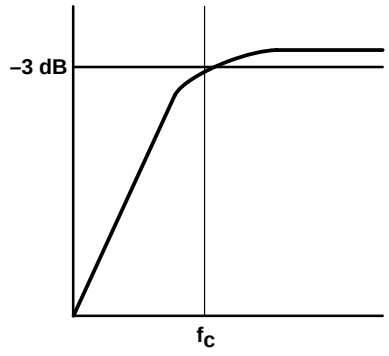
The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA6017A2. At the higher gain settings, the input impedance could increase to as high as 115 kΩ. The typical input impedance at each gain setting is given in Table 1.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 1.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (1)$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 10 kΩ, which is the absolute minimum input impedance of the TPA6017A2, and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 2.

$$C_I = \frac{1}{2\pi Z_I f_C} \quad (2)$$

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA60172A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor C_{BYP}, the most critical capacitor serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 31 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6017A2 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 3).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (3)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

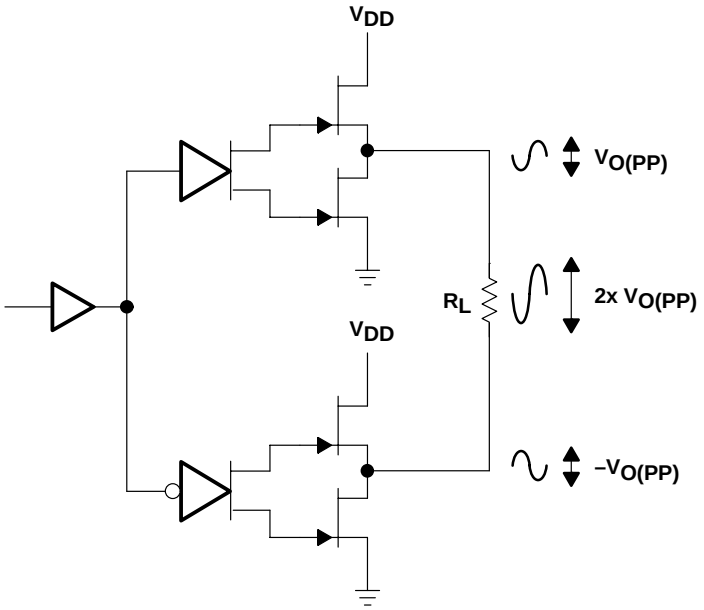


Figure 31. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 32. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 4.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (4)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

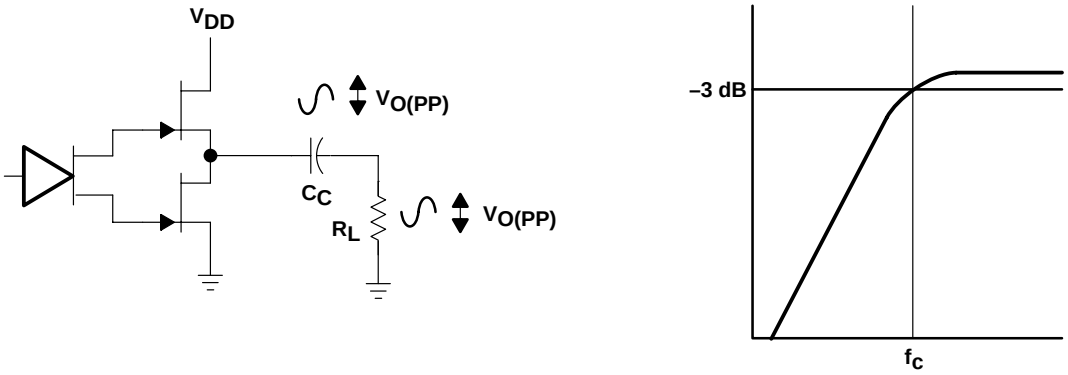


Figure 32. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

BTL amplifier efficiency

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop, multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 33).

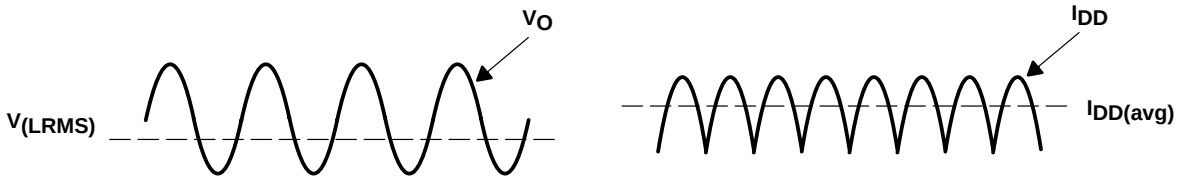


Figure 33. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{5}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\,V_{DD}\,V_P}{\pi\,R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\,R_L}}{\frac{2\,V_{DD}\,V_P}{\pi\,R_L}} = \frac{\pi\,V_P}{4\,V_{DD}}$$

Where:

$$V_P = \sqrt{2\,P_L\,R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\sqrt{2\,P_L\,R_L}}{4\,V_{DD}} \tag{6}$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Table 2. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 6, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6017A2 data sheet, one can see that when the TPA6017A2 is operating from a 5-V supply into a 3-Ω speaker 4-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\text{ W}}{1\text{ W}} = 6\text{ dB} \quad (7)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 18 dB = –12 dB (18 dB crest factor)
6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (8)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (12 dB crest factor)
= 500 mW (9 dB crest factor)
= 1000 mW (6 dB crest factor)
= 2000 mW (3 dB crest factor)

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA60172A2 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA6017A2 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 4. TPA6017A2 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, $P_{D(max)}$, is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating $P_{D(max)}$ may be used for an 8-Ω application:

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (9)$$

However, in the case of a 3-Ω load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (10)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA60172A2 is 150°C. The internal dissipation figures are taken from Figure 26.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (11)$$

$$= 150 - 45(0.6 \times 2) = 96°\text{C (18 dB crest factor)}$$

NOTE:

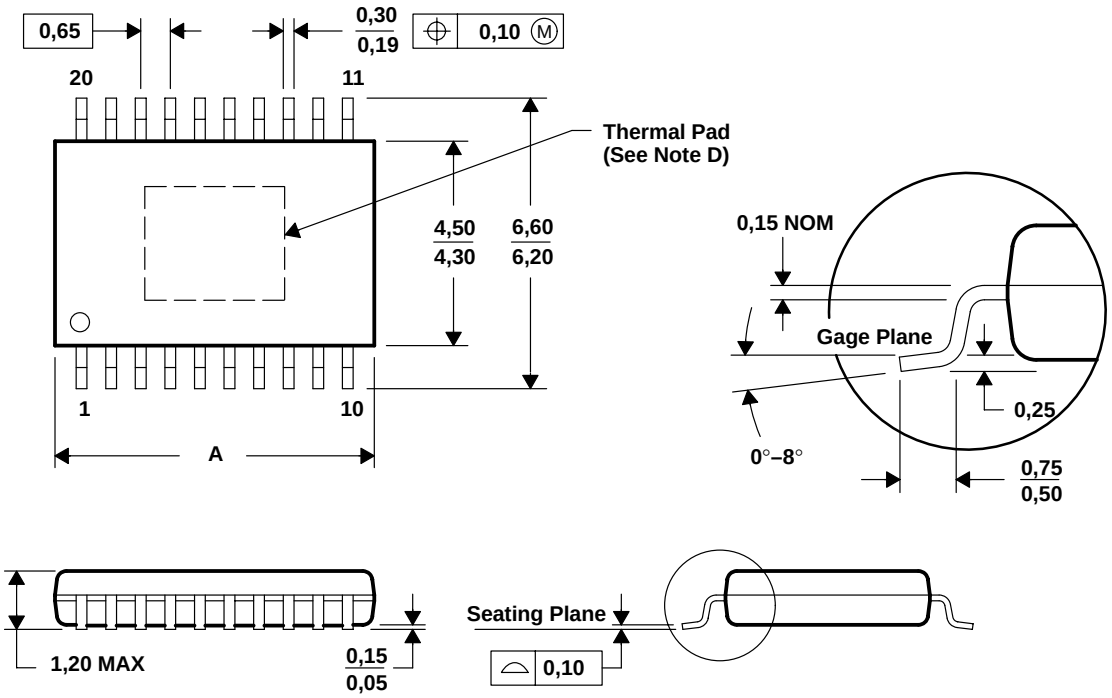
Internal dissipation of 0.6 W is estimated for a 2-W system with 18 dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA60172A2 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and terminals 1, 12, 13, and 24. The dimensions of the thermal pad are 2.40 mm × 4.70 mm (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPA6017A2PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6017A2PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA6017A2PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

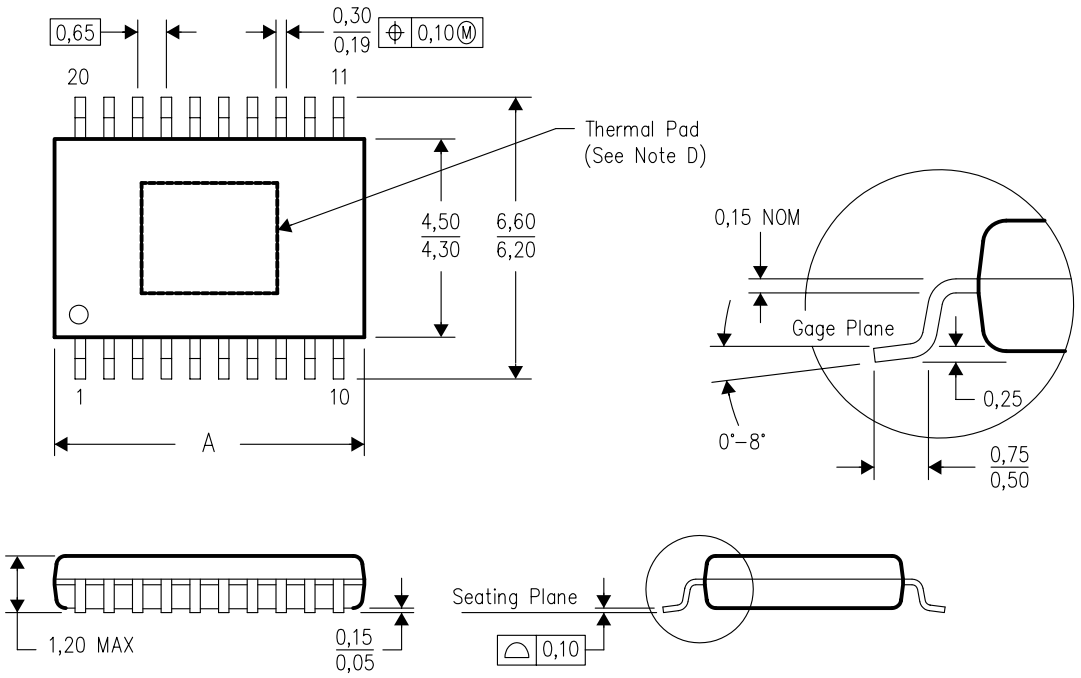
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

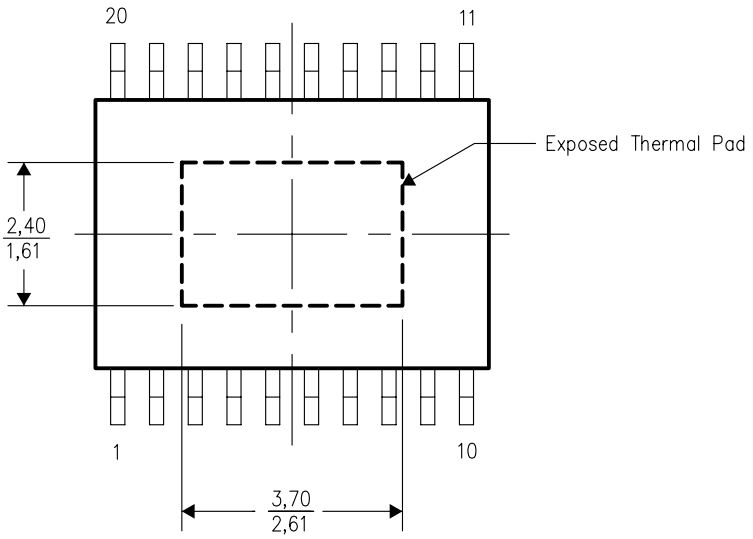
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

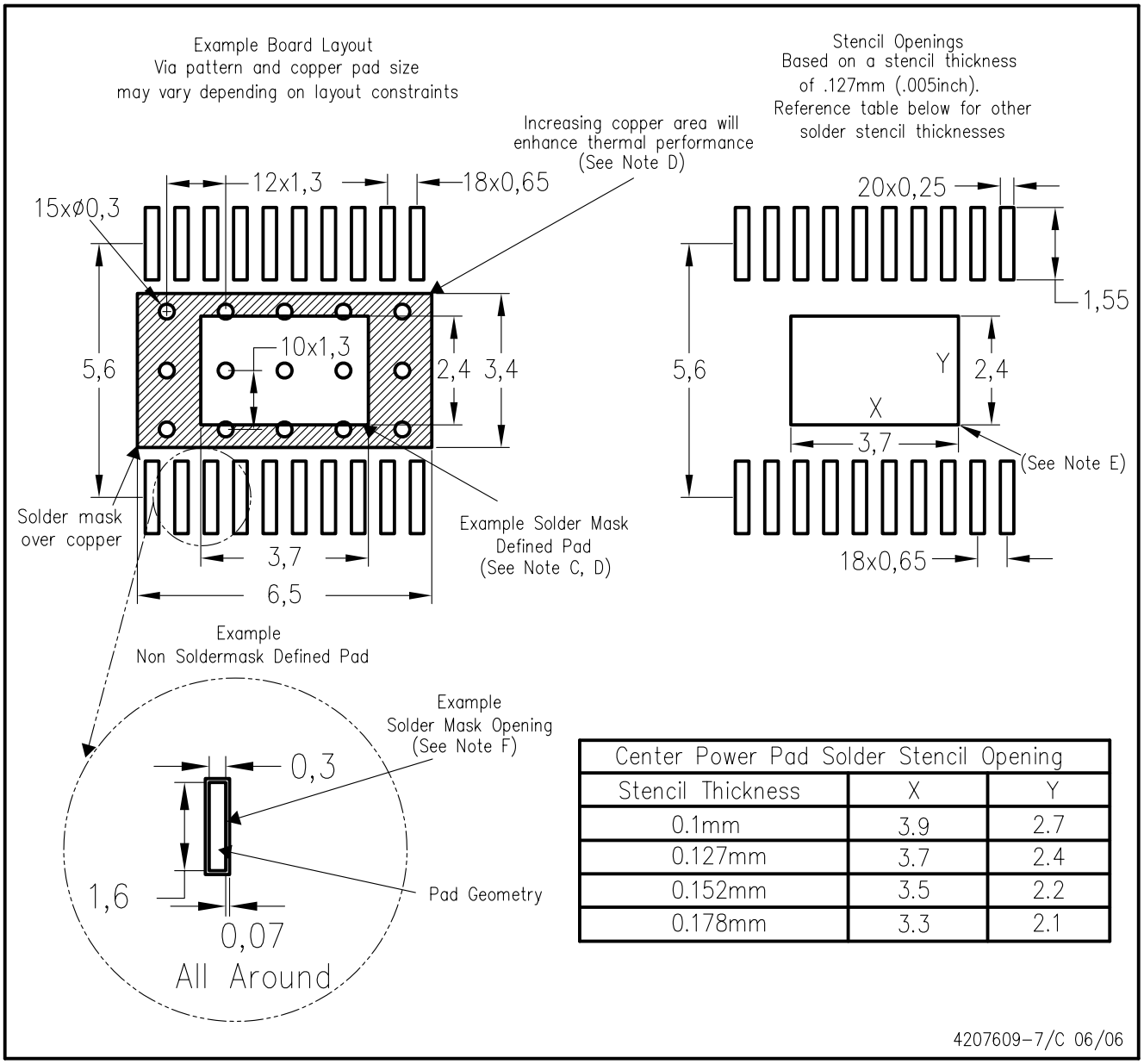


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–7/C 06/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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