STEREO DIGITAL AUDIO LIP-SYNC DELAY WITH I²C CONTROL

FEATURES

- **Digital Audio Formats: 16-24-bit I²S, Right-Justified, Left-Justified**
- **I²C Bus Controlled**
- **Single Serial Input Port**
- **Delay Time: 170 ms/ch at fs = 48 kHz**
- **Delay Resolution: One Sample**
- **Delay Memory Cleared on Power-Up or After Delay Changes**
  - **Eliminates Erroneous Data From Being Output**
- **3.3 V Operation With 5 V Tolerant I/O and I²C Control**
- **Supports Audio Bit Clock Rates of 32 to 64 fs with fs = 32 kHz–192 kHz**
- **No external crystal or oscillator required**
  - **All Internal Clocks Generated From the Audio Clock**
- **Surface Mount 4mm × 4mm, 16-pin QFN Package**

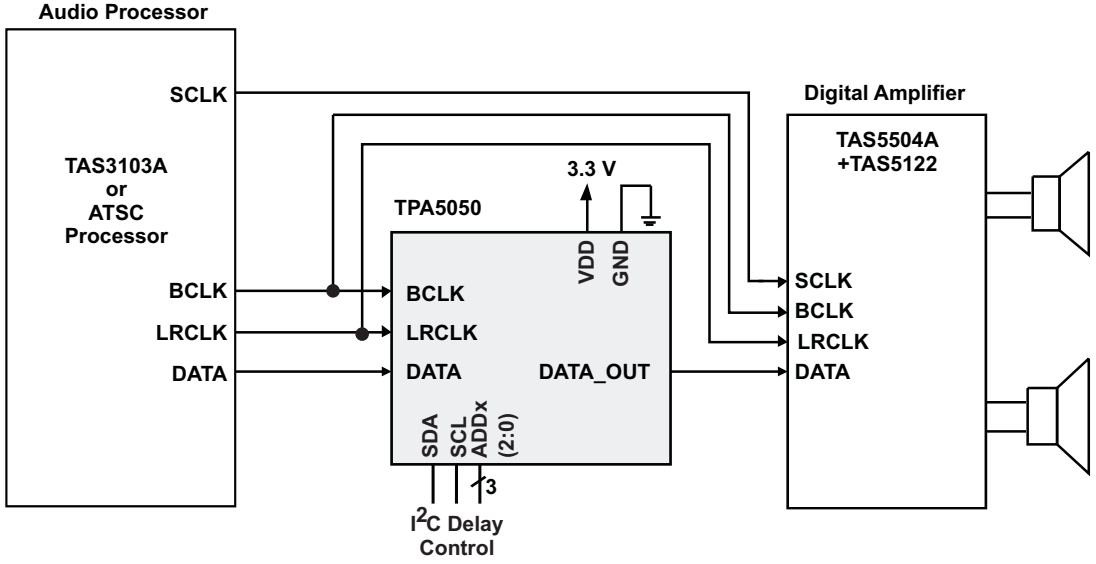
APPLICATIONS

- **High Definition TV Lip-Sync Delay**
- **Flat Panel TV Lip-Sync Delay**
- **Home Theater Rear-Channel Effects**
- **Wireless Speaker Front-Channel Synchronization**

DESCRIPTION

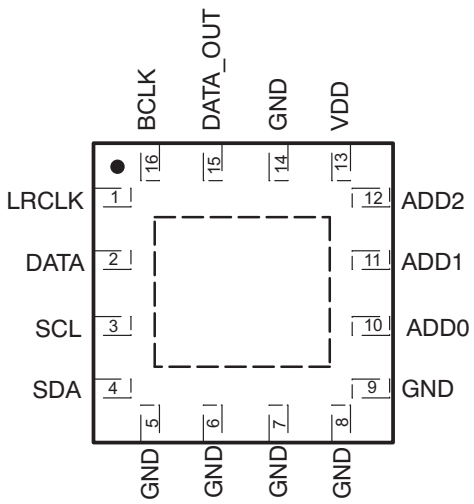
The TPA5050 accepts a single serial audio input, buffers the data for a selectable period of time, and outputs the delayed audio data on a single serial output. One device allows delay of up to 170 ms/ch (fs = 48 kHz) to synchronize the audio stream to the video stream in systems with complex video processing algorithms. If more delay is needed, the devices can be connected in series.

SIMPLIFIED APPLICATION DIAGRAM



PIN DESCRIPTIONS

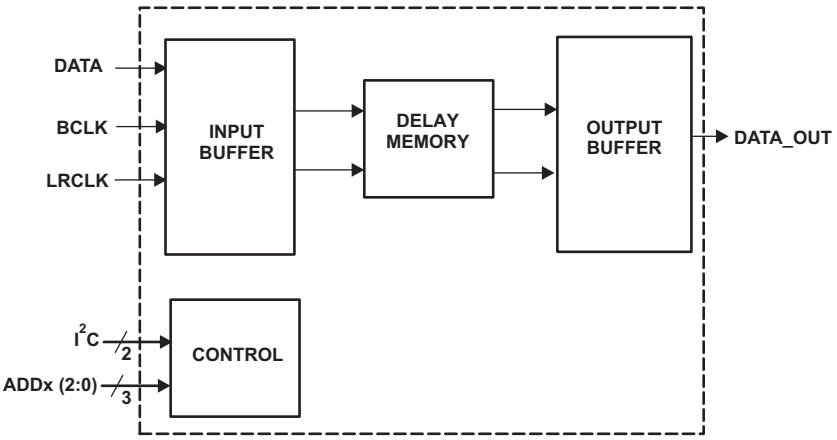
RSA (QFN) PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADD0	10	I	I^2C address select pin – LSB
ADD1	11	I	I^2C address select pin
ADD2	12	I	I^2C address select pin – MSB
BCLK	16	I	Audio data bit clock input for serial input. 5V tolerant input.
DATA	2	I	Audio serial data input for serial input. 5V tolerant input.
DATA_OUT	15	O	Delayed audio serial data output.
GND	5–9, 14	P	Ground – All ground terminals must be tied to GND for proper operation
LRCLK	1	I	Left and Right serial audio sampling rate clock (fs). 5V tolerant input.
SCL	3	I	I^2C communication bus clock input. 5V tolerant input.
SDA	4	I/O	I^2C communication bus data input. 5V tolerant input.
VDD	13	P	Power supply interface.
Thermal Pad		-	Connect to ground. Must be soldered down in all applications to properly secure device on the PCB.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

			VALUE	UNIT
V_{DD}	Supply voltage		–0.3 to 3.6	V
V_I	Input voltage	DATA, LRCLK, BCLK, SCL, SDA	–0.3 to 5.5	V
		ADD[2:0]	–0.3 to VDD+0.3	
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 125	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RSA	2.5 W	25mW/°C	1.375 W	1.0 W

(1) This data was taken using 1 oz trace and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI Technical Briefs SCBA017D and SLUA271 for more information about using the QFN thermal pad.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	3	3.6	V
V_{IH}	High-level input voltage	DATA, LRCLK, BCLK, SCL, SDA, ADD[2:0]	2		V
V_{IL}	Low-level input voltage	DATA, LRCLK, BCLK, SCL, SDA, ADD[2:0]		0.8	V
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 3.3 V, fs = 48 kHz, BCLK = 32 fs		1.5	3	mA
I_{OH}	High-level output current	DATA_OUT = 2.6 V	7		13	mA
I_{OL}	Low-level output current	DATA_OUT = 0.4 V	7		13	mA
I_{IH}	High-level input current	DATA, LRCLK, BCLK, SCL, SDA, Vi = 5.5V, VDD = 3V			20	µ A
		ADD[2:0], Vi = 3.6V, VDD = 3.6V			5	
I_{IL}	Low-level input current	DATA, LRCLK, BCLK, SCL, SDA, ADD[2:0], Vi = 0V, VDD = 3.6V			1	µA

TIMING CHARACTERISTICS(1)(2)

For I^2C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6			µs
$t_{w(L)}$	Pulse duration, SCL low		1.3			µs
t_{su1}	Setup time, SDA to SCL		100			ns
t_{h1}	Hold time, SCL to SDA		10			ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3			µs
t_{su2}	Setup time, SCL to start condition		0.6			µs
t_{h2}	Hold time, start condition to SCL		0.6			µs
t_{su3}	Setup time, SCL to stop condition		0.6			µs

(1) $V_{Pull\text{-}up} = V_{DD}$
(2) A pull-up resistor ≤2 kΩ is required for a 5 V I^2C bus voltage.

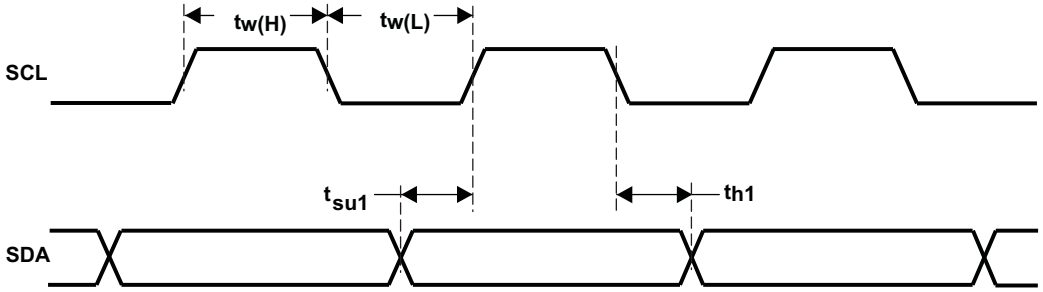


Figure 1. SCL and SDA Timing

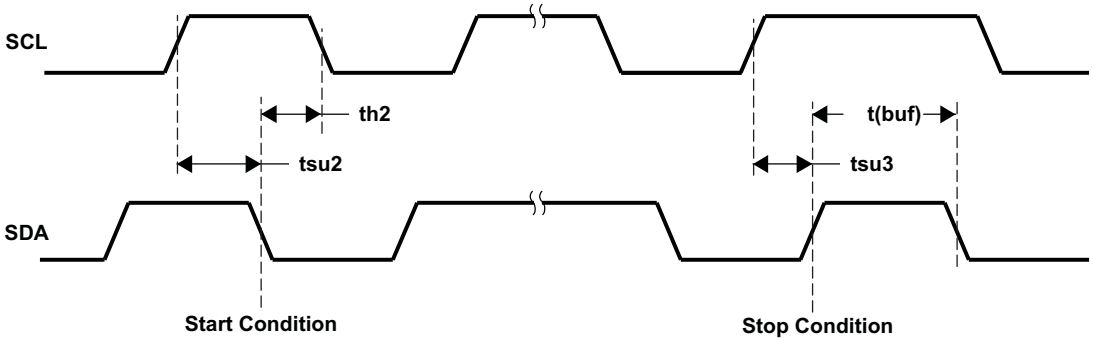


Figure 2. Start and Stop Conditions Timing

Serial Audio Input Ports

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, BCLK 32 × fs, 48 × fs, 64 × fs		1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to BCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from BCLK rising edge		10			ns
t_{su2}	Setup time, DATA to BCLK rising edge		10			ns
t_{h2}	Hold time, DATA from BCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	BCLK duty cycle			50%		
	LRCLK duty cycle			50%		
	BCLK rising edges between LRCLK rising edges	LRCLK duty cycle = 50%	32		64	BCLK edges

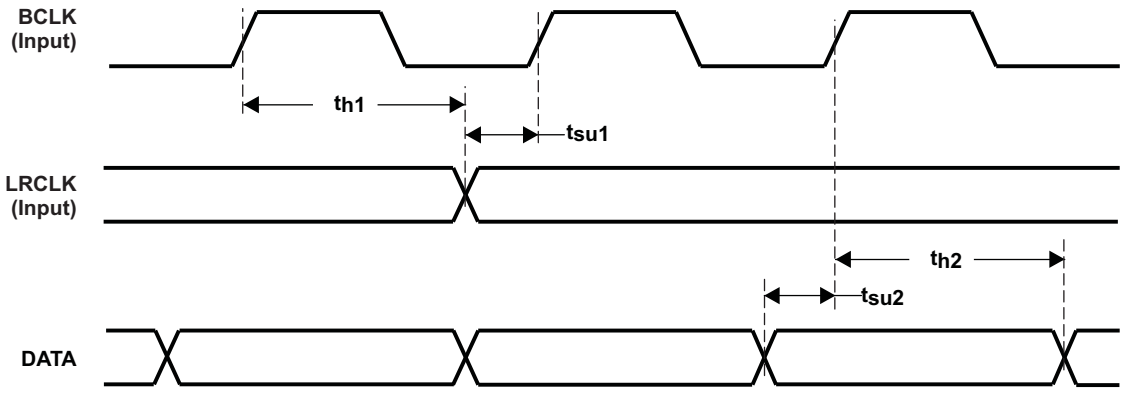


Figure 3. Serial Data Interface Timing

APPLICATION INFORMATION

AUDIO SERIAL INTERFACE

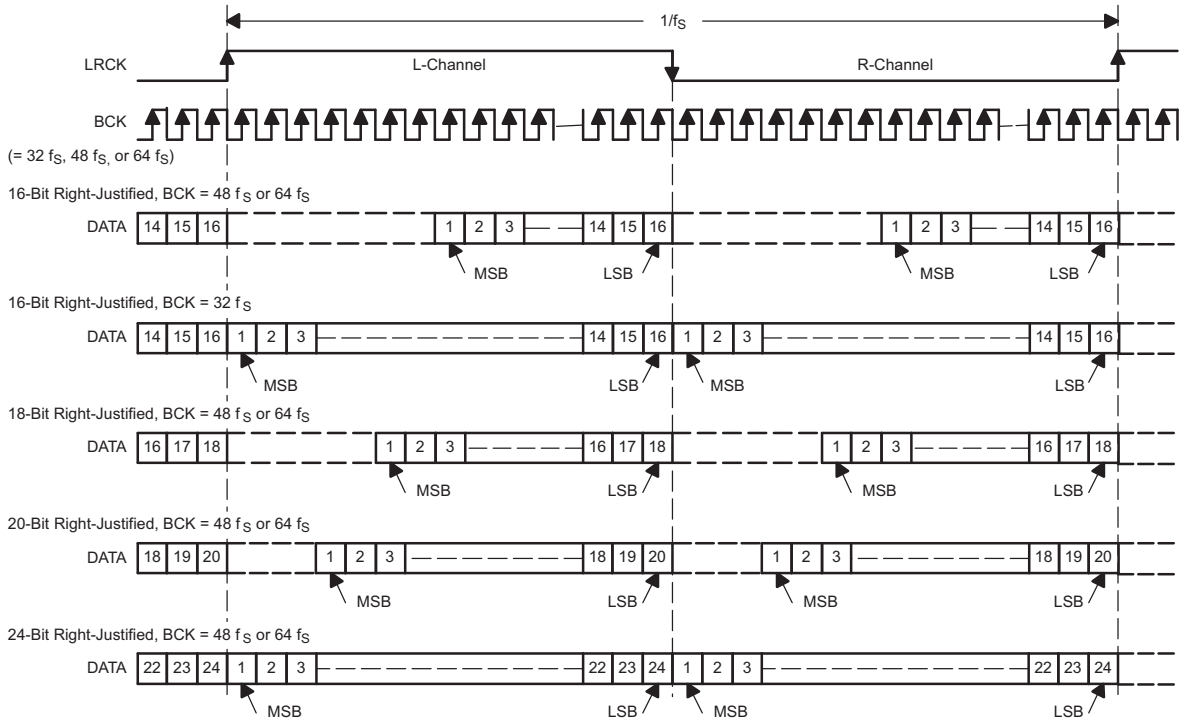
The audio serial interface for the TPA5050 consists of a 3-wire synchronous serial port. It includes LRCLK, BCLK, and DATA. BCLK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the TPA5050 on the rising edge of BCLK. LRCLK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface. LRCLK is operated at the sampling frequency, fs. BCLK can be operated at 32 to 64 times the sampling frequency for right-justified, left-justified, and I^2S formats. A system clock is not necessary for the operation of the TPA5050.

AUDIO DATA FORMATS AND TIMING

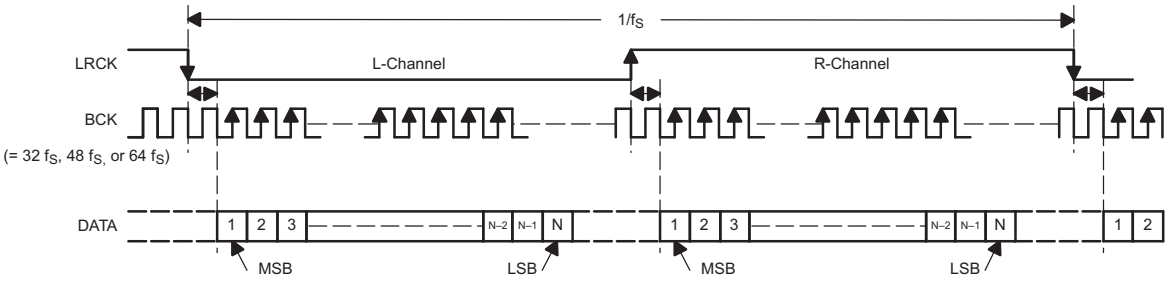
The TPA5050 supports industry-standard audio data formats, including right-justified, I^2S, and left-justified. The data formats are shown in Figure 4. Data formats are selected using the I^2C interface and register map (see Table 1).

APPLICATION INFORMATION (continued)

(1) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

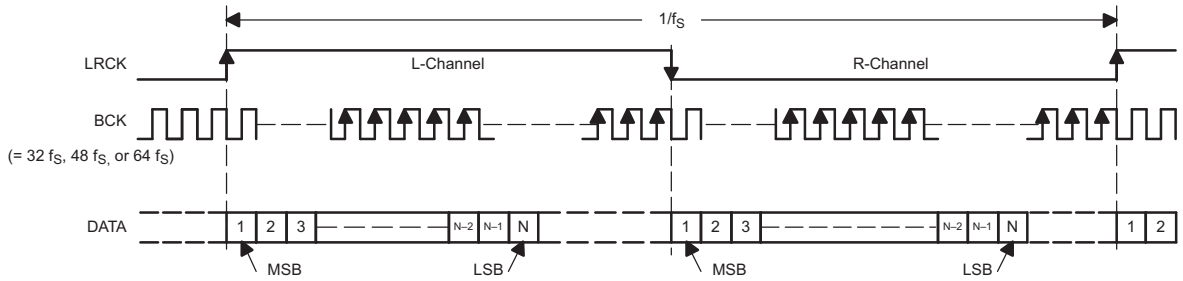


Figure 4. Audio Data Formats

APPLICATION INFORMATION (continued)

GENERAL I²C OPERATION

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 5. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TPA5050 holds SDA low during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. When the bus level is 5 V, pull-up resistors between 1 kΩ and 2 kΩ in value must be used.

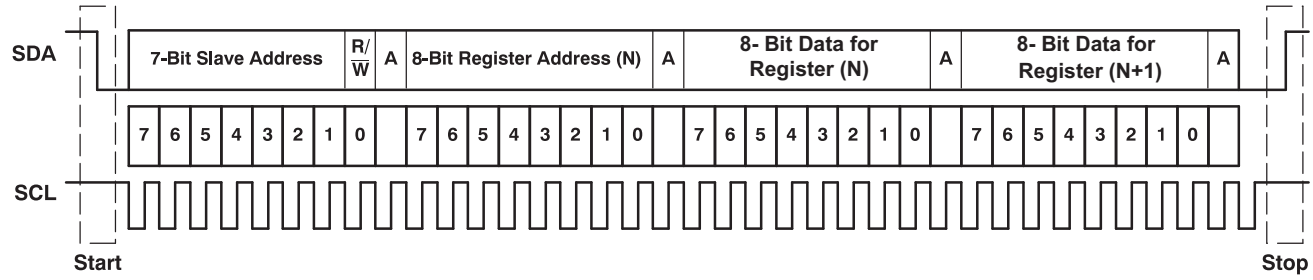


Figure 5. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 5.

The 7-bit address for the TPA5050 is selectable using the 3 address pins (ADD2, ADD1, ADD0). Table 1 lists the 8 possible slave addresses.

Table 1. I²C Slave Address

FIXED ADDRESS (4 MSB bits)	SELECTABLE ADDRESS BITS		
	ADD2	ADD1	ADD0
1101	0	0	0
1101	0	0	1
1101	0	1	0
1101	0	1	1
1101	1	0	0
1101	1	0	1
1101	1	1	0
1101	1	1	1

SINGLE-AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA5050 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TPA5050 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

SINGLE-BYTE WRITE

As shown is Figure 6, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA5050 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA5050 internal memory address being accessed. After receiving the register byte, the TPA5050 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TPA5050 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

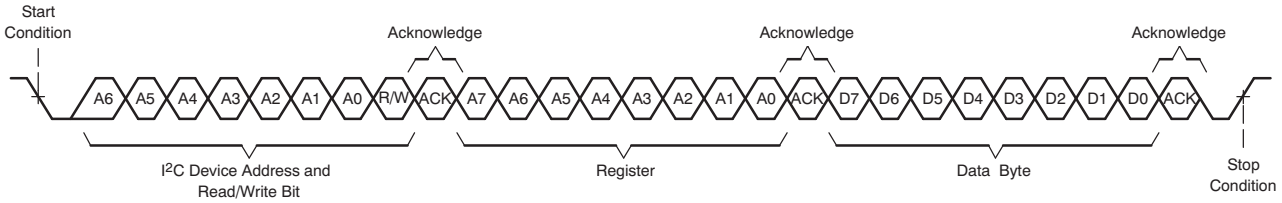


Figure 6. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA5050 as shown in Figure 7. After receiving each data byte, the TPA5050 responds with an acknowledge bit.

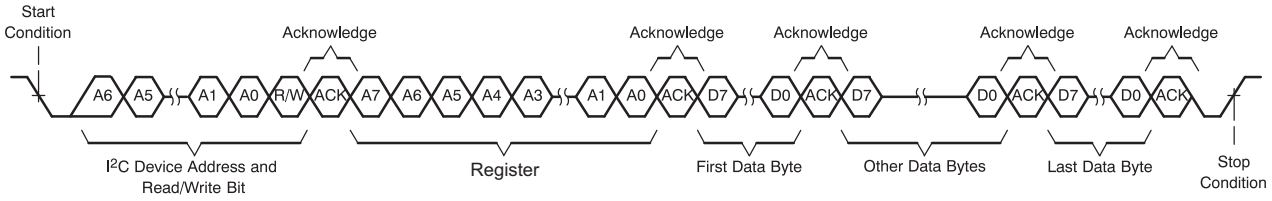


Figure 7. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As shown in Figure 8, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA5050 address and the read/write bit, the TPA5050 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA5050 issues an acknowledge bit. The master device transmits another start condition followed by the TPA5050 address and the read/write bit again. This time the read/write bit is set to 1, indicating a read transfer. Next, the TPA5050 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

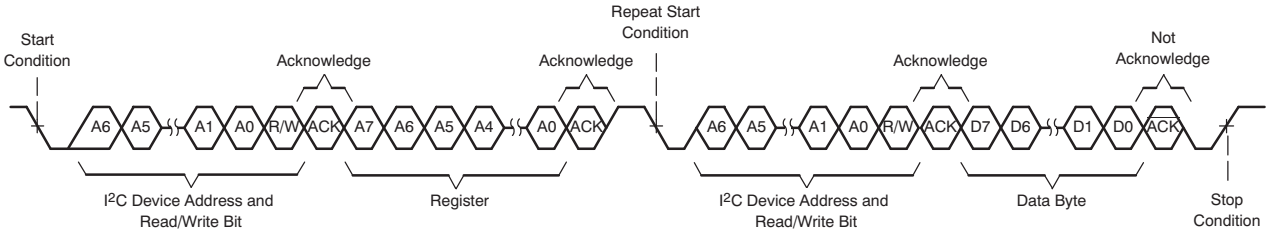


Figure 8. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA5050 to the master device as shown in Figure 9. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

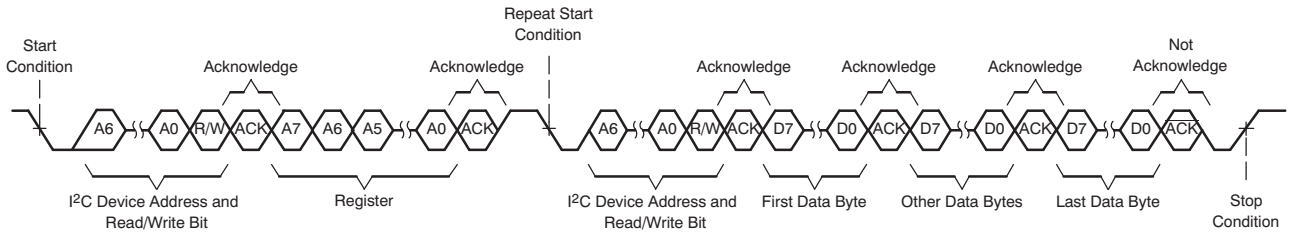


Figure 9. Multiple-Byte Read Transfer

TPA5050 Operation

The following sections describe the registers configurable via I^{2}C commands for the TPA5050.

Only a single decoupling capacitor (0.1 µF–1 µF) is required across VDD and GND. The ADDx terminals can be directly connected to VDD or GND. Table 1 describes the I^{2}C addresses selectable via the ADDx terminals. A schematic implementation of the TPA5050 is shown in Figure 10.

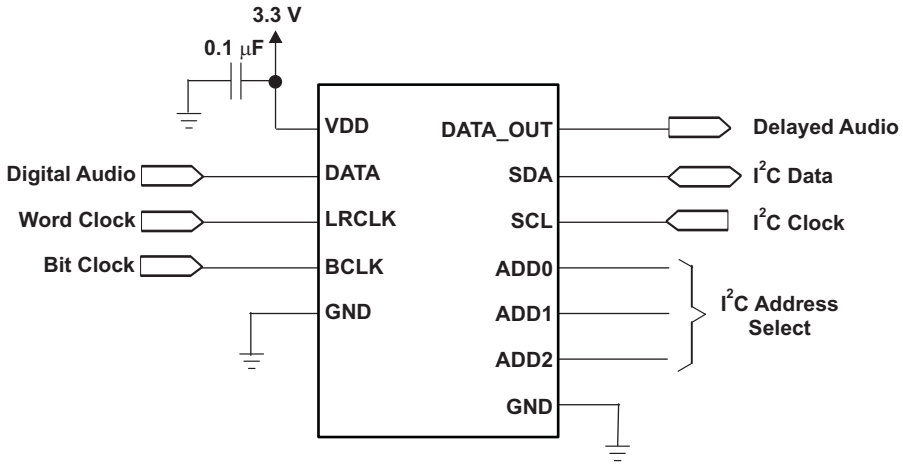


Figure 10. TPA5050 Schematic

SERIAL CONTROL INTERFACE REGISTER SUMMARY

Table 2. Serial Control Register Summary

REGISTER	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x01	Control Register	1	Description shown in subsequent section	00
0x02	Right Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x03	Right Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x04	Left Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x05	Left Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x06	Frame Delay	1	Description shown in subsequent section	00
0x07	RJ Packet Length	1	Description shown in subsequent section	00
0x08	Complete Update	1	Description shown in subsequent section	00

CONTROL REGISTER (0x01)

The control register allows the user to mute a specific audio channel. It is also used to specify the data type (I^2S, Right-Justified, or Left-Justified.

Table 3. Control Registers (0x01)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	X	X	X	X	–	–	**Left and Right channel are active.**
0	1	X	X	X	X	–	–	Left channel is MUTED.
1	0	X	X	X	X	–	–	Right channel is MUTED.
1	1	X	X	X	X	–	–	Left and Right channel are MUTED.
–	–	X	X	X	X	**0**	**0**	**I^2S data format**
–	–	X	X	X	X	0	1	Right-justified data format (see PACKET LENGTH register 0x07)
–	–	X	X	X	X	1	0	Left-justified data format
–	–	X	X	X	X	1	1	Bypass mode – data is passed straight through without delay.

(1) Default values are in **bold**.

AUDIO DELAY REGISTERS (0x02–0x05)

The audio delay for the left and right channels is fixed by writing a total of 13 bits (2 byte transfer) to upper and lower registers as specified in Table 1. A multiple byte transfer should be performed starting with the control register and following with 4 bytes to fill the upper and lower registers associated with right/left channel delay. The decimal value of D0–D13 equals the number of samples to delay. The maximum number of delayed samples is 8191 for the TPA5050. This equates to 170.65 ms [8191 × (1/fs)] at 48 kHz.

Table 4. Audio Delay Registers (0x02–0x05)(1)

D13	D12	D11–D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**Left and Right audio is passed to output with no delay.**
0	0	0	0	1	Left and Right audio is delayed by 1 sample (1/fs = delay time)
1	1	1	1	1	Left and Right audio is delayed by 8191 samples (8191/fs = delay time)

(1) Default values are in **bold**.

FRAME DELAY REGISTERS (0x06)

This register can be used to specify delay in video frames instead of audio samples. When the MSB is set to 1, the audio delay registers (0x01–0x04) are bypassed and the Frame Delay Register is used to set the delay based on the frame rate (D6), audio sample rate (D5–D3), and number of frames to delay (D2–D0).

The total audio delay time is calculated by the following formula:

Audio Delay (in samples) = int [# Delay Frames × (1/Frame Rate) × Audio Sample Rate]

If the result of the formula above is greater than the maximum number of delay samples (8191 for TPA5050), then the value is limited to this maximum before passing to the delay block.

Table 5. Frame Delay Registers (0x06)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								**Settings in this register are masked and audio delay is determined by settings in the right/left audio delay registers.**
1								Right/left audio delay registers are masked and delay is determined by settings in this register.
	0							**Frame rate = 50 Hz**
	1							Frame rate = 59.94 Hz
		0	**0**	**0**				**Audio sample rate = 32 kHz**
		0	0	1				Audio sample rate = 44.1 kHz
		0	1	0				Audio sample rate = 48 kHz
		0	1	1				Audio sample rate = 88.2 kHz
		1	0	0				Audio sample rate = 96 kHz
		1	0	1				Audio sample rate = 176.4 kHz
		1	1	0				Audio sample rate = 192 kHz
		1	1	1				Audio sample rate = 192 kHz
					0	**0**	**0**	**Delay frames = 1**
					0	0	1	Delay frames = 2
					1	1	1	Delay frames = 8

(1) Default values are in **bold**.

RJ PACKET LENGTH REGISTERS (0x07)

This register is only used in right justified mode. The decimal value of bits [5:0] represents the width of the useable data in a right justified audio stream. The number of BCLK transitions between LRCLK transitions must be greater than or equal to the packet length selected in this register. The maximum packet length value is 24 bits. Any setting greater whose numerical value is greater than 24 bits is limited to the maximum 24 bits.

Table 6. RJ Package Length (0x07)(1)

D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	Packet length = 0 bits
0	0	0	0	0	1	Packet length = 1 bits
0	1	1	X	X	X	Packet length = 24 bits

(1) Default values are in **bold**.

COMPLETE UPDATE REGISTER (0x08)

Since the audio delay values are divided among several registers, it is likely that multiple writes would be necessary to configure the device. This may cause interruptions in the audio stream and unwanted pops and clicks might occur as register data is passed to delay functional block.

To avoid this from happening, the **Complete Update** register is used to transfer the user settings from the register file to the delay functional block when a 1 is written to the LSB. For example, if the right delay is set to 35 samples, and the left delay is set to 300 samples, the device holds the right channel in MUTE until 35 samples of audio data have passed, and holds the left channel in MUTE until 300 samples of audio data have passed.

Note that the individual channels can be muted using the upper bits of the Control Registers **without** writing to the Complete Update registers.

Table 7. Complete Update Registers (0x08)(1)

D7–D1	D0	FUNCTION
X	**0**	**No data from the register settings is passed to the delay block.**
X	1	Stream type, right/left delay or frame delay, and packet length is passed to the delay functional block.

(1) Default values are in **bold**.

APPLICATION EXAMPLES

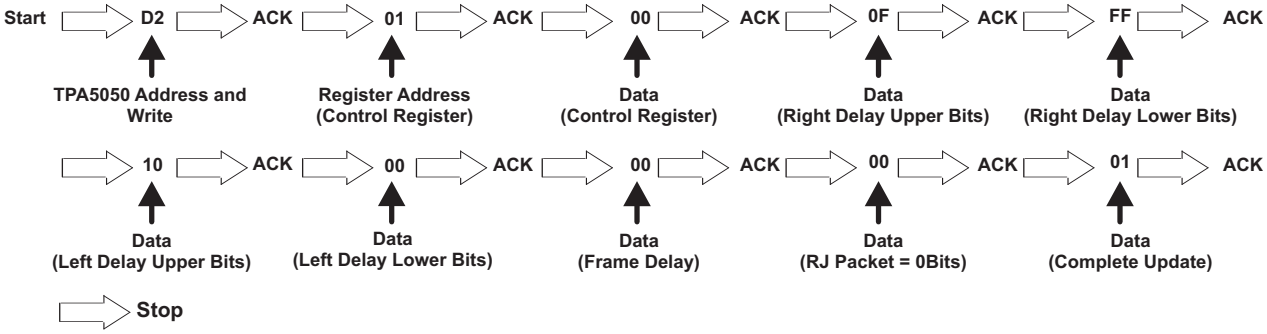
The following are some examples of I²C commands used to read or write to the TPA5050. For all conditions, assume the address of the TPA5050 is set to 001.

Single Byte Write

In this example, the TPA5050 is set to mute both left and right channels, and to operate in I²S mode.

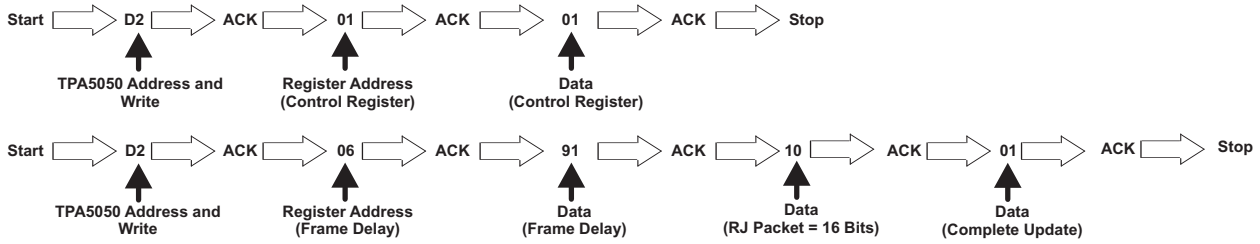
Multiple Byte Write

In this example, the TPA5050 is set to make both the left and right channels active, operate in I²S mode, delay the right channel by 4095 samples, and delay the left channel by 4096 samples. This is a sequential write, so all registers must have data written to them.



Combination Single Byte Write and Sequential Write

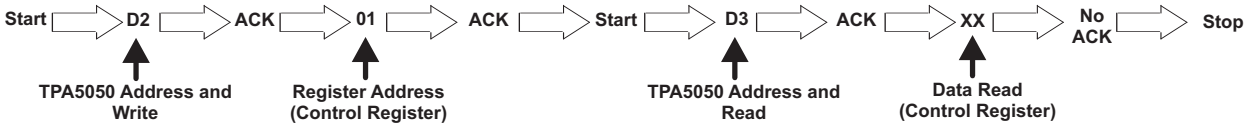
In this example, the TPA5050 is set to operate in the Right Justified mode, with a packet length of 16 bits. The device is to delay the audio signal by 40 ms using the Frame Delay function. Assume the audio sample rate (fs) = 48 kHz, and the Frame rate = 50 Hz. This is a combination of single writes and a sequential write. Since the Right Justified mode is set in the Control Register, and the Frame Delay is set in register 0x06, the data in registers 0x02–0x05 can be ignored.



Note that in every circumstance where a delay was written into the memory of the TPA5050, a *1* must be written to the *Complete Data* register for the change to take effect. This does not apply to muting, which occurs in the *Control* register.

Single Byte Read

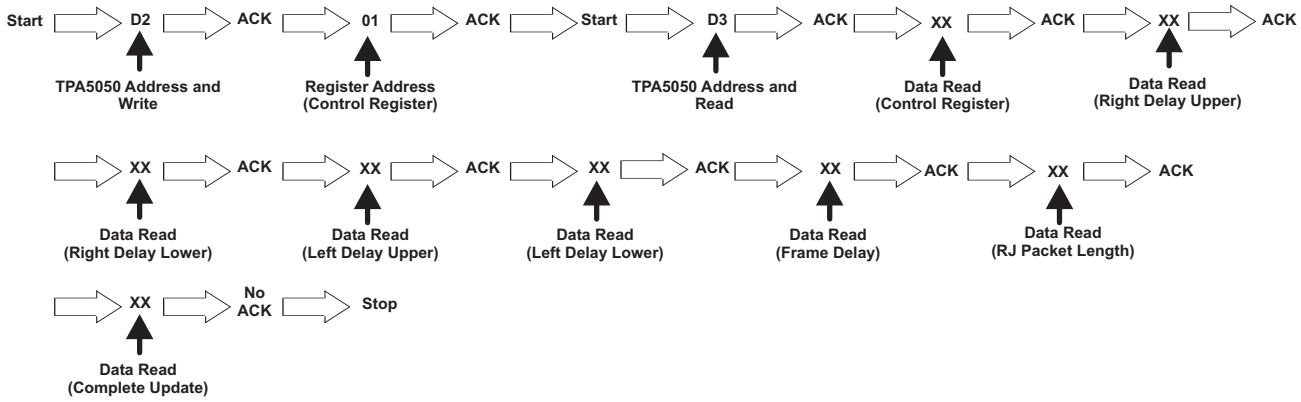
In this example, one byte of data is read from the Control Register (0x01). After the data (represented *xx*) by is read by the master device, the master device issues a Not Acknowledge, before stopping the communication.



Multiple Byte Read

Often, when it is necessary to read what is contained in one register, it is necessary to determine what information is contained in all registers. In such a case, a sequential read should be used. In situations where data must be read from a register at the beginning (0x01), and a register towards the end (0x07), a sequential read is likely to be faster to implement than multiple single byte reads.

In this example, a sequential read is initiated with the Control Register (0x01), and ends with the Complete Update Register (0x08).



DEVICE CURRENT CONSUMPTION

The TPA5050 draws different amounts of supply current depending upon the conditions under which it is operated. As V_{DD} increases, so too does I_{DD}. Likewise, as V_{DD} decreases, I_{DD} decreases. The same is true of the sampling frequency, fs. An increase in fs causes an increase in I_{DD}. Figure 11 illustrates the relationship between operating condition and typical supply current.

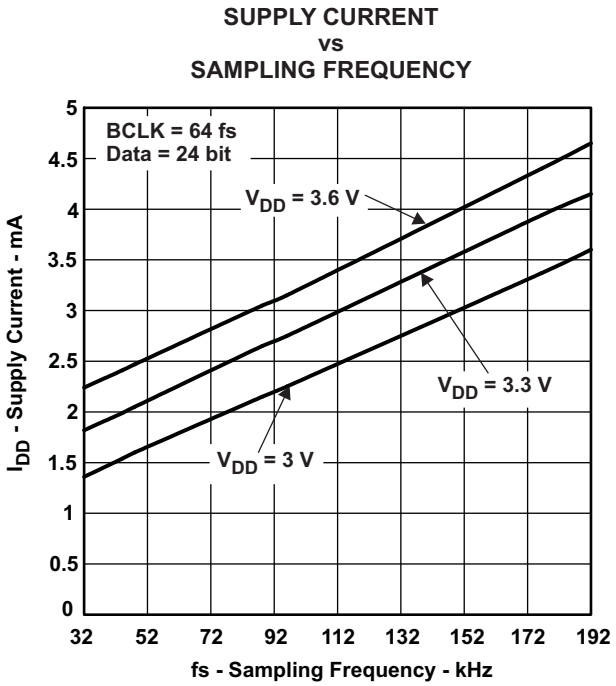


Figure 11. Typical Supply Current

PACKAGING INFORMATION

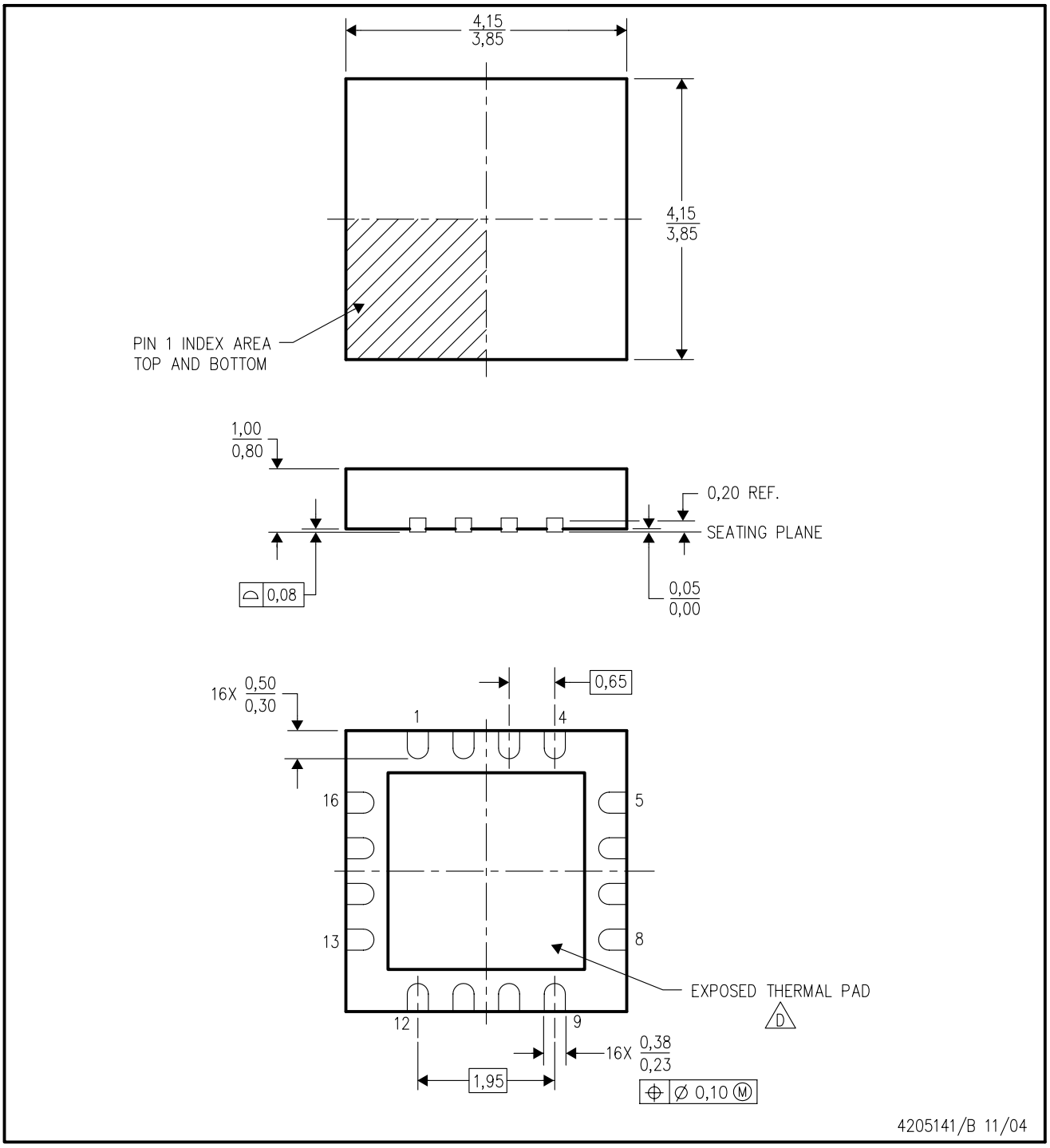
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPA5050RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5050RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5050RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA5050RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RSA (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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