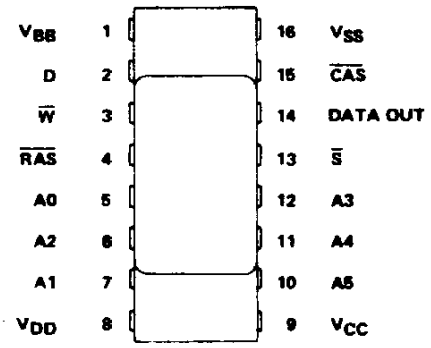
TMS 4027 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORY

- 4096 X 1 Organization
- Industry Standard 16-Pin 300-Mil Package Configuration
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Three-State Fully TTL-Compatible Output Latched and Valid Into Next Cycle
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4027-15	150 ns	100 ns	320 ns	330 ns
TMS 4027-20	200 ns	135 ns	375 ns	420 ns
TMS 4027-25	250 ns	165 ns	375 ns	480 ns

- Page-Mode Operation for Faster Access Time
- Low-Power Dissipation
  - Operating 460 mW (max)
  - Standby 27 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology

16-PIN CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



PIN NAMES

A0–A5	Address Inputs
$\overline{CAS}$	Column address strobe
D	Data input
DATA OUT	Data output
$\overline{RAS}$	Row address strobe
$\overline{S}$	Chip select
$\overline{W}$	Write enable
V_{BB}	−5 V power supply
V_{CC}	+5 V power supply
V_{DD}	+12 V power supply
V_{SS}	0 V ground

scription

The TMS 4027 JL, NL series is composed of monolithic high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words, employing single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe ($\overline{RAS}$) or ($\overline{R}$) and Column Address Strobe ($\overline{CAS}$) or ($\overline{C}$). All address lines (A0 through A5) and data-in (D) are latched on chip to simplify system design. Data out is latched and available until the negative edge of $\overline{CAS}$ in the next memory cycle returns the output to the high-impedance state.

Typical power dissipation is less than 300 milliwatts active and 14 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 20 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4027 JL, NL series is offered in a 16-pin dual-in-line package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil centers.

eration

address (A0 through A5)

Twelve address bits are required to decode 1 of 4096 storage cell locations. Six row-address bits are set up on pins A0 through A5 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on

† term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

LIMINARY DATA SHEET:
plementary data will be
lished at a later date.

pins A0 through A5 and latched onto the chip by the column-address strobe ($\overline{CAS}$). $\overline{RAS}$ activates the sense amplifiers as well as the row decoder, and $\overline{CAS}$ activates the column decoder and the input and output buffers.

chip select ($\overline{S}$)

When the chip select ($\overline{S}$) input is high, the column decode and the input and output buffers are disabled. However, the row decode is unaffected by chip select so that row addresses are latched and refresh can continue to take place.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data-out will contain the data written into the selected cell.

data-in (D)

Data is written during a write or read modify-write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output goes into the high-impedance state after the negative transition of $\overline{CAS}$. The output becomes valid after the access time has elapsed, and it remains valid into the next memory cycle before $\overline{CAS}$ going low returns it to a high-impedance state.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 64 row addresses (A0 through A5) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe the row addresses is eliminated. To extend beyond the 64 column locations on a single RAM, apply the row address and $\overline{RAS}$ to multiple 4K RAMs, then decode chip select to select the proper RAM. (A RAM need not be selected during the first page mode cycles to have the row address latched on chip.)

power up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applied to system use where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

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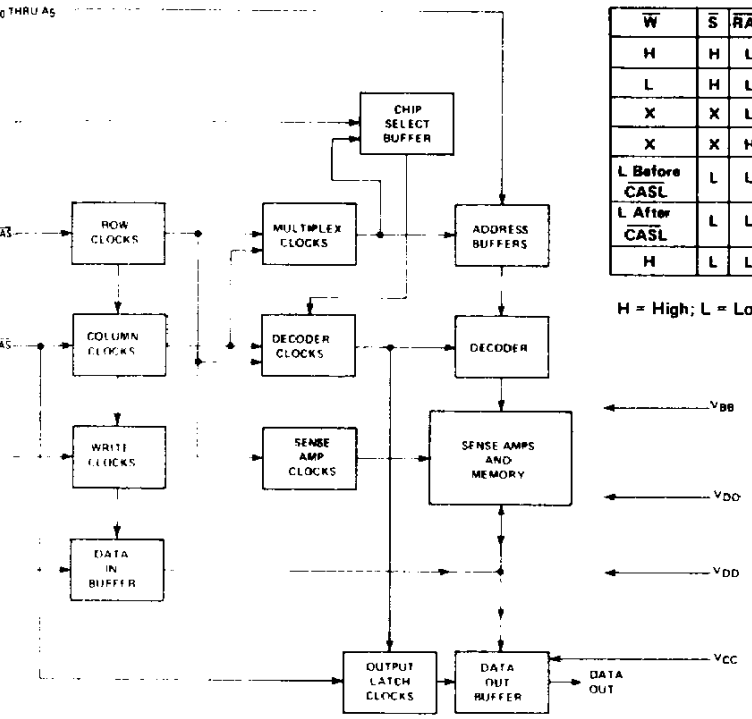
ctional block diagram



$\overline{W}$	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	OUTPUT	MODE
H	H	L	L	Hi-Z	Not selected
L	H	L	L	Hi-Z	No write will occur
X	X	L	H	Hi-Z	$\overline{RAS}$ only cycle
X	X	H	L	Hi-Z	$\overline{CAS}$ only cycle
L Before $\overline{CAS}$	L	L	L	Input data	Early write
L After $\overline{CAS}$	L	L	L	Valid data	Write or read/write cycle
H	L	L	L	Data out	Read

H = High; L = Low; X = Don't Care; Hi-Z = High impedance.

olute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 20 V
Voltage on V_{DD}, V_{CC}, relative to V_{SS}	−1.0 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 20 V
All input voltages (see Note 1)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 10 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

TE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

eses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and ctional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" tion of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

commended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
upply voltage, V_{BB}	−4.5	−5	−5.5	V
upply voltage, V_{CC}	4.5	5	5.5	V
upply voltage, V_{DD}	10.8	12	13.2	V
upply voltage, V_{SS}		0		V
igh-level input voltage, except $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$, V_{IH}	2.2	3.5	7	V
igh-level input voltage, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$, $V_{IH(R)}$	2.4	3.5	7	V
ow-level input voltage, V_{IL}	−1	0	0.8	V
efresh time, $t_{refresh}$			2	ms
perating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA, C_L = 50 pF			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 10 V, All other pins = 0 V except V_{BB} = −5 V			10	µA
I_O	Output current (leakage)	V_O = 0 to 10 V, $\overline{RAS}$ and $\overline{CAS}$ high, Output disabled, after 1 memory cycle			10	µA
$I_{BB(av)}$	Average operating current	Minimum cycle time		90	150	µA
$I_{CC(av)}$*	during read or write					
$I_{DD(av)}$	cycle	Minimum cycle time		25	35	mA
I_{DD}	Standby current, $\overline{RAS}$, $\overline{CAS}$, and $\overline{CS}$ high	Chip deselected after 1 memory cycle		0.85	2	mA
	$\overline{RAS}$, $\overline{CAS}$ high, $\overline{CS}$ low			2	4	
$I_{DD(av)}$	Average refresh current, $\overline{RAS}$ cycling, $\overline{CAS}$ high	Minimum cycle time		15	25	mA
I_{BB}	Standby current, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ high			90	150	µA

*V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.

capacitance over recommended supply voltage range and operating free-air temperature range f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 50 pF, $t_{r(C)}$ and $t_{r(R)}$ = 5 ns,		100		135		165	ns
$t_{a(R)}$	Access time from row address strobe	$t_{RL,CL}$ = MAX, Load = 2 Series 74 TTL gates		150		200		250	ns
t_{PVZ}	Output valid time	C_L = 50 pF, Load = 2 Series 74 TTL gates	10		10		10		µs
t_{PXZ}	Output disable time		0	40	0	50	0	60	ns

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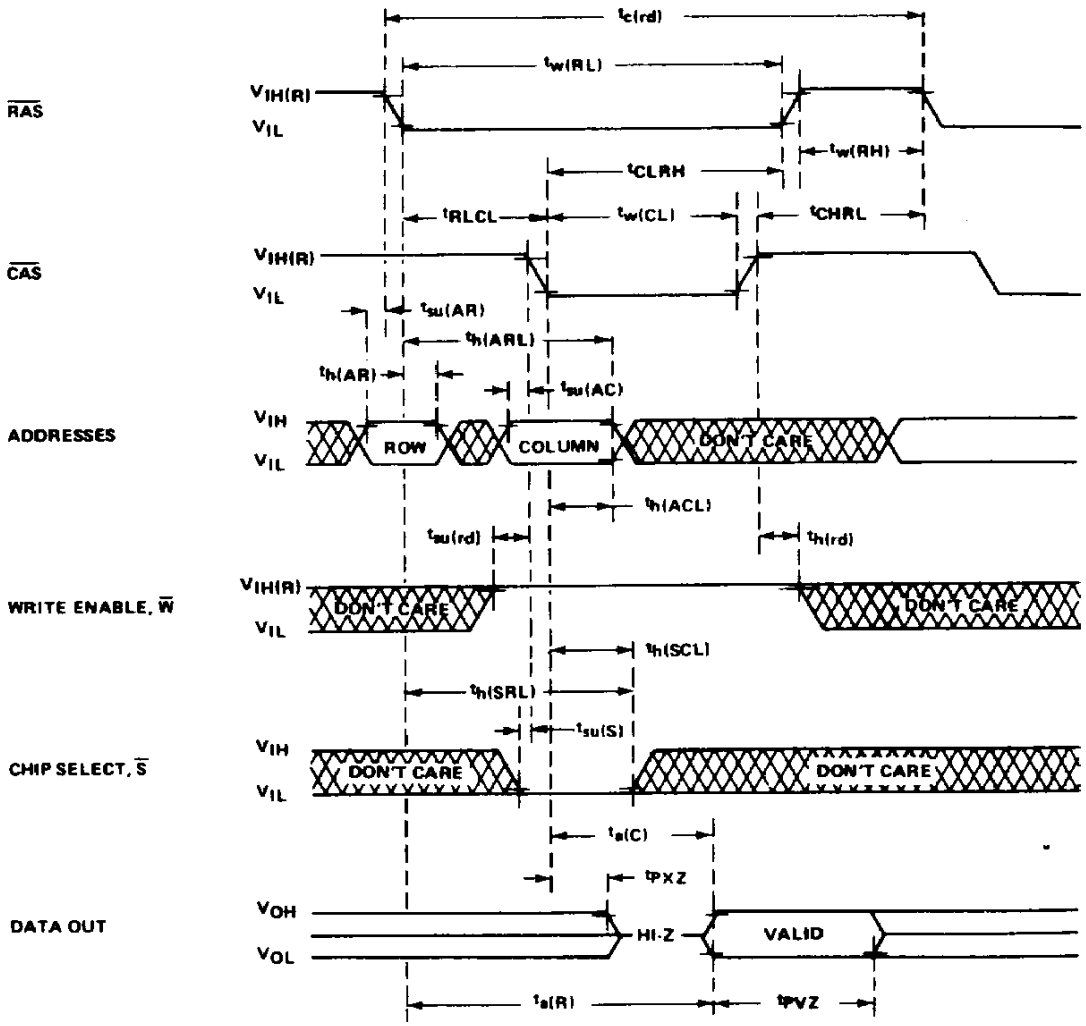
ing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TMS 4027-15		TMS 4027-20		TMS 4027-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
rd)	Read cycle time	320		375		375		ns
W)	Write cycle time	320		375		375		ns
RW)	Read, modify-write cycle time	330		420		480		ns
CH)	Pulse width, column address strobe high (precharge time)	60		80		110		ns
CL)	Pulse width, column address strobe low	100		135		165		ns
RH)	Pulse width, row address strobe high (precharge time)	100		120		120		ns
RL)	Pulse width, row address strobe low	150	10,000	200	10,000	250	10,000	ns
W)	Write pulse width	45		55		75		ns
	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	3	35	3	50	3	50	ns
AC)	Column address setup time	−10		−10		−10		ns
AR)	Row address setup time	0		0		0		ns
D)	Data setup time	0		0		0		ns
S)	Chip select setup time	−10		−10		−10		ns
rd)	Read command setup time	0		0		0		ns
WCH)	Write command setup time before $\overline{CAS}$ high	50		70		85		ns
WRH)	Write command setup time before $\overline{RAS}$ high	50		70		85		ns
ACL)	Column address hold time after $\overline{CAS}$ low	45		55		75		ns
AR)	Row address hold time	20		25		35		ns
ARL)	Column address hold time after $\overline{RAS}$ low	95		120		160		ns
DCL)	Data hold time after $\overline{CAS}$ low	45		55		75		ns
DRL)	Data hold time after $\overline{RAS}$ low	95		120		160		ns
DWL)	Data hold time after $\overline{W}$ low	45		55		75		ns
rd)	Read command hold time	0		0		0		ns
SCL)	Chip select hold time after $\overline{CAS}$ low	45		55		75		ns
SRL)	Chip select hold time after $\overline{RAS}$ low	95		120		160		ns
WCL)	Write command hold time after $\overline{CAS}$ low	45		55		75		ns
HRL	Delay time, column address strobe high to row address strobe low	0		0		0		ns
LRH	Delay time, column address strobe low to row address strobe high	100		135		165		ns
LWL	Delay time, column address strobe low to $\overline{W}$ low (read, modify-write cycle only)	60		80		90		ns
EF	Refresh period		2		2		2	ms
LCL	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	20	50	25	65	35	85	ns
LWL	Delay time, row address strobe low to $\overline{W}$ low (read, modify-write cycle only)	110		145		175		ns
LCL	Delay time, $\overline{W}$ low to column address strobe low (early write cycle)	0		0		0		ns

E: All timing is measured from $V_{IH(R)}$ or V_{IH} minimum and V_{IL} maximum; V_{OH} minimum and V_{OL} maximum.

read cycle timing



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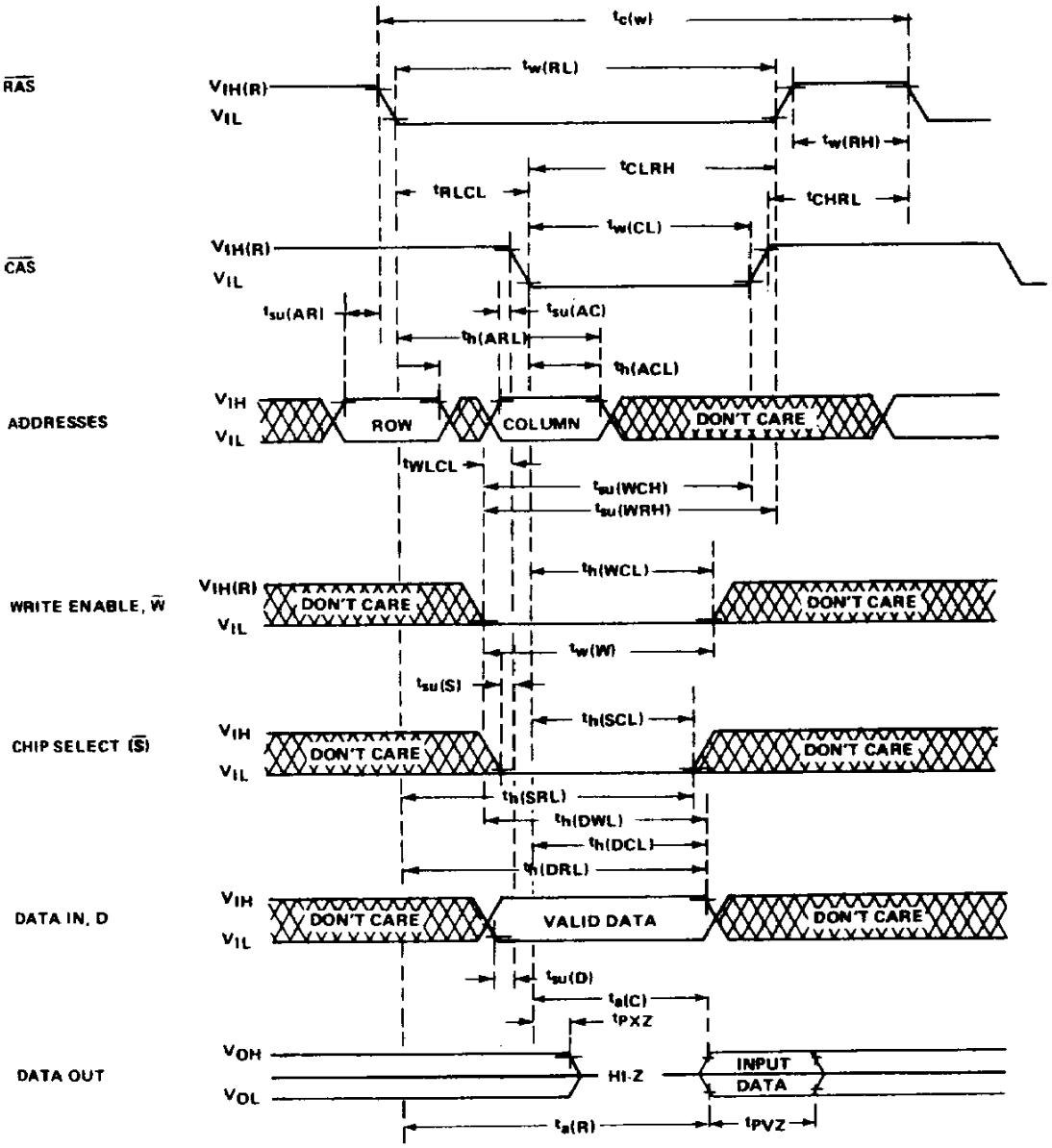
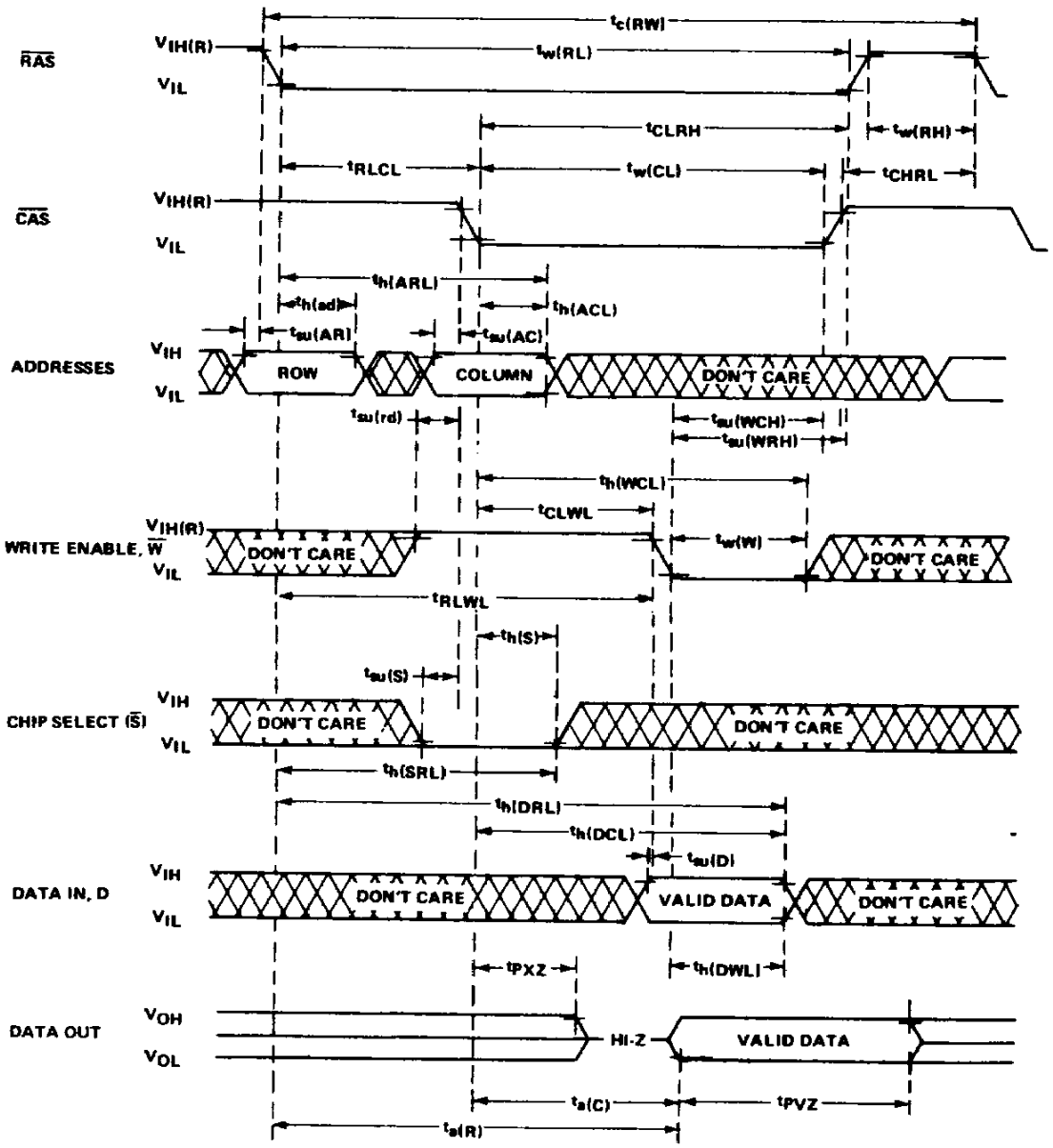
early write cycle timing



read-write/read-modify-write cycle timing



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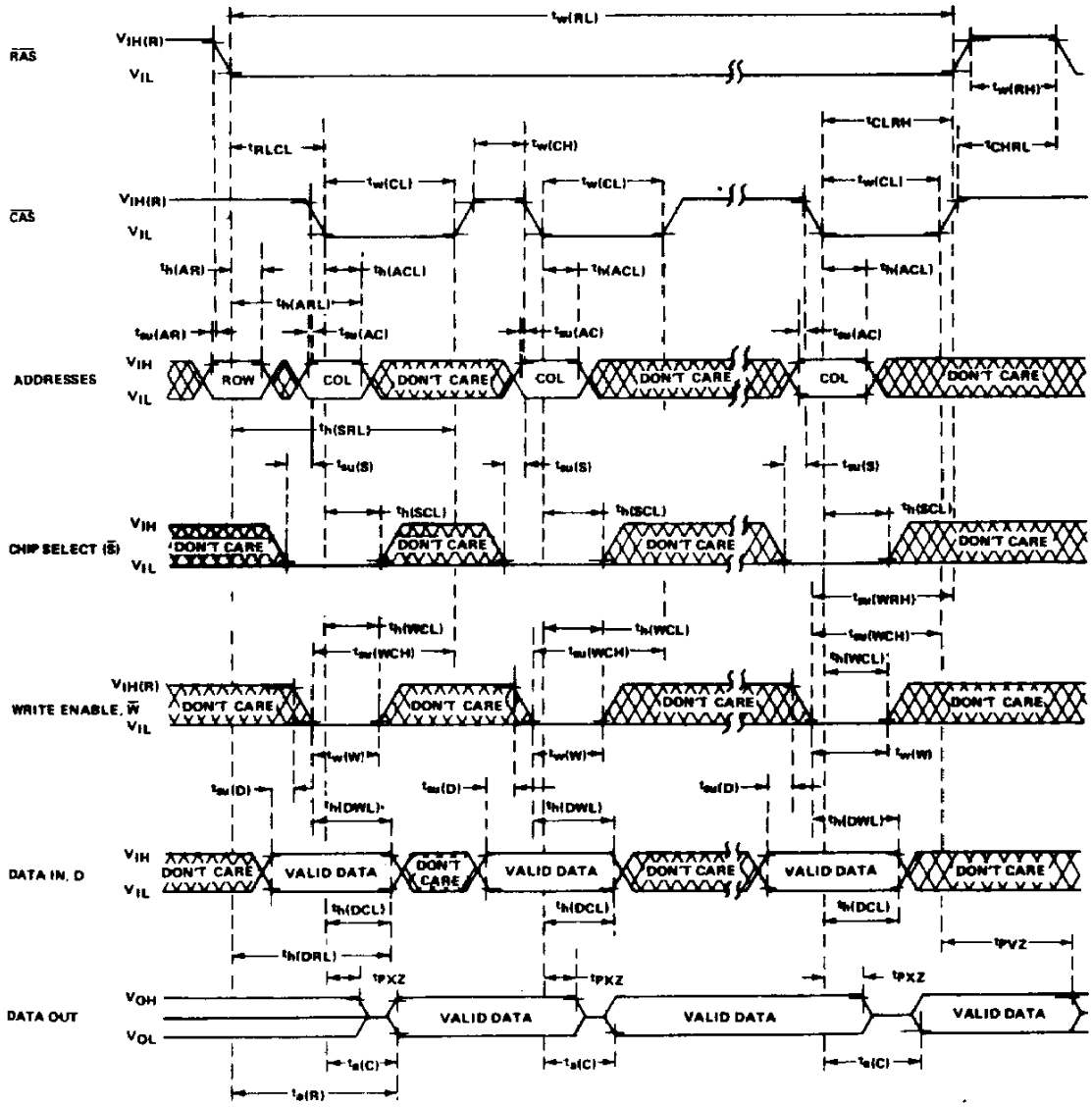
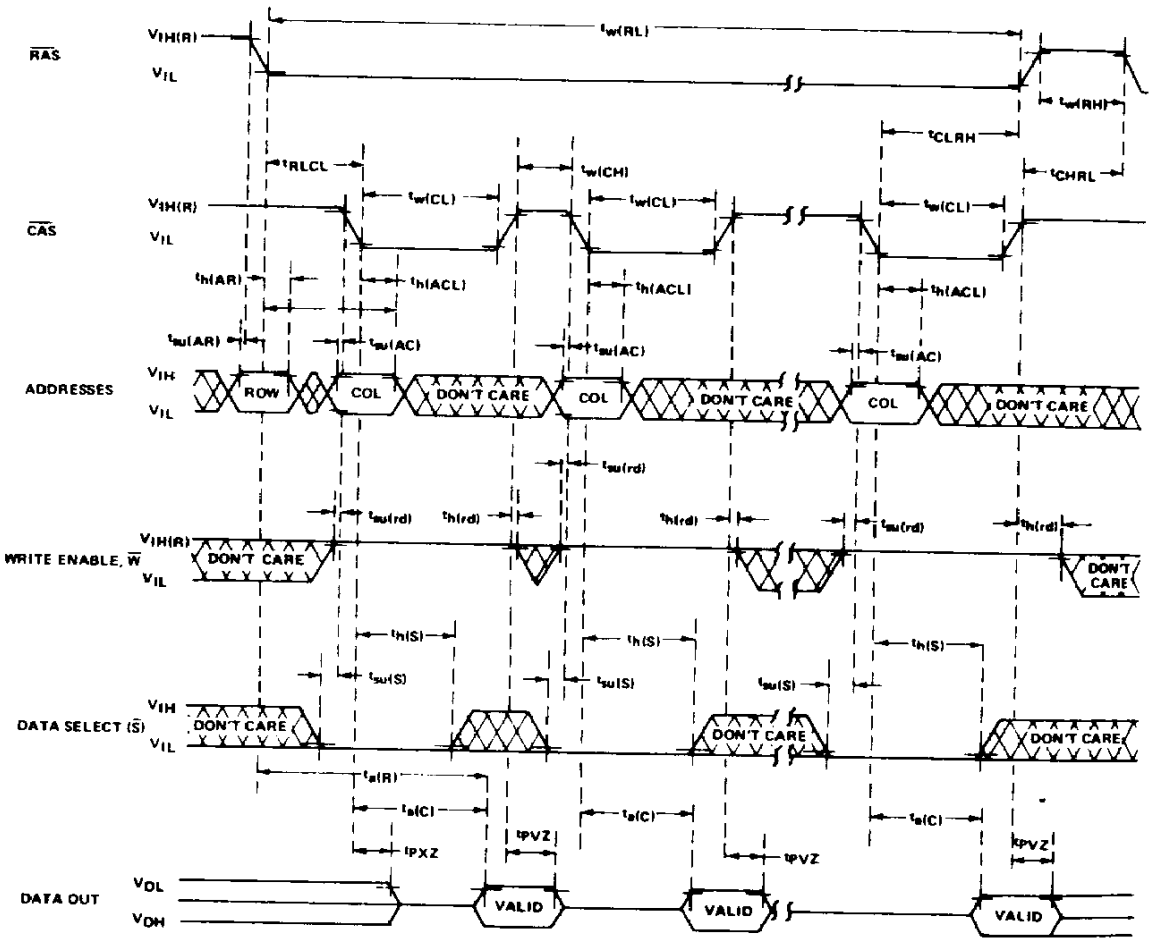
page mode write cycle timing



page mode read cycle timing



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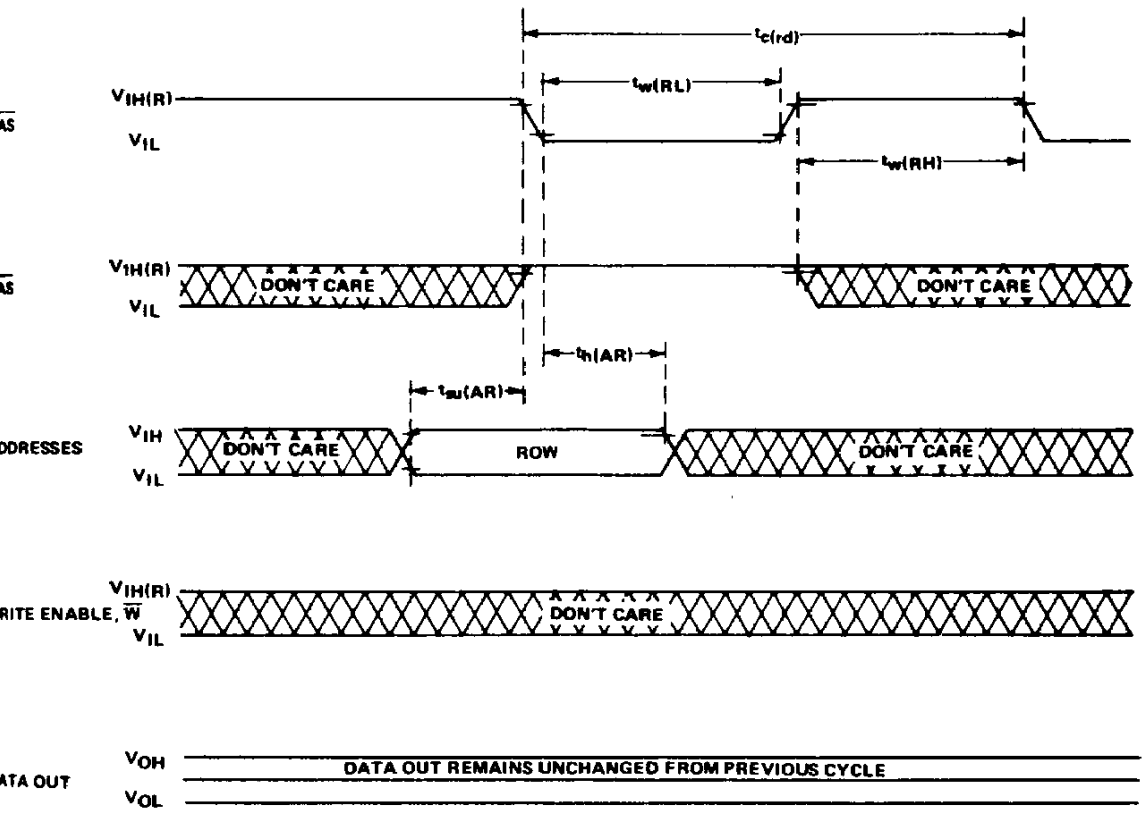
$\overline{AS}$ only refresh timing



iming diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
———	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state