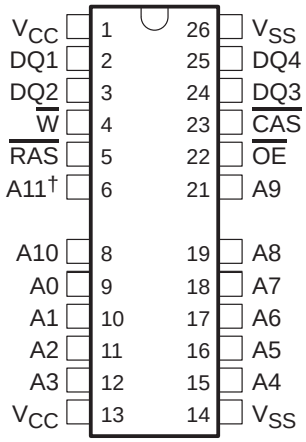
This data sheet is applicable to all TMS41x400As symbolized by Revision "B", Revision "E" and subsequent revisions as described in the device symbolization section.

- **Organization . . . 4194304 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **2048-Cycle Refresh in 32 ms for TMS417400A**
- **4096-Cycle Refresh in 64 ms for TMS416400A**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'41x400A-50	50 ns	13 ns	25 ns	90 ns
'41x400A-60	60 ns	15 ns	30 ns	110 ns
'41x400A-70	70 ns	18 ns	35 ns	130 ns

- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$) Refresh**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 24/26-Lead 300-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DJ Suffix)**
- **Ambient Temperature Range: 0°C to 70°C**

DJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A[0:11]†	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ[1:4]	Data In/Data Out
$\overline{OE}$	Output Enable
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† A11 is NC for TMS417400A

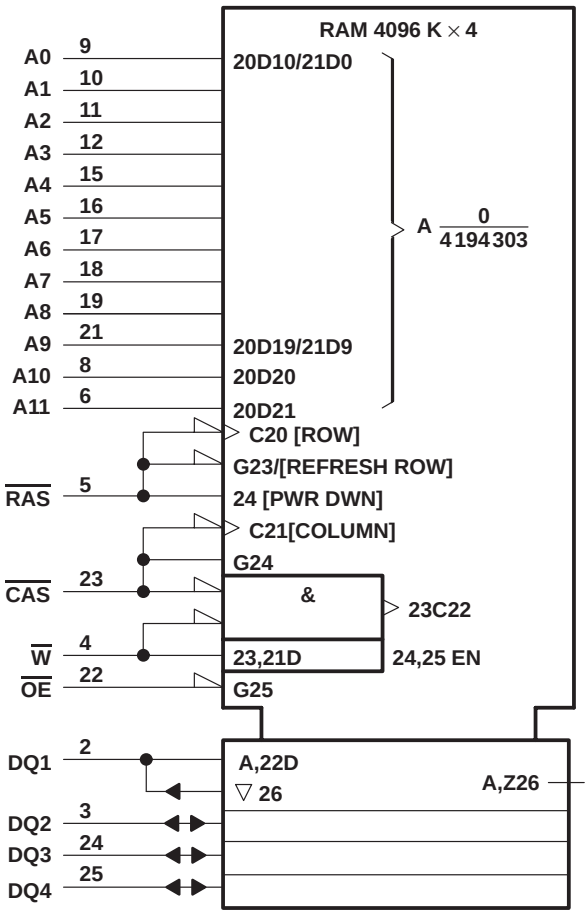
description

The TMS41x400A is a set of 16 777 216-bit dynamic random-access memory (DRAMs) devices organized as 4194304 words of 4 bits each. The TMS41x400A employs state-of-the-art technology for high performance, reliability, and low power.

These devices feature maximum $\overline{RAS}$ access times of 50-, 60-, and 70 ns. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

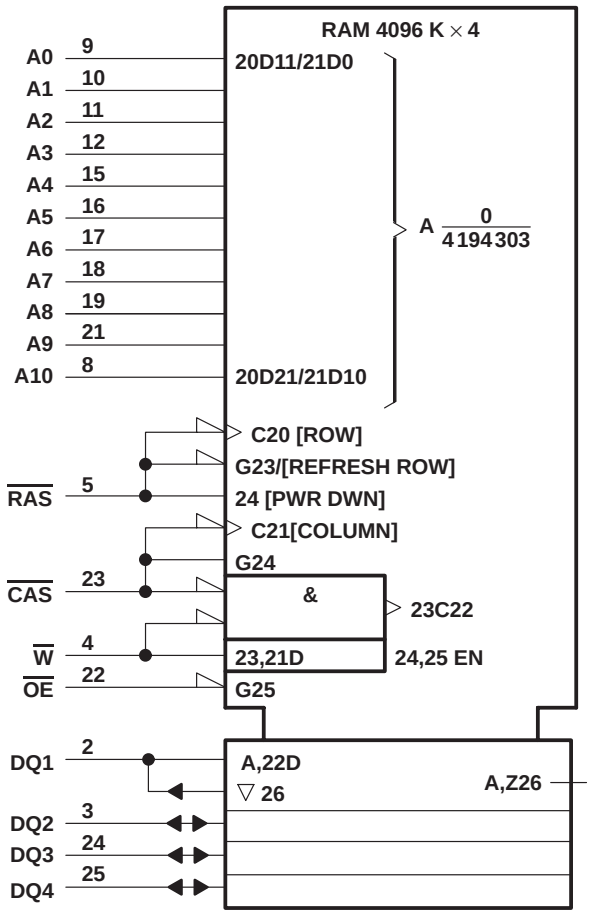
The TMS416400A and TMS417400A are offered in a 24/26-lead plastic surface-mount SOJ package (DJ suffix). This package is designed for operation from 0°C to 70°C.

logic symbol (TMS416400A)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

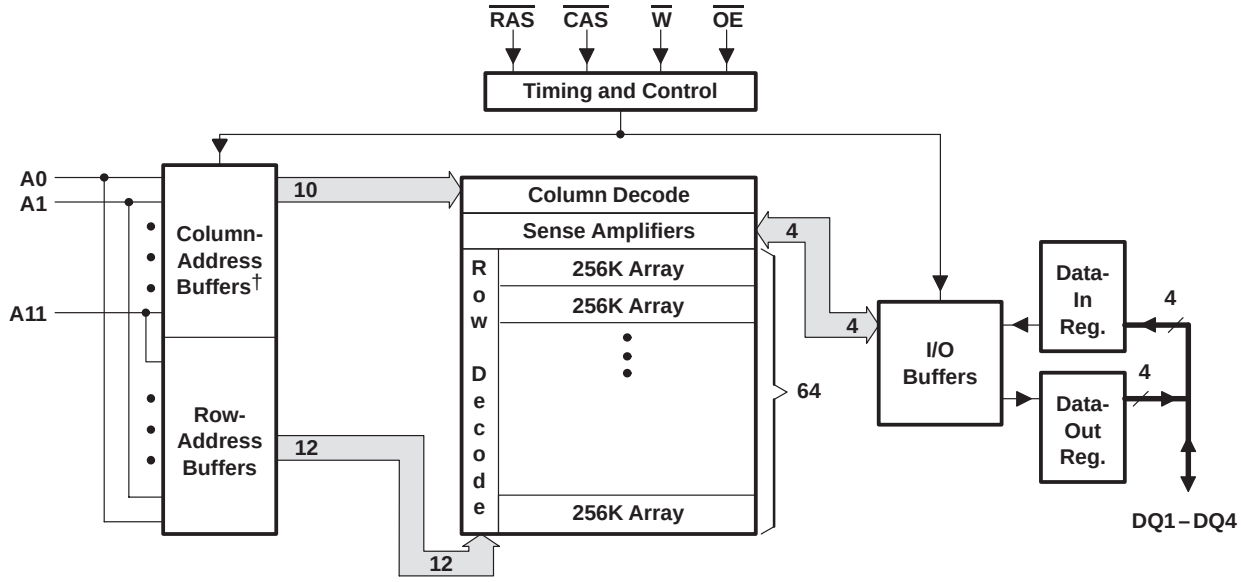
logic symbol (TMS417400A)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

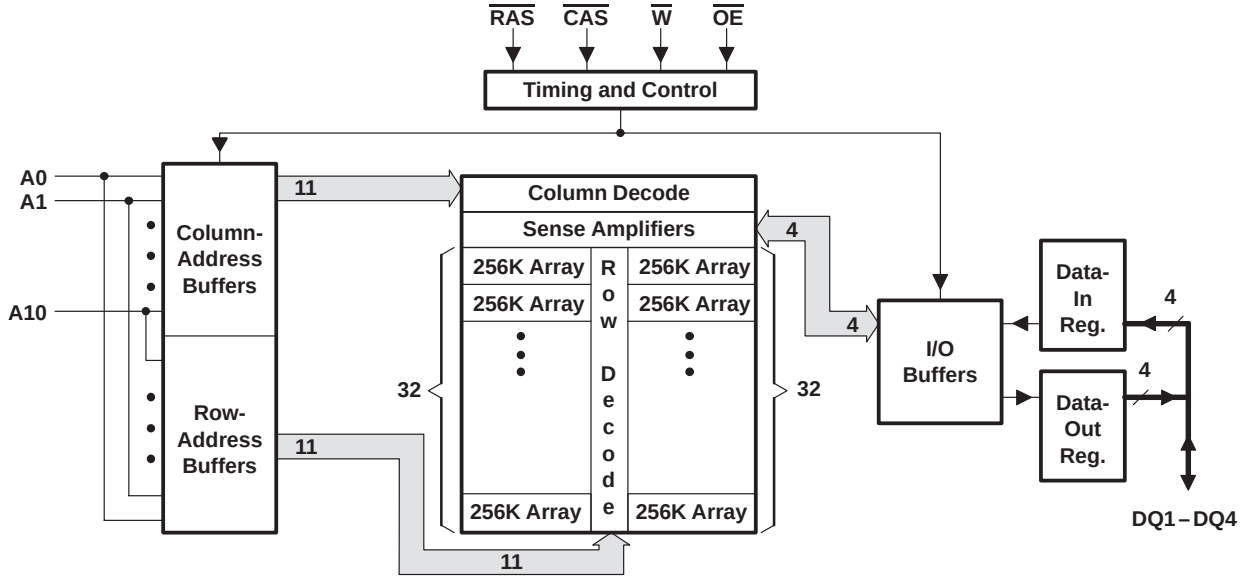
functional block diagram

TMS416400A



† Column addresses A10 and A11 are not used.

TMS417400A



operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses and enables the output. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode devices because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced-page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} or t_{CAC}.

address: A0 – A11 (TMS416400A) and A0 – A10 (TMS417400A)

Twenty-two address bits are required to decode each of the 4194304 storage cell locations. For the TMS416400A, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Ten column-address bits are set up on A0 through A9. For TMS417400A, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by $\overline{RAS}$. Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read- or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ1 – DQ4)

Data is written during a write- or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup-and-hold times referenced to this signal. In a delayed-write- or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with the setup-and-hold time referenced to this signal. Also, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ1 – DQ4)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

$\overline{\text{RAS}}$-only refresh

TMS416400A

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4 096 rows (A0–A11). A normal read- or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

TMS417400A

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 2 048 rows (A0–A10). A normal read- or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

power up

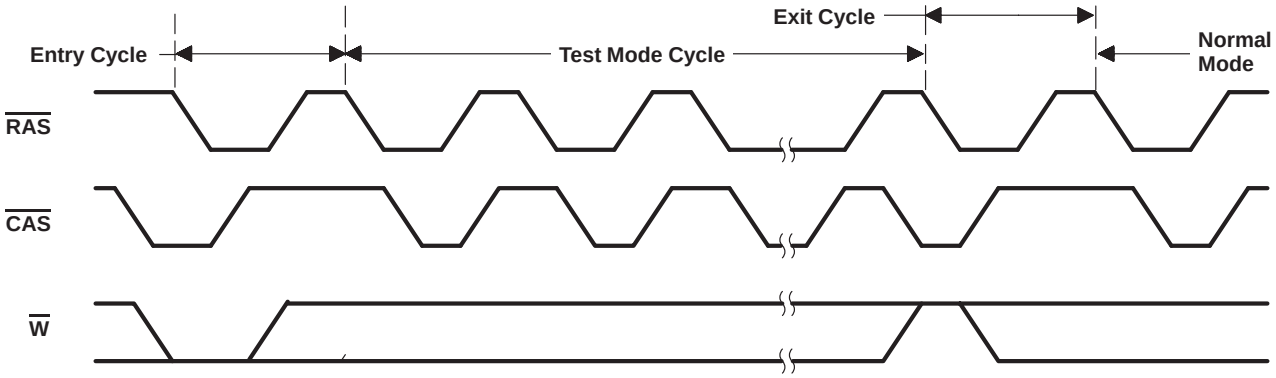
To achieve proper device operation, an initial pause of 200 µs, followed by a minimum of eight initialization cycles, is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

test mode

The test mode is initiated with a CBR-refresh cycle while simultaneously holding the $\overline{\text{W}}$ input low. The entry cycle performs an internal-refresh cycle while internally setting the device to perform a parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR-refresh cycle (with $\overline{\text{W}}$ held high) or a $\overline{\text{RAS}}$-only refresh cycle is performed.

In the test mode, the device is configured as 1 024K bits × 4 bits for each DQ. Each DQ pin has a separate 4-bit parallel-read- and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, DQ goes high; if not, DQ goes low. Test time is reduced by a factor of four for this series of events.

test mode (continued)



NOTE A: The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . –1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x400A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Ambient temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TMS416400A

PARAMETER		TEST CONDITIONS†	'416400A-50		'416400A-60		'416400A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		100		80		70	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), $\overline{After}$ one $\overline{memory}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), $\overline{After}$ one $\overline{memory}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average $\overline{refresh}$ current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		100		80		70	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $t_{\overline{PC}}$ = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		80		70		60	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TMS417400A

PARAMETER		TEST CONDITIONS†	'417400A-50		'417400A-60		'417400A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		130		110		100	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		130		110		100	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ low, $\overline{t_{PC}}$ = MIN, $\overline{CAS}$ cycling		90		70		60	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}.

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance‡		7	pF

† $\overline{A11}$ is NC (no internal connection) for TMS417400A.
‡ $\overline{CAS}$ = V_{IH} to disable outputs.
NOTE 3: V_{CC} = 5 V ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 4)

PARAMETER		’41x400A-50		’41x400A-60		’41x400A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$		13		15		18	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$		13		15		18	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output data hold time from $\overline{CAS}$	3		3		3		ns
t_{OHO}	Output data hold time from $\overline{OE}$	3		3		3		ns
t_{OFF}	Output buffer turn-off delay from $\overline{CAS}$ (see Note 5)	0	13	0	15	0	18	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 5)	0	13	0	15	0	18	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven. Data-in should not be enabled until one of the maximum values is satisfied.

ac timing requirements (see Note 4)

		’41x400A-50		’41x400A-60		’41x400A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	90		110		130		ns
t_{WC}	Cycle time, write	90		110		130		ns
t_{RWC}	Cycle time, read-write	131		155		181		ns
t_{PC}	Cycle time, page-mode read or write (see Note 6)	35		40		45		ns
t_{PRWC}	Cycle time, page-mode read-write	76		85		96		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 7)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 7)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 8)	13	10 000	15	10 000	18	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	8		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data-in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	13		15		18		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	13		15		18		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, write command before $\overline{RAS}$ active (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address	10		10		15		ns
t_{DH}	Hold time, data-in (see Note 9)	10		10		15		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	10		10		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	30		35		40		ns
t_{OEH}	Hold time, $\overline{OE}$ command	13		15		18		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{WRH}	Hold time, write after $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, write command after $\overline{RAS}$ active (test mode only)	10		10		10		ns

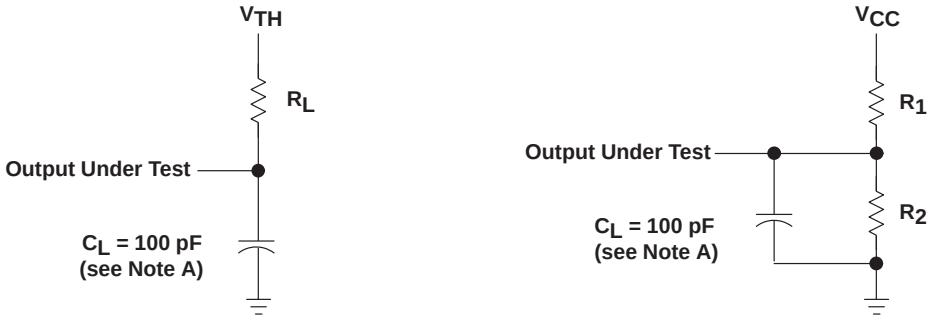
NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
6. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ac timing requirements (see Note 4) (continued)

			'41x400A-50		'41x400A-60		'41x400A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to write command (read-write operation only)		48		55		63		ns
t_{CHR}	Delay time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge		50		60		70		ns
t_{CSR}	Delay time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)		5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write operation only)		36		40		46		ns
t_{OED}	Delay time, $\overline{OE}$ to data in		13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 11)		13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge		25		30		35		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 11)		18	37	20	45	20	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$ active		5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		13		15		18		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write operation only)		73		85		98		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)		53		60		68		ns
t_{TAA}	Access time from address (test mode)		30		35		40		ns
t_{TCPA}	Access time from column precharge (test mode)		35		40		45		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		55		65		75		ns
t_{REF}	Refresh time interval	'416400A		64		64		64	ms
		'417400A		32		32		32	
t_T	Transition time		2	30	2	30	2	30	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
11. The maximum value is specified only to ensure access time.

PARAMETER MEASUREMENT INFORMATION



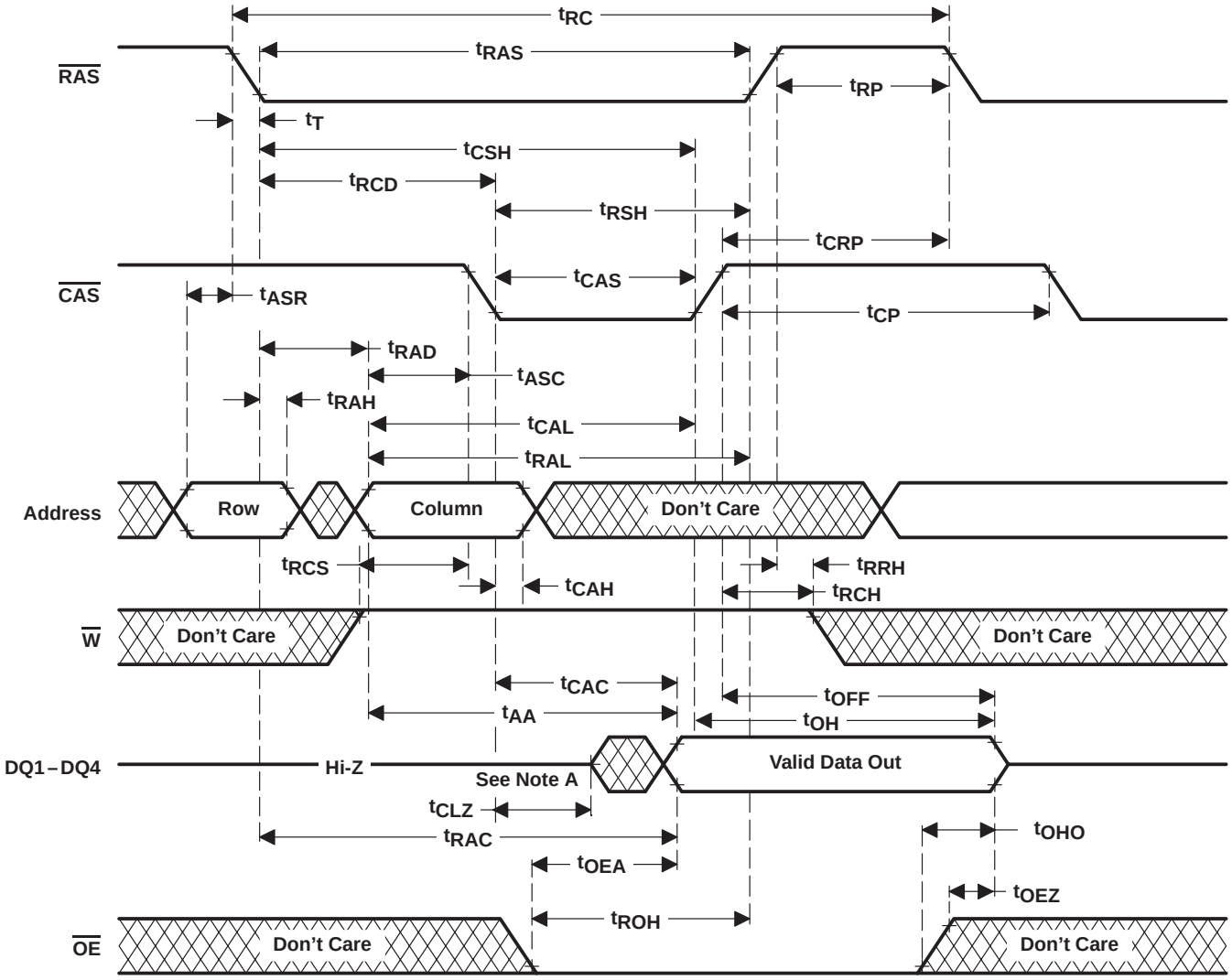
(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	V_{TH} (V)	R_L (Ω)
'41x400A	5	828	295	1.31	218

Figure 2. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

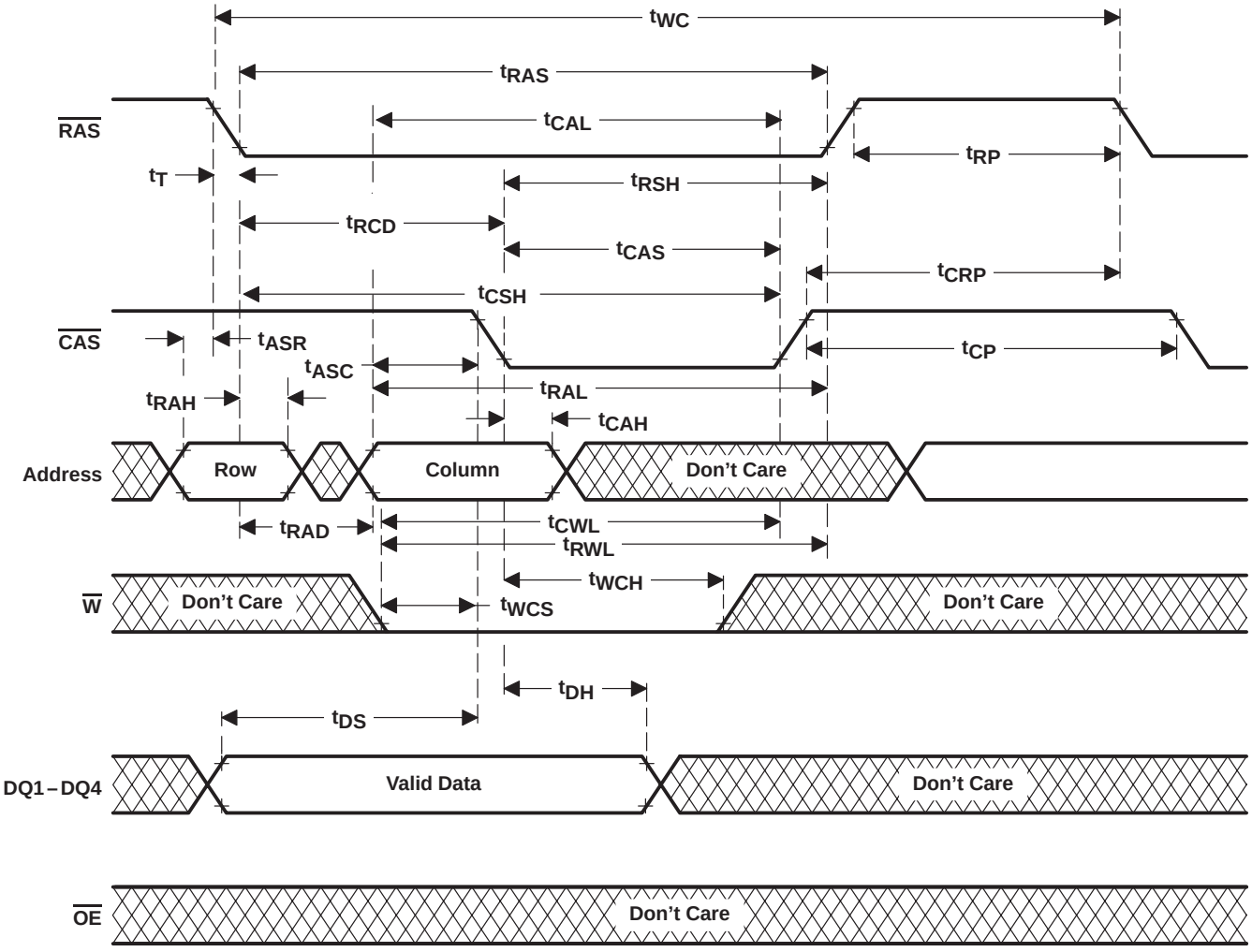


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

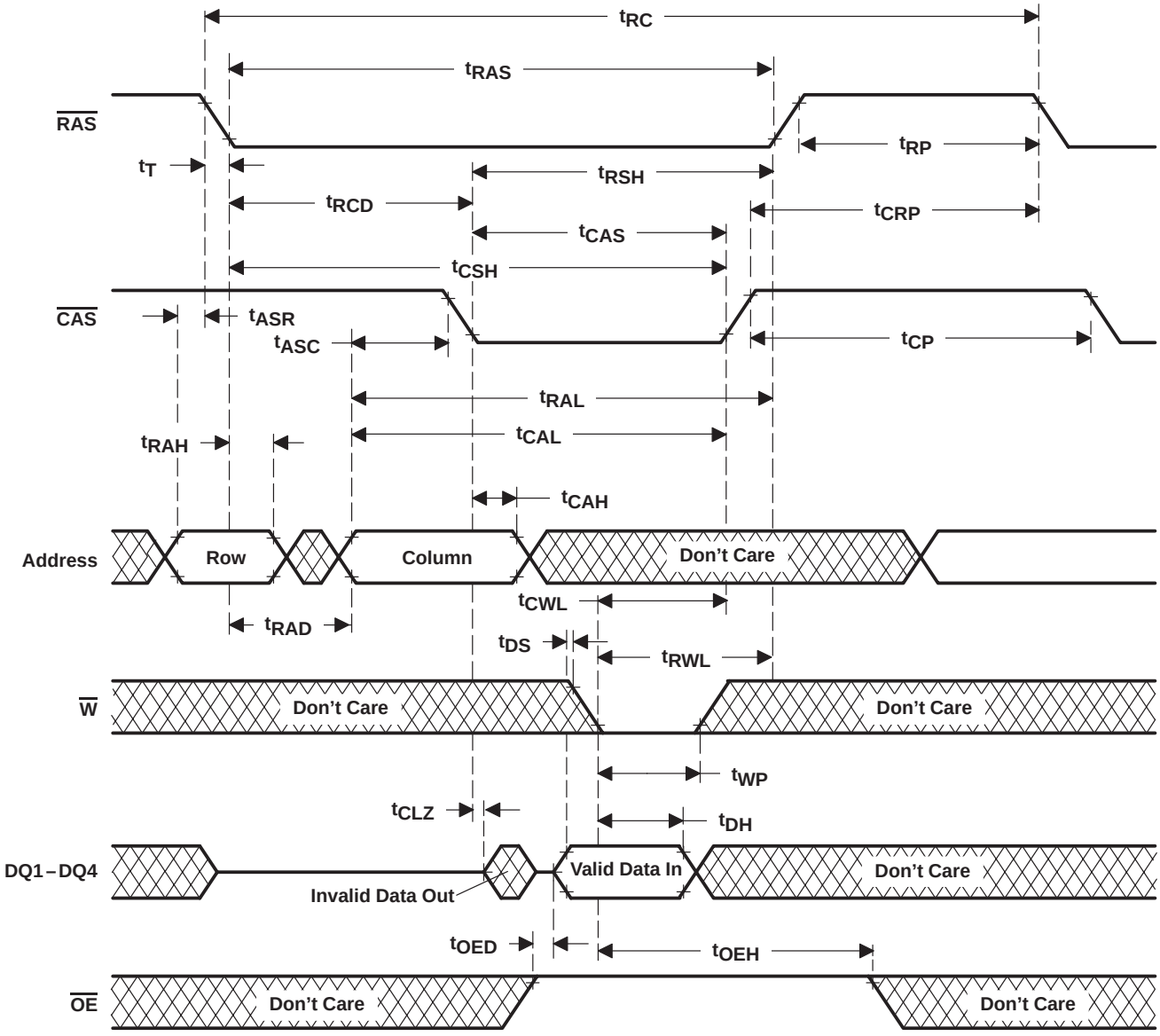
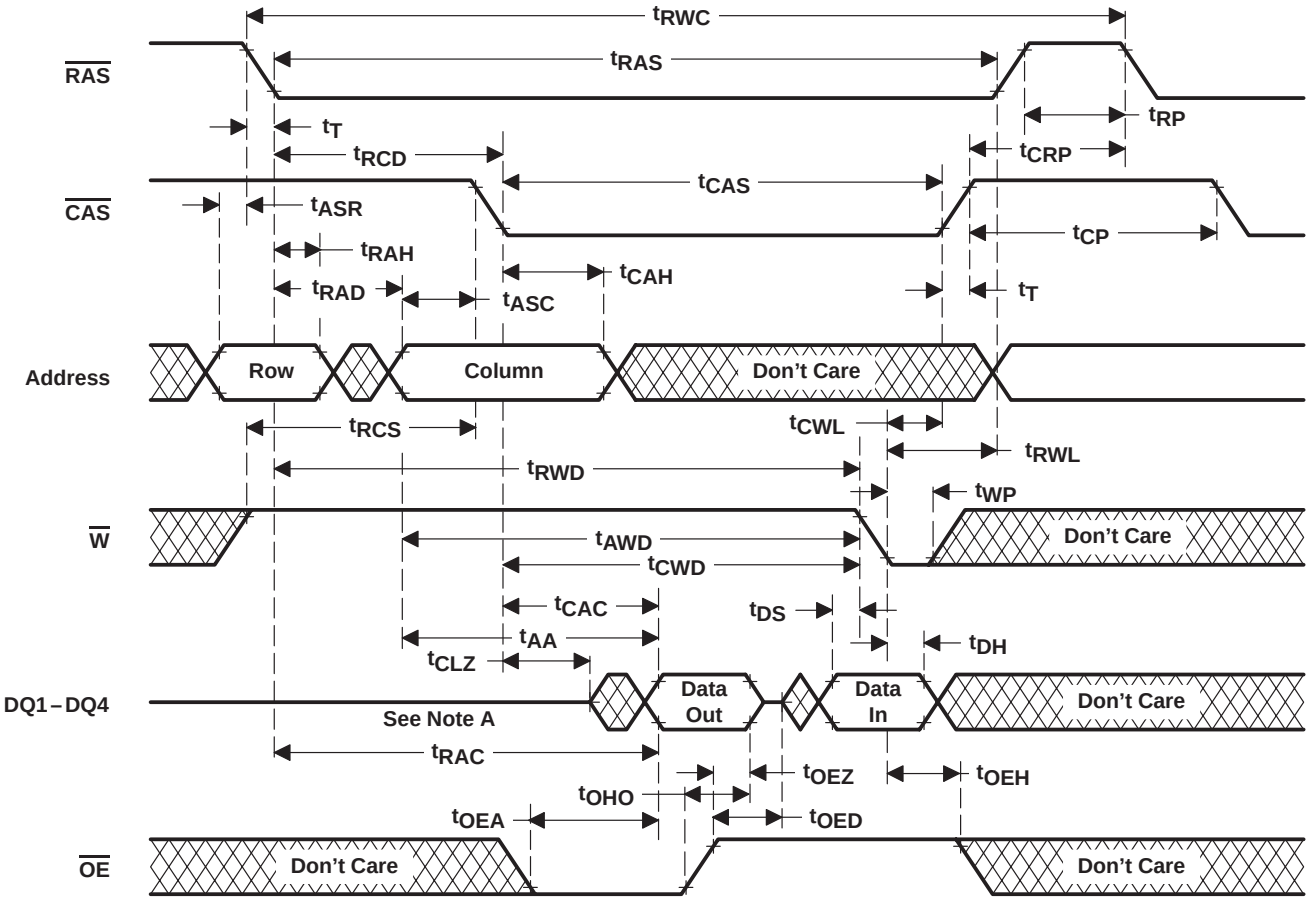


Figure 5. Write-Cycle Timing

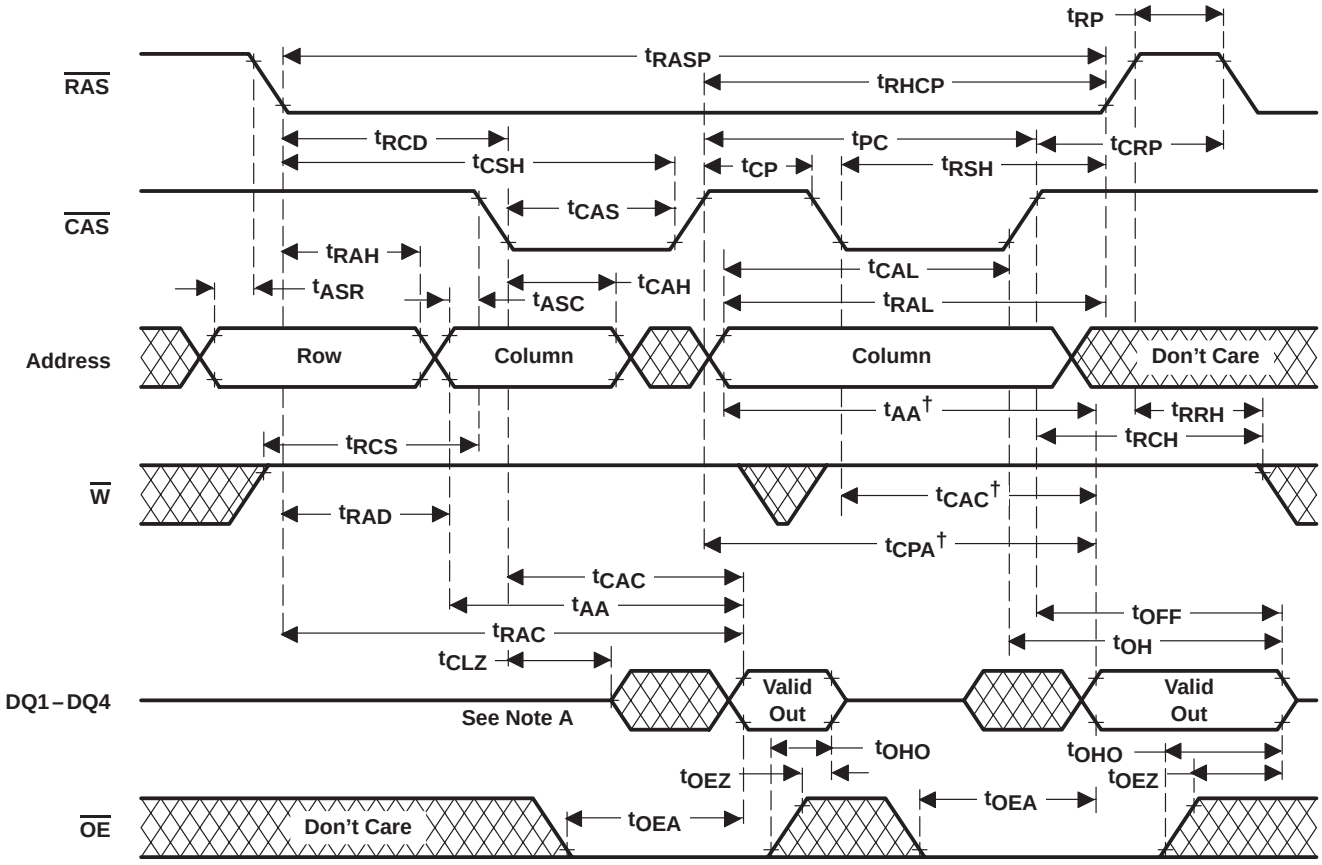
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

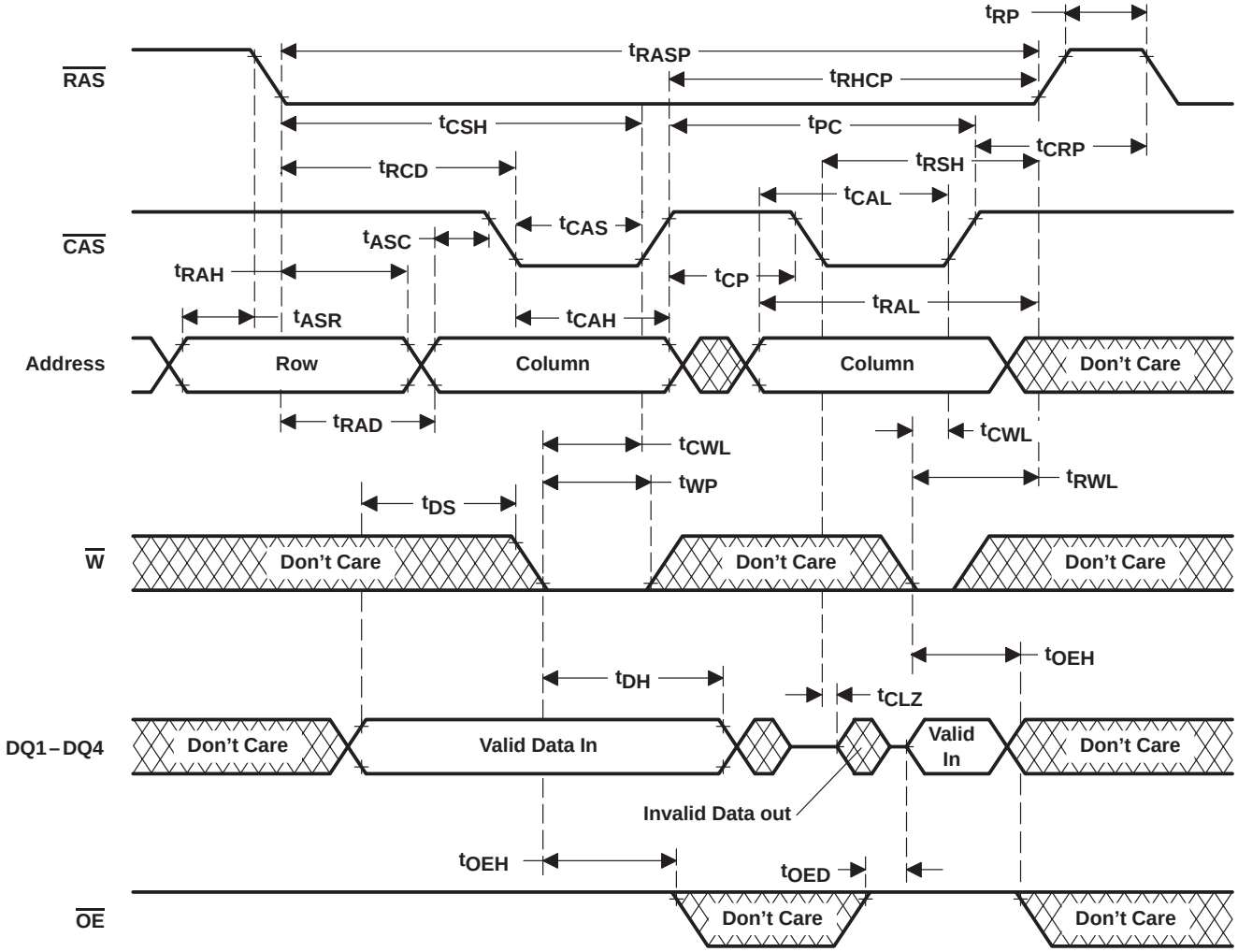
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}-, t_{CAC}-, or t_{AA}-dependent.
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

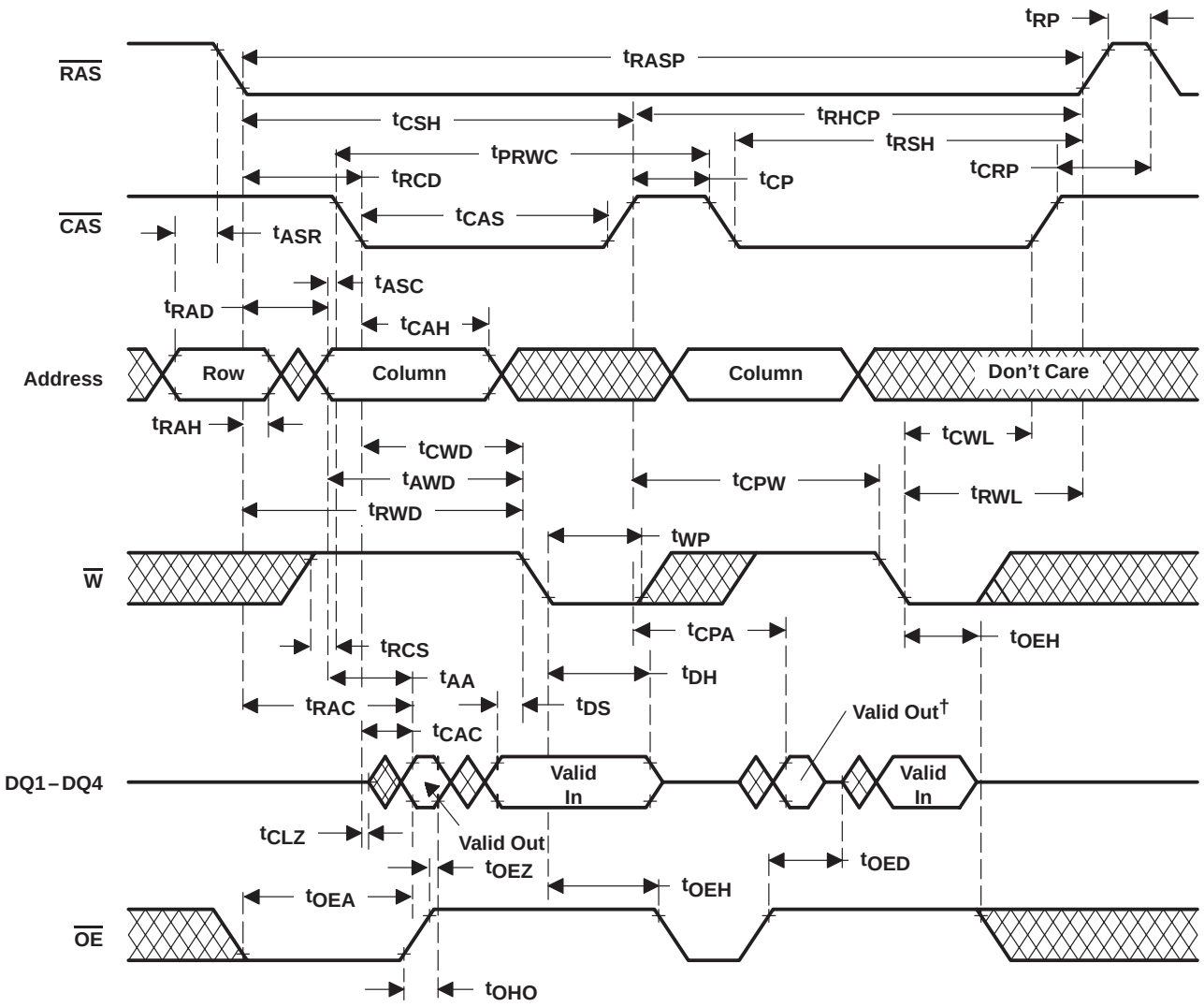
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

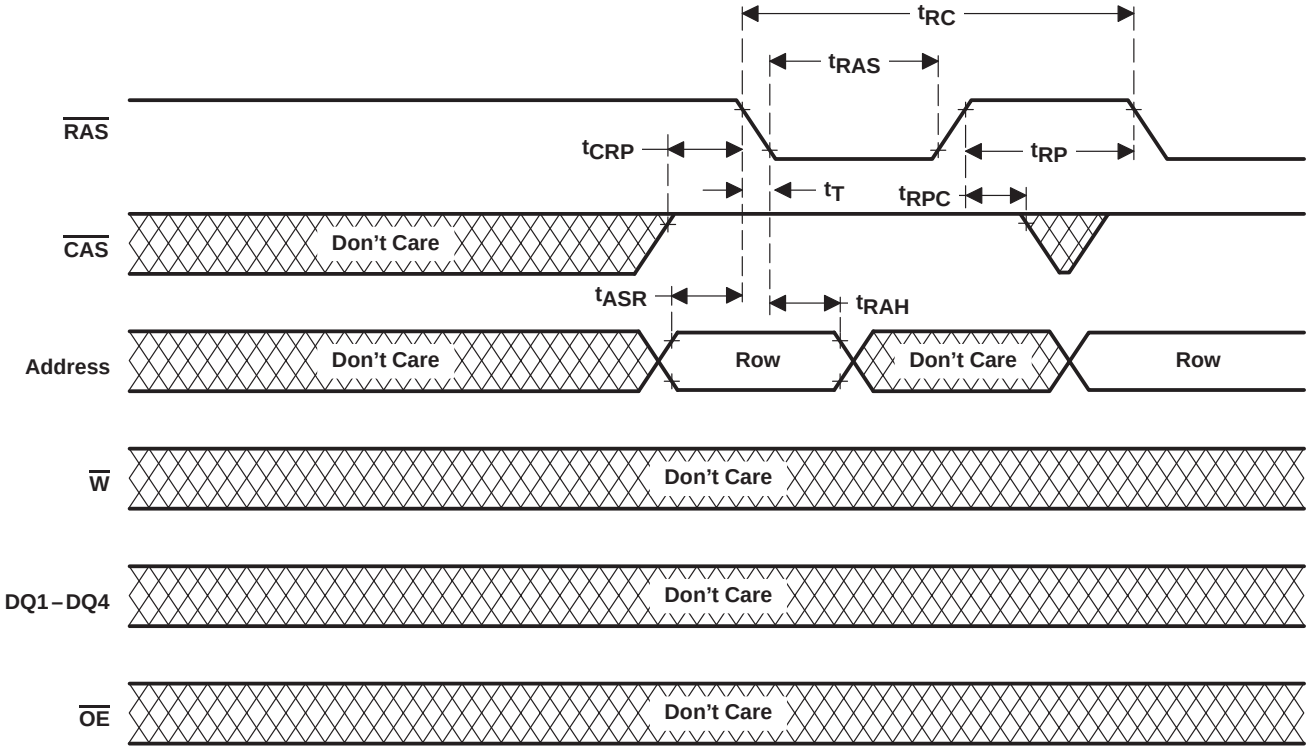


Figure 10. $\overline{\text{RAS}}$-Only Refresh Timing

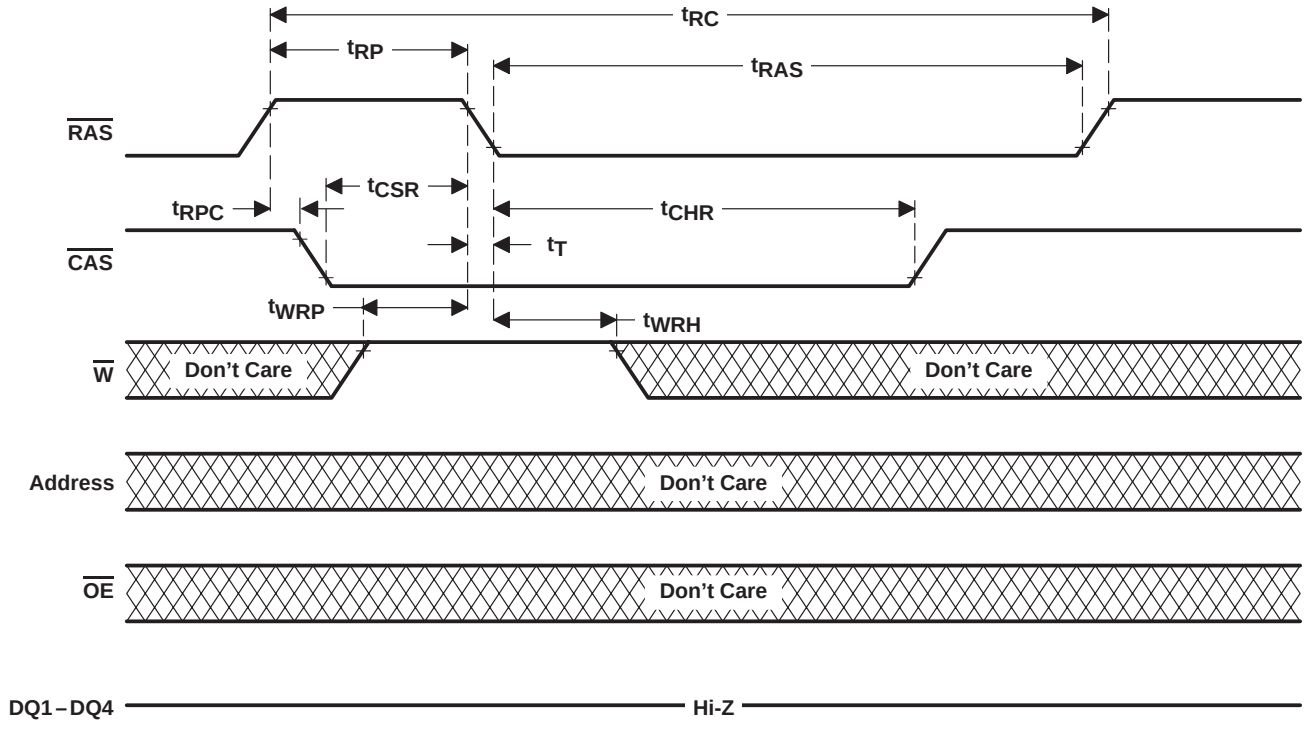


Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

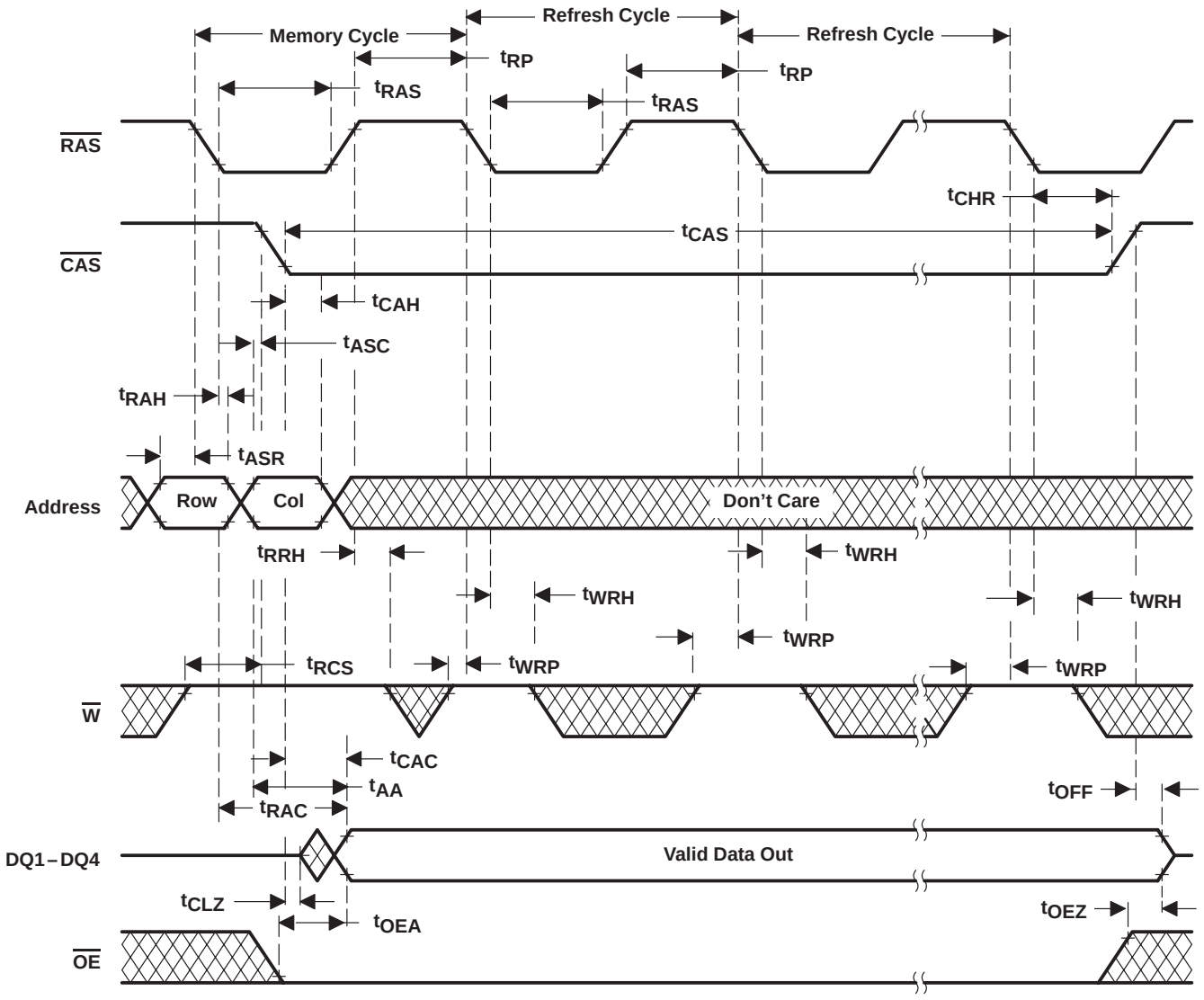


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

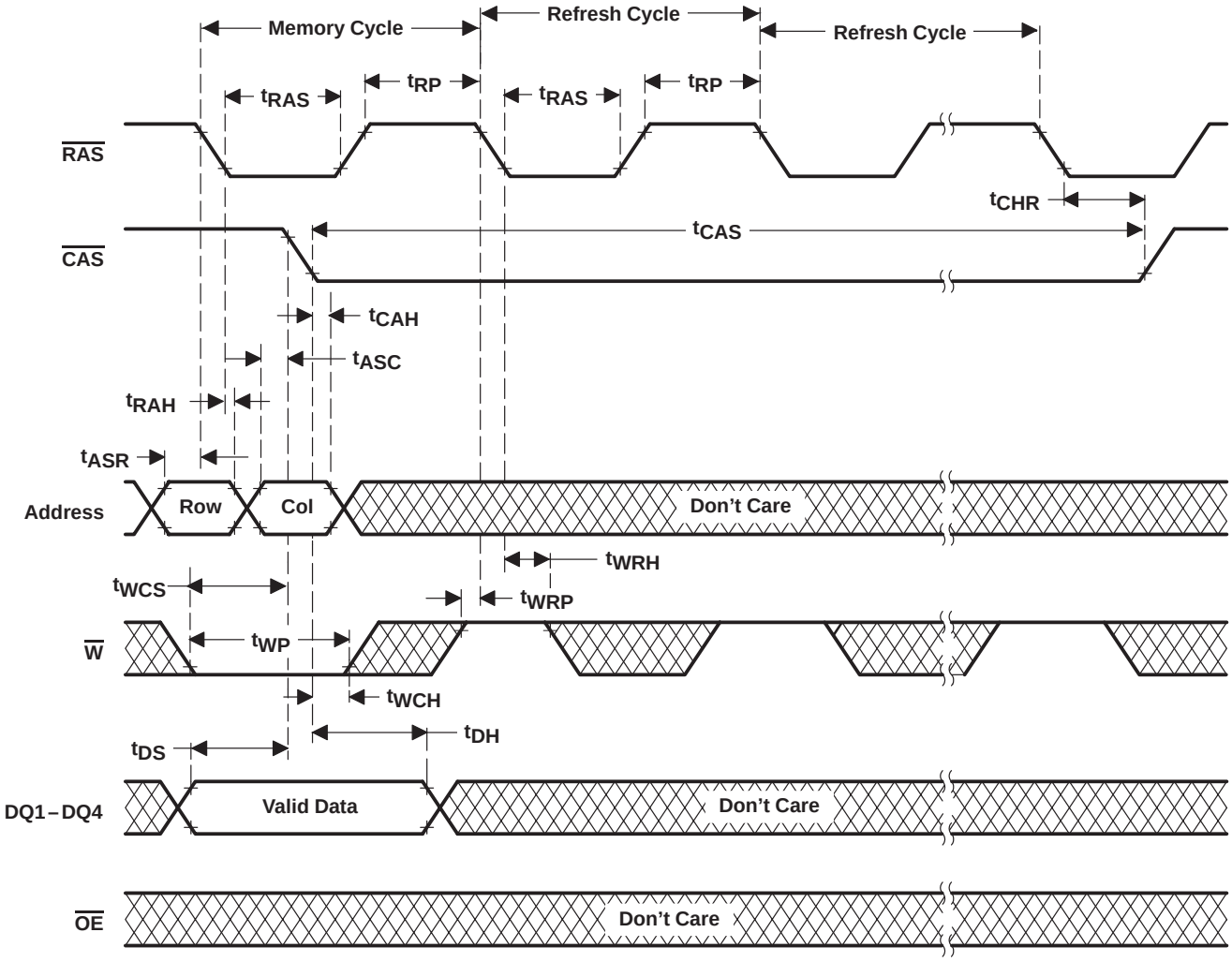


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

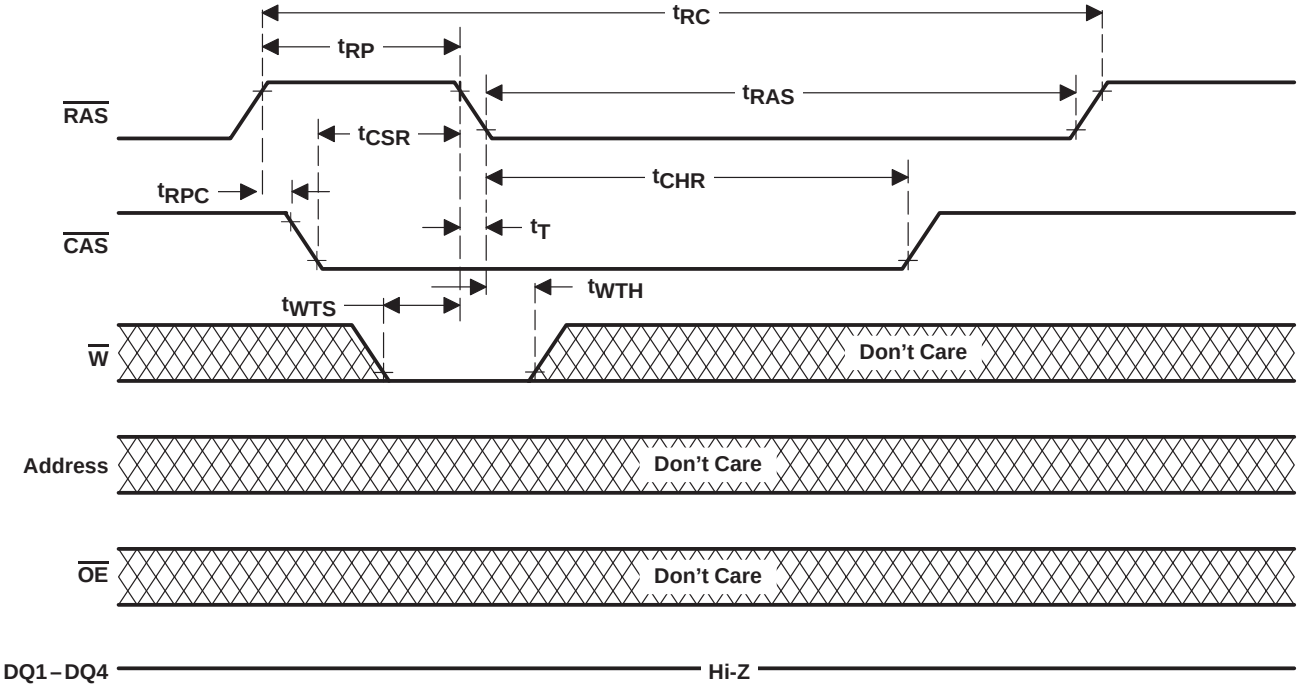


Figure 14. Test-Mode-Entry-Cycle Timing

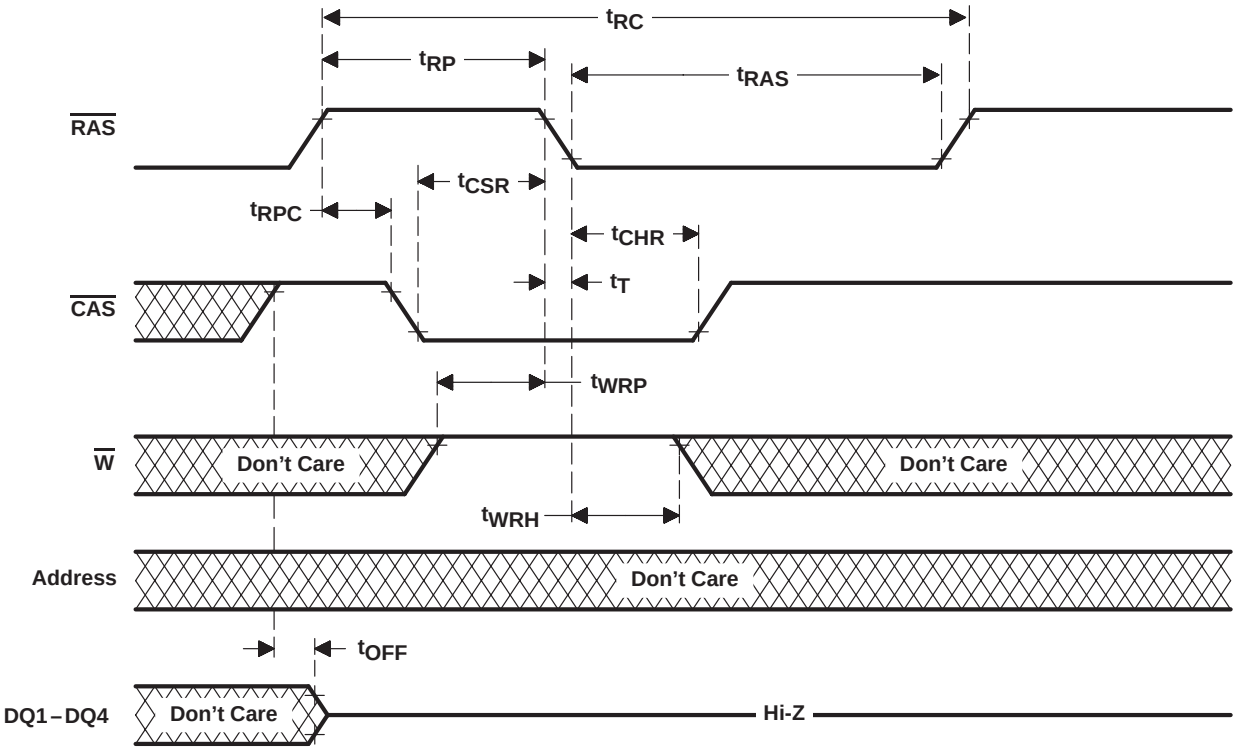
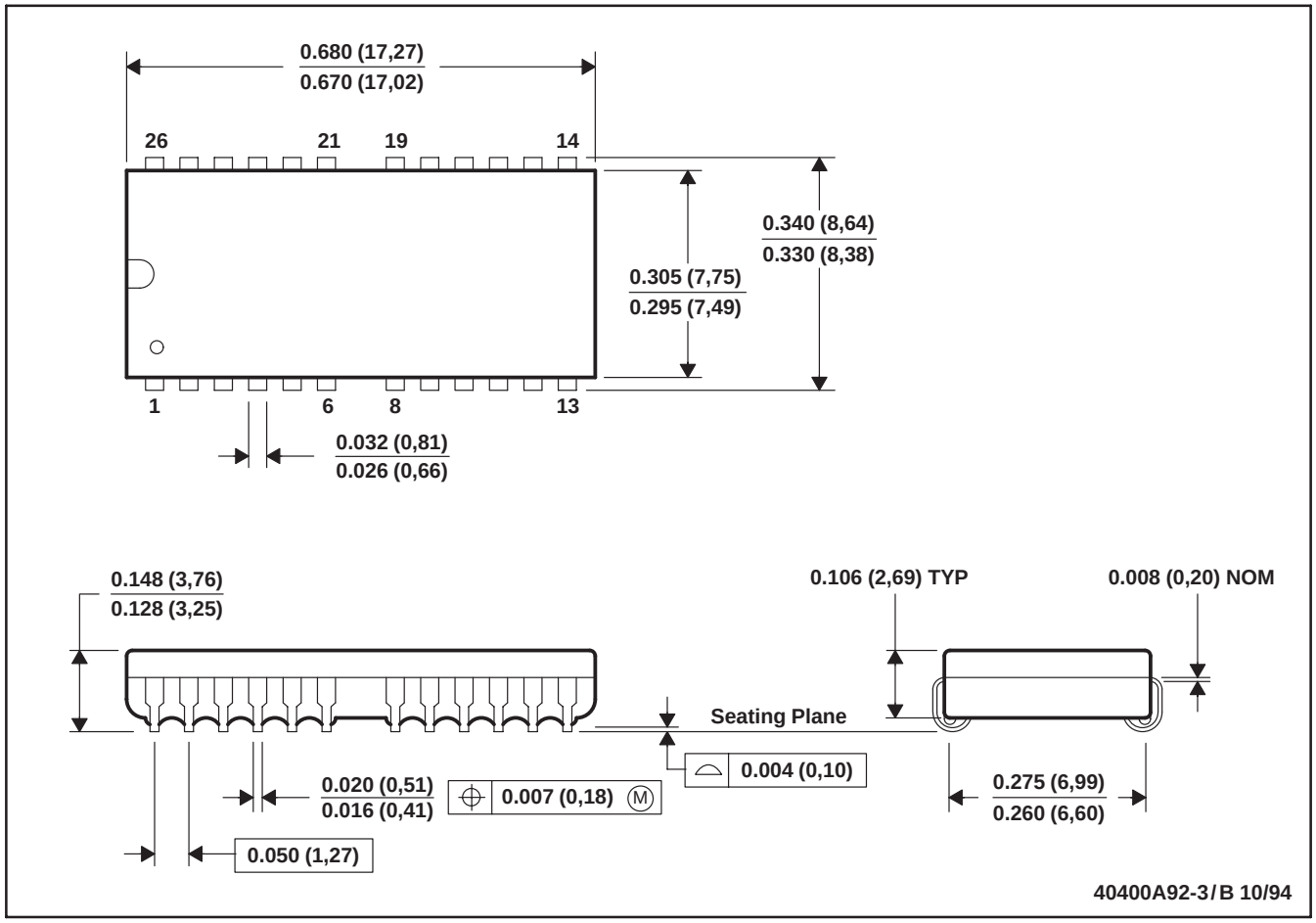


Figure 15. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing

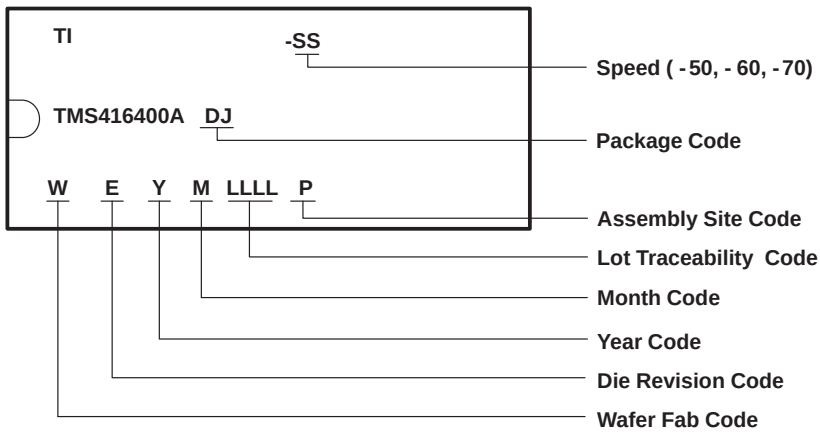
MECHANICAL DATA

DJ (R-PDSO-J24/26) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization (TMS416400A illustrated)



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