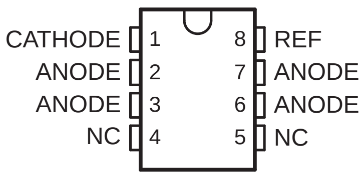
FEATURES

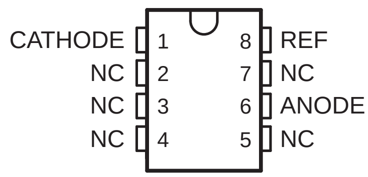
- **0.4% Initial Voltage Tolerance**
- **0.2-Ω Typical Output Impedance**
- **Fast Turnon…500 ns**
- **Sink Current Capability…1 mA to 100 mA**
- **Low Reference Current (REF)**
- **Adjustable Output Voltage…$V_{I(ref)}$ to 36 V**

D PACKAGE
(TOP VIEW)



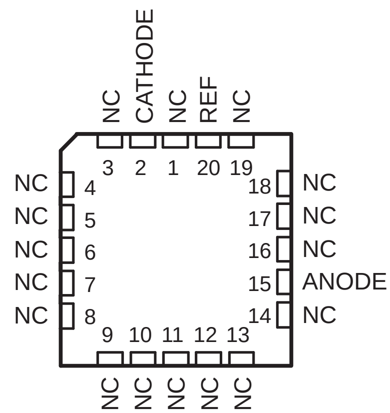
NC – No internal connection
ANODE terminals are connected internally

JG OR PW PACKAGE
(TOP VIEW)

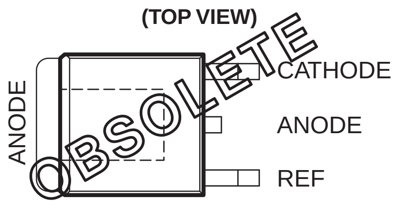


NC – No internal connection

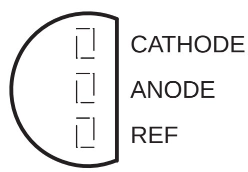
FK PACKAGE
(TOP VIEW)



KTP PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TL1431 is a precision programmable reference with specified thermal stability over automotive, commercial, and military temperature ranges. The output voltage can be set to any value between $V_{I(ref)}$ (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). This device has a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TL1431Q is characterized for operation over the full automotive temperature range of –40°C to 125°C. The TL1431M is characterized for operation over the full military temperature range of –55°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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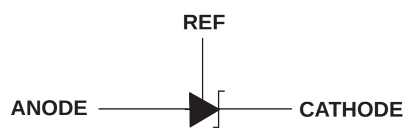
ORDERING INFORMATION[1]

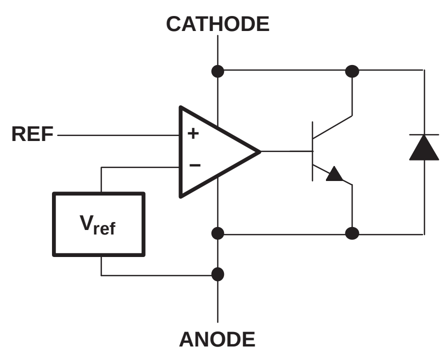
T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PowerFLEX™ – KTP	Reel of 3000	TL1431CKTPR	OBSOLETE
	SOIC – D	Tube of 75	TL1431CD	1431C
		Reel of 2500	TL1431CDR	
	TO-226 / TO-92 – LP	Bulk of 1000	TL1431CLP	TL1431C
		Reel of 2000	TL1431CLPR	
	TSSOP – PW	Tube of 150	TL1431CPW	T1431
		Reel of 2000	TL1431CPWR	
–40°C to 125°C	SOIC – D	Tube of 75	TL1431QD	TL1431QD
		Reel of 2500	TL1431QDR	
	TSSOP – PW	Tube of 150	TL1431QPW	T1431QPW
		Reel of 2000	TL1431QPWR	
–55°C to 125°C	CDIP – JG	Tube of 50	TL1431MJG	TL1431MJG
	LCCC – FK	Tube of 55	TL1431MFK	TL1431MFK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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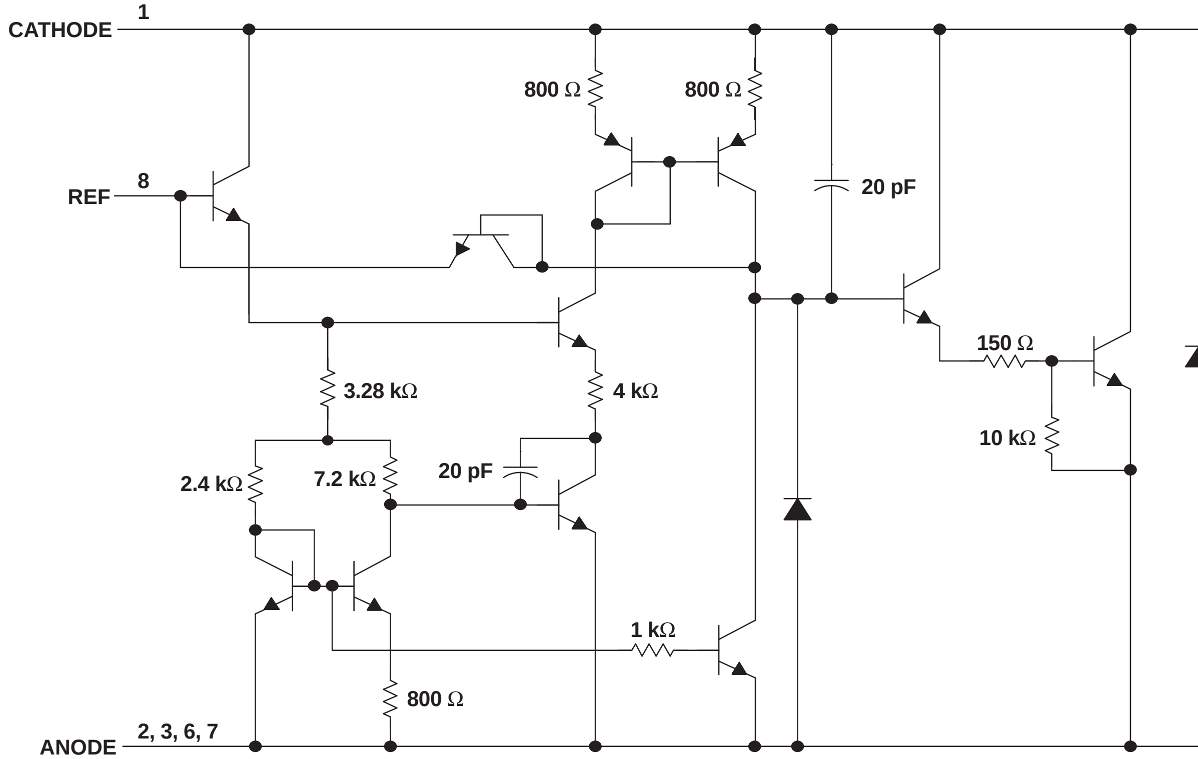
EQUIVALENT SCHEMATIC



A. All component values are nominal.

B. Pin numbers shown are for the D package.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage(2)			37	V
I_{KA}	Continuous cathode current range		–100	150	mA
$I_{I(ref)}$	Reference input current range		–0.05	10	mA
θ_{JA}	Package thermal impedance(3)(4)	D package		97	°C/W
		LP package		140	
		PW package		149	
θ_{JC}	Package thermal impedance(5)(6)	FK package		5.61	°C/W
		JG package		14.5	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature	1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.
(3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_{J(max)} - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with MIL-STD-883.

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Recommended Operating Conditions

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		$V_{I(ref)}$	36	V
I_{KA}	Cathode current		1	100	mA
T_A	Operating free-air temperature	TL1431C	0	70	°C
		TL1431Q	–40	125	
		TL1431M	–55	125	

Electrical Characteristics

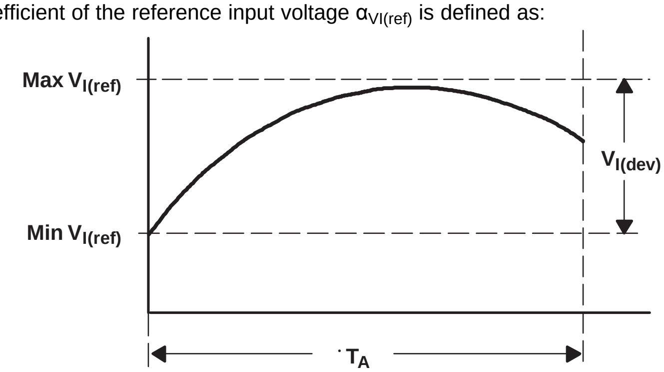
at specified free-air temperature, I_{KA} = 10 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TEST CIRCUIT	TL1431C MIN	TL1431C TYP	TL1431C MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$	25°C	Figure 1	2490	2500	2510	mV
			Full range		2480		2520	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (2)	$V_{KA} = V_{I(ref)}$	Full range	Figure 1		4	20	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	Full range	Figure 2		–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞	25°C	Figure 2		1.5	2.5	μA
			Full range				3	
$I_{I(dev)}$	Deviation of reference input current over full temperature range (2)	R1 = 10 kΩ, R2 = ∞	Full range	Figure 2		0.2	1.2	μA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$	25°C	Figure 1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0	25°C	Figure 3		0.18	0.5	μA
			Full range				2	
$\lvert z_{KA}\rvert$	Output impedance (3)	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA	25°C	Figure 1		0.2	0.4	Ω

(1) Full range is 0°C to 70°C for C-suffix devices.
(2) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right|\left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)}\ \text{at}\ 25^\circ C}\right)\times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(3) The output impedance is defined as: $\left|z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $\left|z'\right| = \frac{\Delta V}{\Delta I}$,

which is approximately equal to $\left|z_{KA}\right|\left(1 + \frac{R1}{R2}\right)$.

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Electrical Characteristics

at specified free-air temperature, I_{KA} = 10 mA (unless otherwise noted)

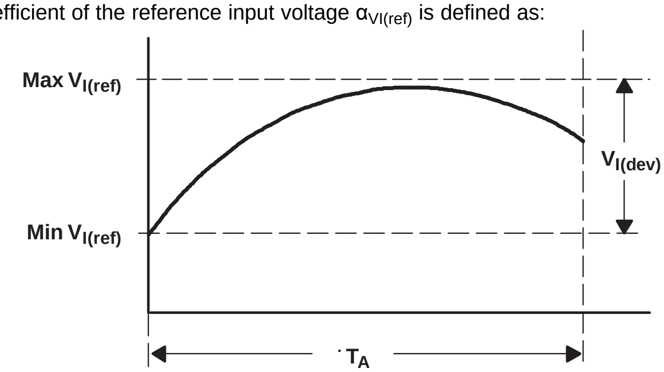
PARAMETER		TEST CONDITIONS	T_A (1)	TEST CIRCUIT	TL1431Q MIN	TL1431Q TYP	TL1431Q MAX	TL1431M MIN	TL1431M TYP	TL1431M MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$	25°C	Figure 1	2490	2500	2510	2475	2500	2540	mV
			Full range		2470		2530	2460		2550	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (2)	$V_{KA} = V_{I(ref)}$	Full range	Figure 1		17	55		17	55 (3)	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	Full range	Figure 2		–1.1	–2		–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10 kΩ, R2 = ∞	25°C	Figure 2		1.5	2.5		1.5	2.5	µA
			Full range				4			5	
$I_{I(dev)}$	Deviation of reference input current over full temperature range (2)	R1 = 10 kΩ, R2 = ∞	Full range	Figure 2		0.5	2		0.5	3 (3)	µA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$	25°C	Figure 1		0.45	1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, $V_{I(ref)}$ = 0	25°C	Figure 3		0.18	0.5		0.18	0.5	µA
			Full range				2			2	
$\|z_{KA}\|$	Output impedance (4)	$V_{KA} = V_{I(ref)}$, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA	25°C	Figure 1		0.2	0.4		0.2	0.4	Ω

(1) Full range is –40°C to 125°C for Q-suffix devices and –55°C to 125°C for M-suffix devices.

(2) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{VI(ref)}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)} \text{ at } 25°C}\right) \times 10^6}{\Delta T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

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PARAMETER MEASUREMENT INFORMATION

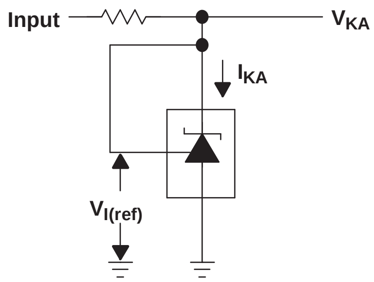

Figure 1. Test Circuit for $V_{(KA)} = V_{ref}$

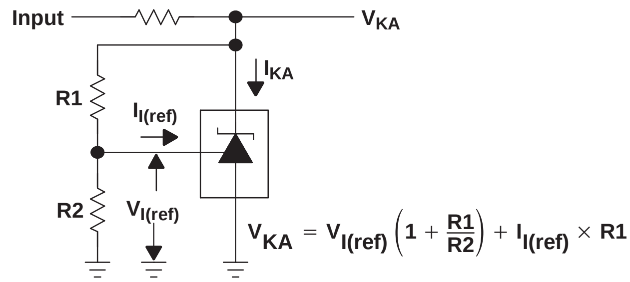

Figure 2. Test Circuit for $V_{(KA)} > V_{ref}$

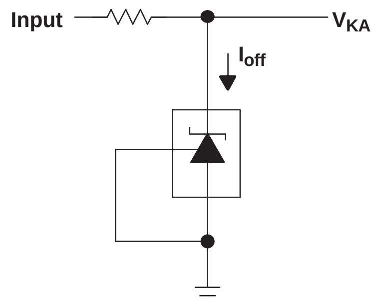

Figure 3. Test Circuit for I_{off}

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

Table of Graphs

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Reference voltage vs Free-air temperature	4
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Reference impedance vs Frequency	13
Pulse response	14
Stability boundary conditions	15

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REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

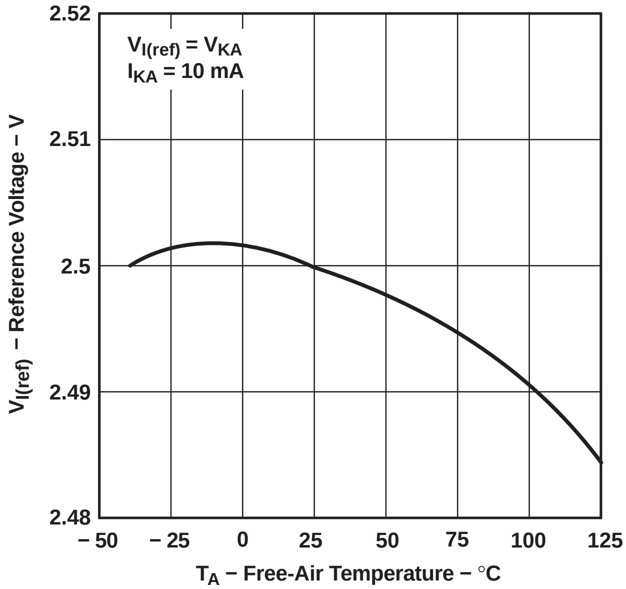

Figure 4.

REFERENCE CURRENT
vs
FREE-AIR TEMPERATURE

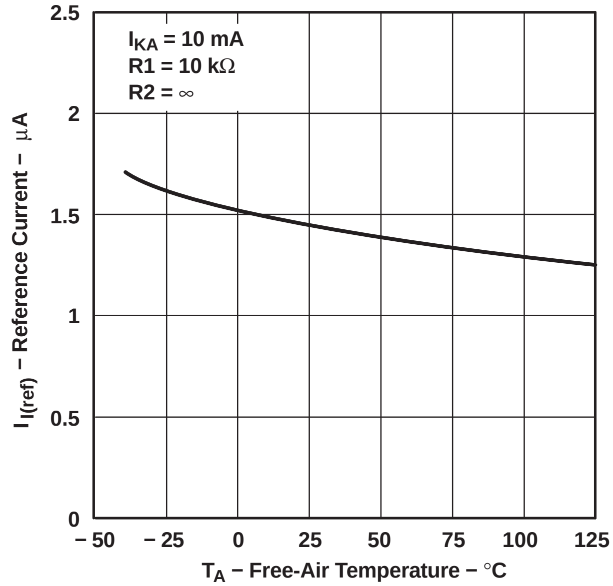

Figure 5.

CATHODE CURRENT
vs
CATHODE VOLTAGE

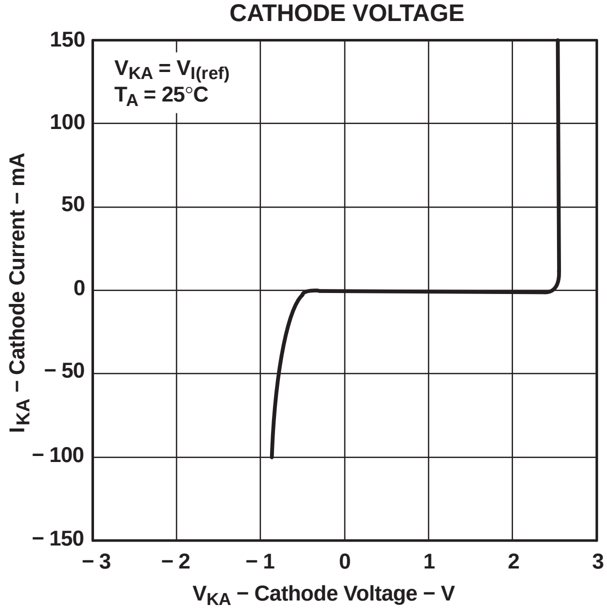

Figure 6.

CATHODE CURRENT
vs
CATHODE VOLTAGE

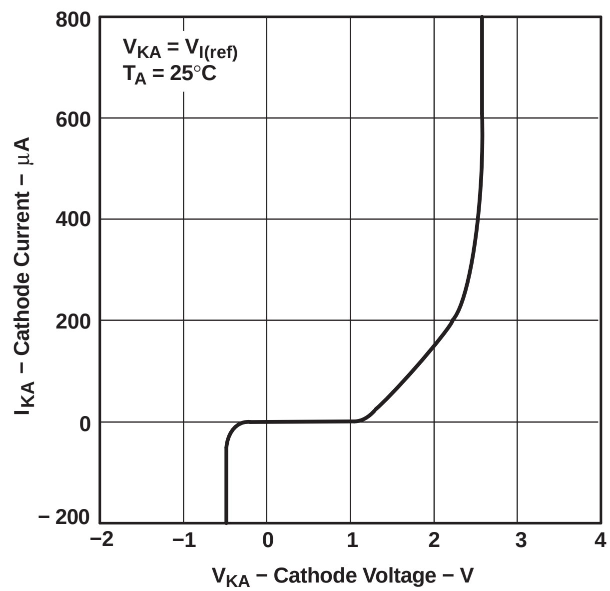

Figure 7.

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OFF-STATE CATHODE CURRENT vs FREE-AIR TEMPERATURE

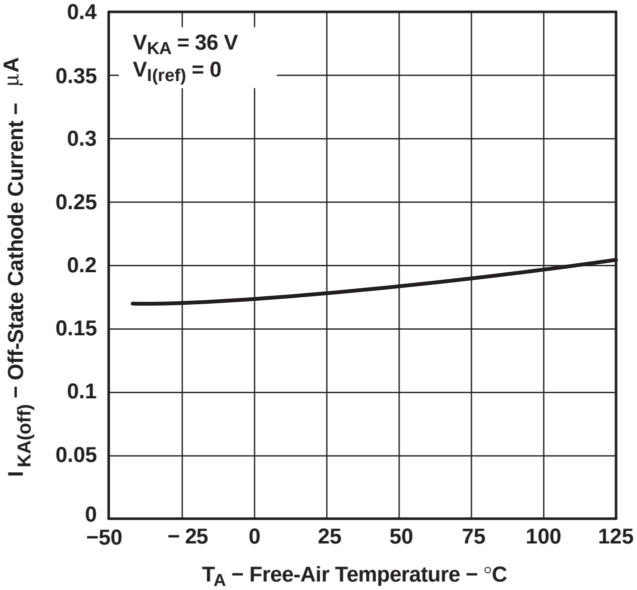

Figure 8.

RATIO OF DELTA REFERENCE VOLTAGE TO DELTA CATHODE VOLTAGE vs FREE-AIR TEMPERATURE

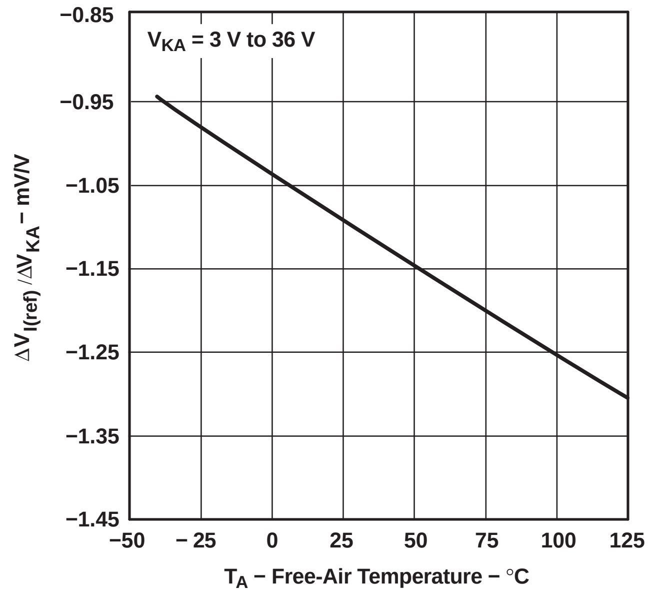

Figure 9.

EQUIVALENT INPUT-NOISE VOLTAGE vs FREQUENCY

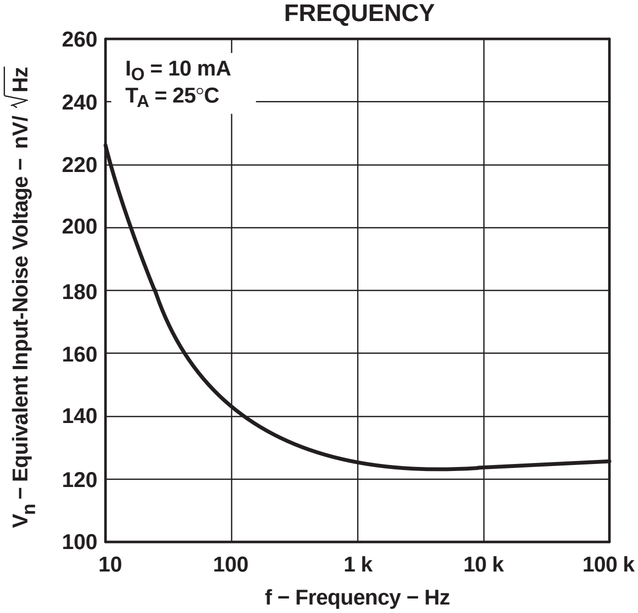

Figure 10.

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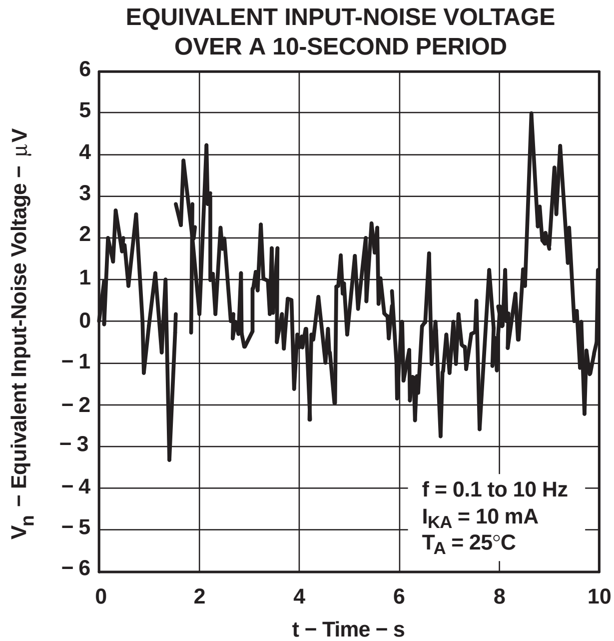

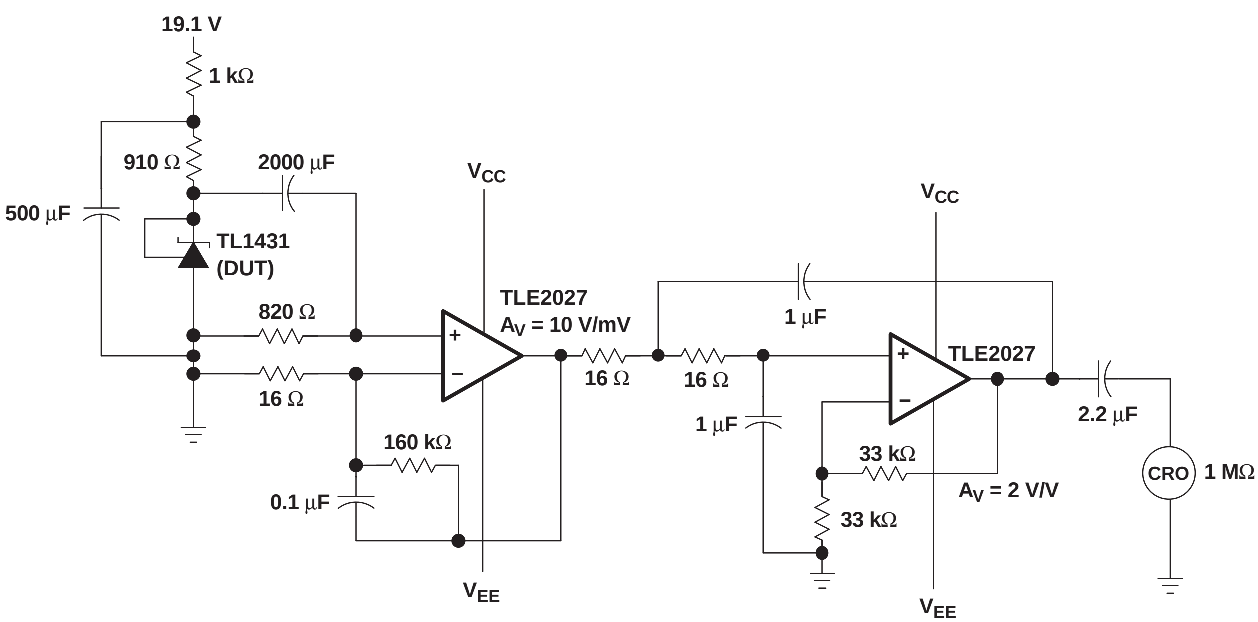

TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT INPUT-NOISE VOLTAGE
Figure 11.

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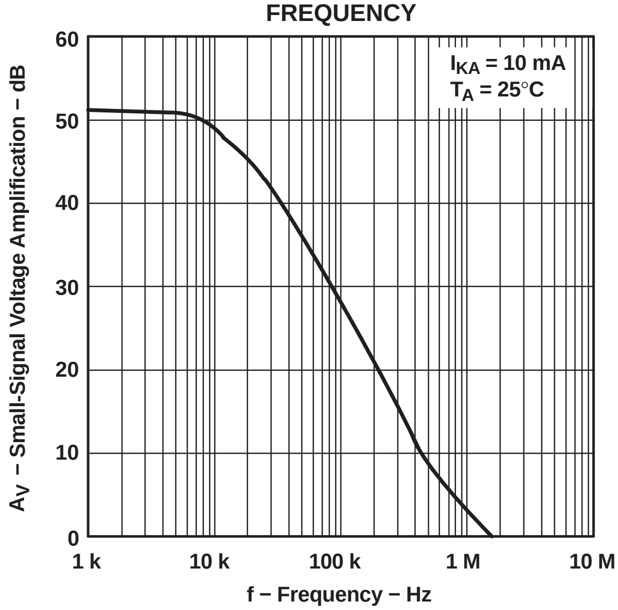
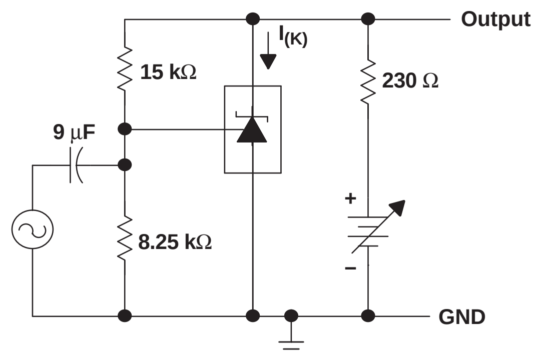
SMALL-SIGNAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

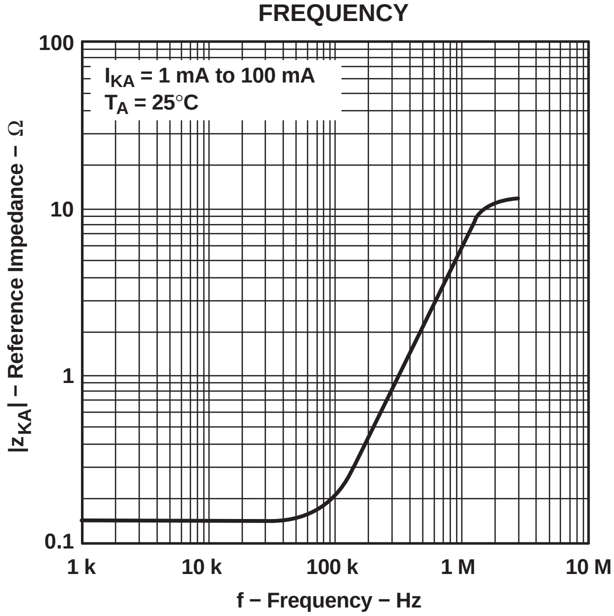


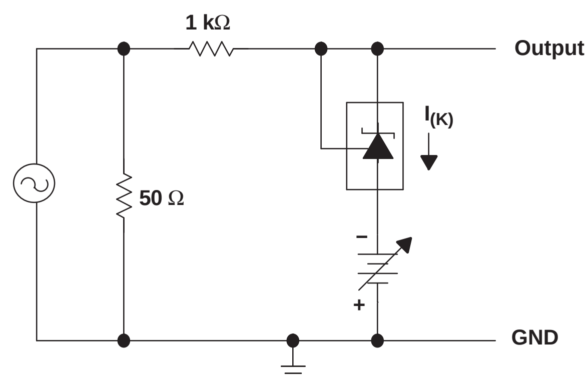


TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

Figure 12.

REFERENCE IMPEDANCE
vs
FREQUENCY





TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 13.

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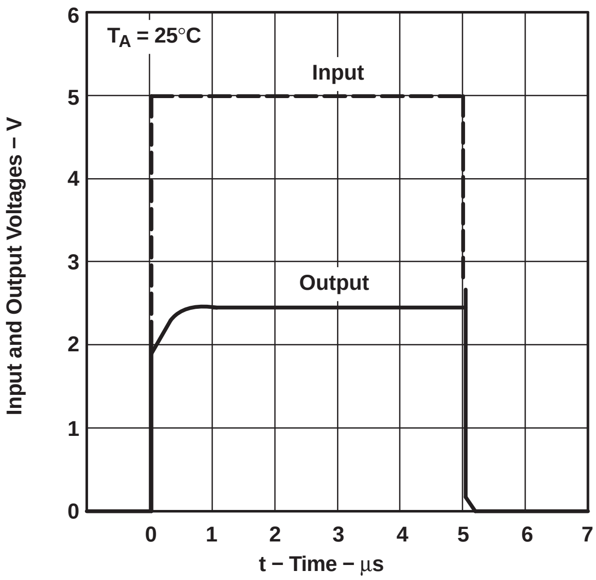
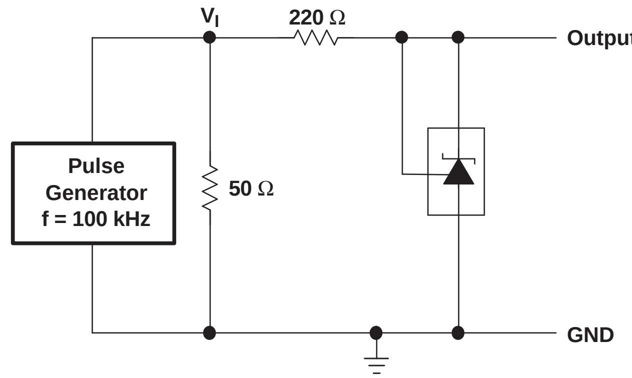
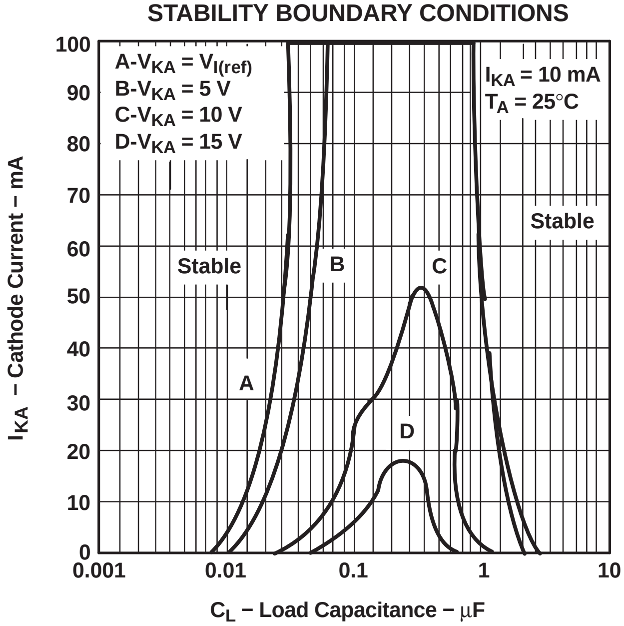
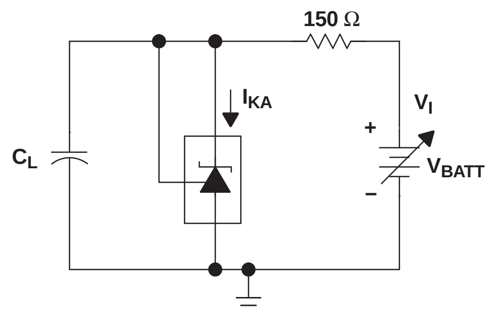




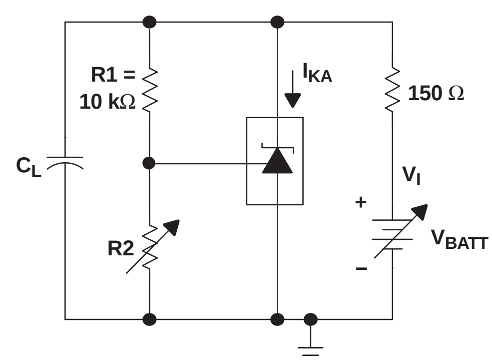
TEST CIRCUIT FOR PULSE RESPONSE

Figure 14.





TEST CIRCUIT FOR CURVE A



TEST CIRCUIT FOR CURVES B, C, AND D

A. The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 15.

APPLICATION INFORMATION

Table of Application Circuits

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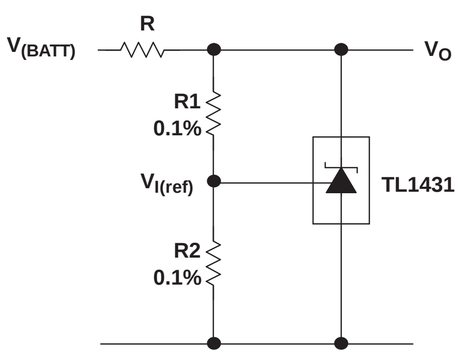

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

A. R should provide cathode current ≥1 mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 16. Shunt Regulator

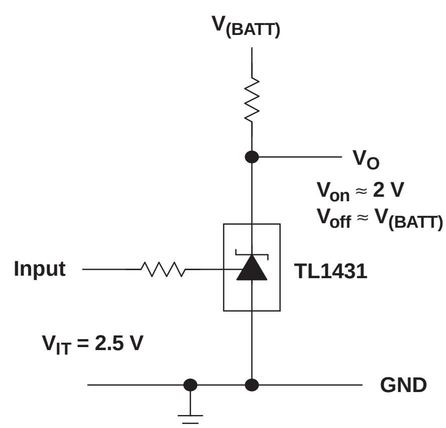

Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold

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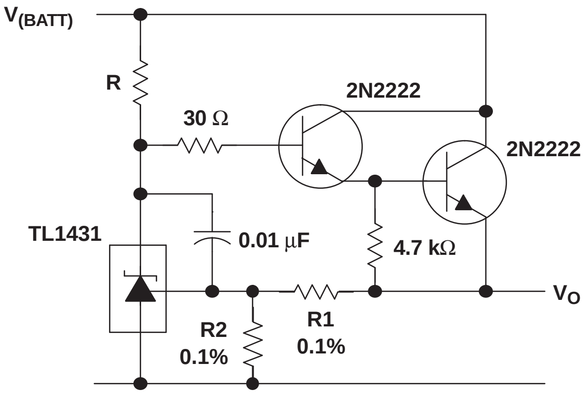
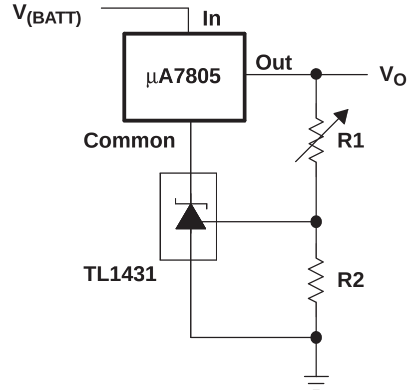


$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

A. R should provide cathode current ≥1 mA to the TL1431 at minimum $V_{(BATT)}$.

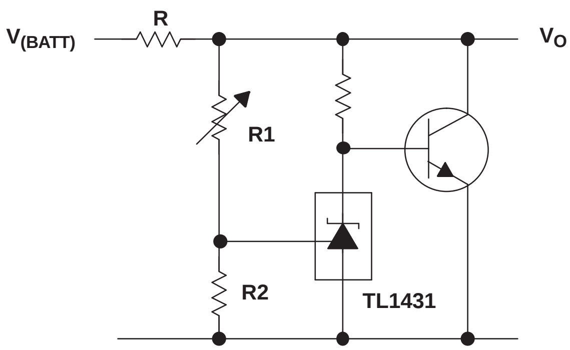
Figure 18. Precision High-Current Series Regulator



$$V = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

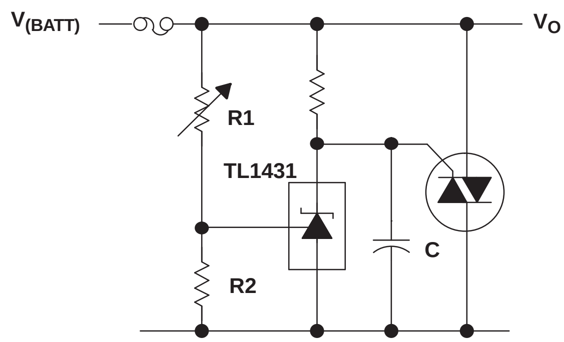
$$\text{Min } V = V_{I(ref)} + 5\ V$$

Figure 19. Output Control of a Three-Terminal Fixed Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

Figure 20. Higher-Current Shunt Regulator



$$V_{trip} = \left(1 + \frac{R1}{R2}\right) V_{I(ref)}$$

A. Refer to the stability boundary conditions in Figure 15 to determine allowable values for C.

Figure 21. Crowbar

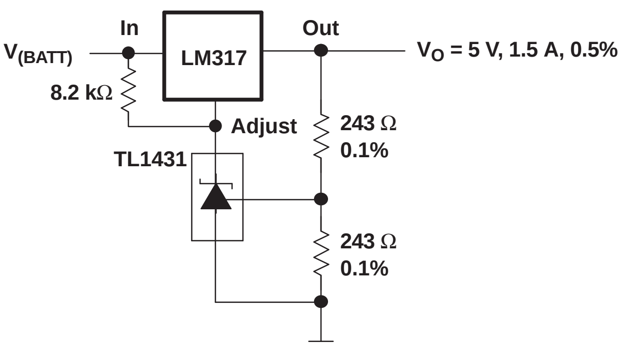
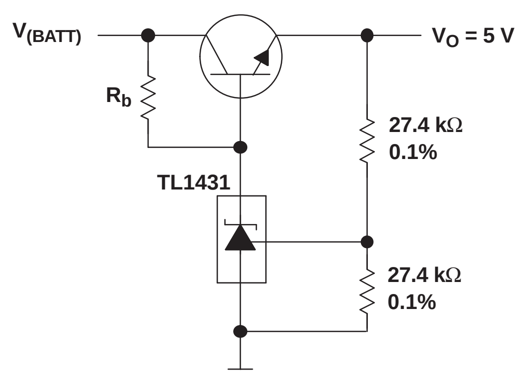


Figure 22. Precision 5-V, 1.5-A, 0.5% Regulator



A. R_b should provide cathode current ≥1 mA to the TL1431.

Figure 23. 5-V Precision Regulator

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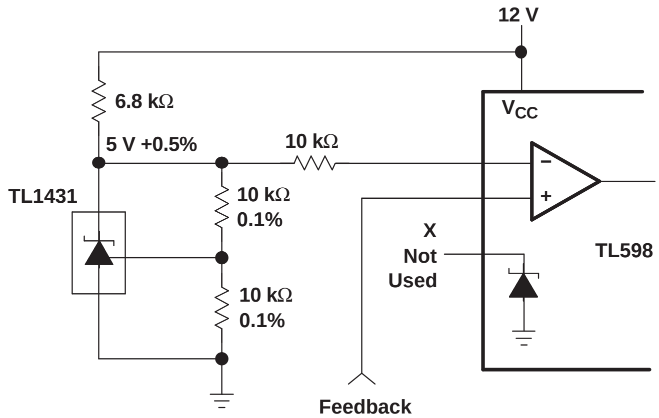
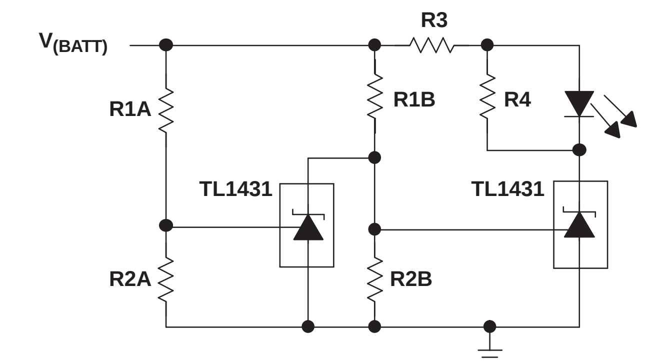


Figure 24. PWM Converter With 0.5% Reference



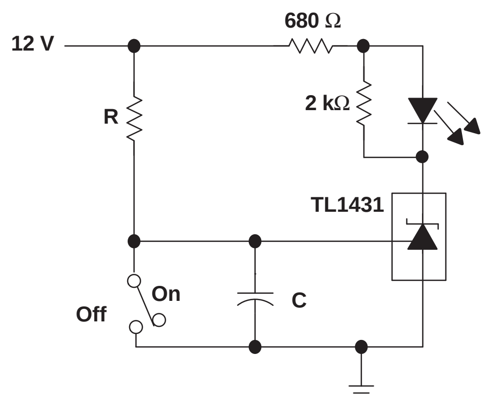
$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{I(ref)}$$

$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right) V_{I(ref)}$$

LED on When
Low Limit < $V_{(BATT)}$ < High Limit

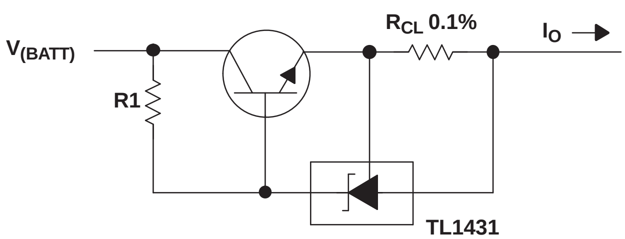
A. Select R3 and R4 to provide the desired LED intensity and cathode current ≥1 mA to the TL1431.

Figure 25. Voltage Monitor



$$\text{Delay} = R \times C \times l \frac{12\ V}{l\,(12\ V) - V_{I(ref)}}$$

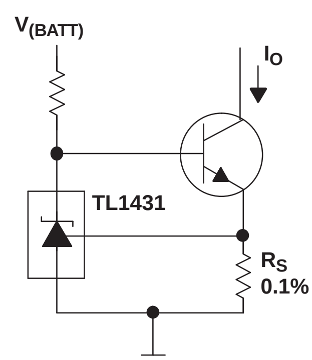
Figure 26. Delay Timer



$$I_O = \frac{V_{I(ref)}}{R_{CL}} + I_{KA}$$

$$R1 = \frac{V_{(BATT)}}{\left(\frac{I_O}{h_{FE}}\right) + I_{KA}}$$

Figure 27. Precision Current Limiter



$$I_O = \frac{V_{I(ref)}}{R_S}$$

Figure 28. Precision Constant-Current Sink

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9962001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9962001QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9962001VPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TL1431CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CKTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TL1431CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TL1431CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TL1431CLPM	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL1431CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TL1431CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TL1431CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL1431MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL1431MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TL1431MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TL1431QD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TL1431QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL1431QDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TL1431QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL1431QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL1431QLPR	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI
TL1431QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM
TL1431QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

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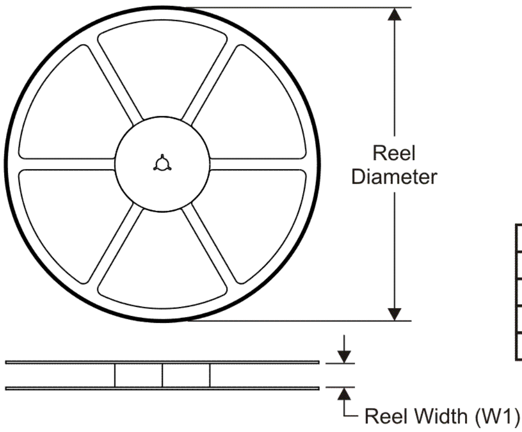
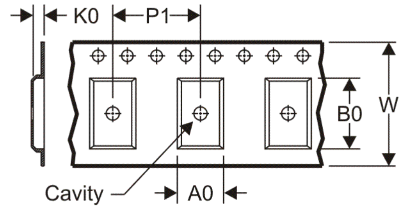
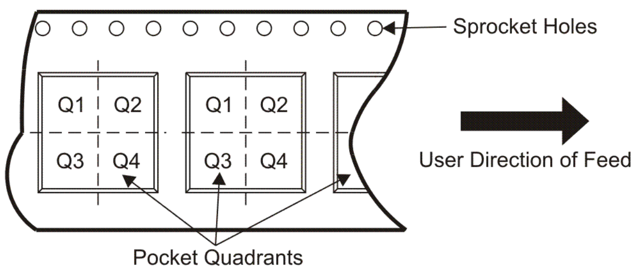


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

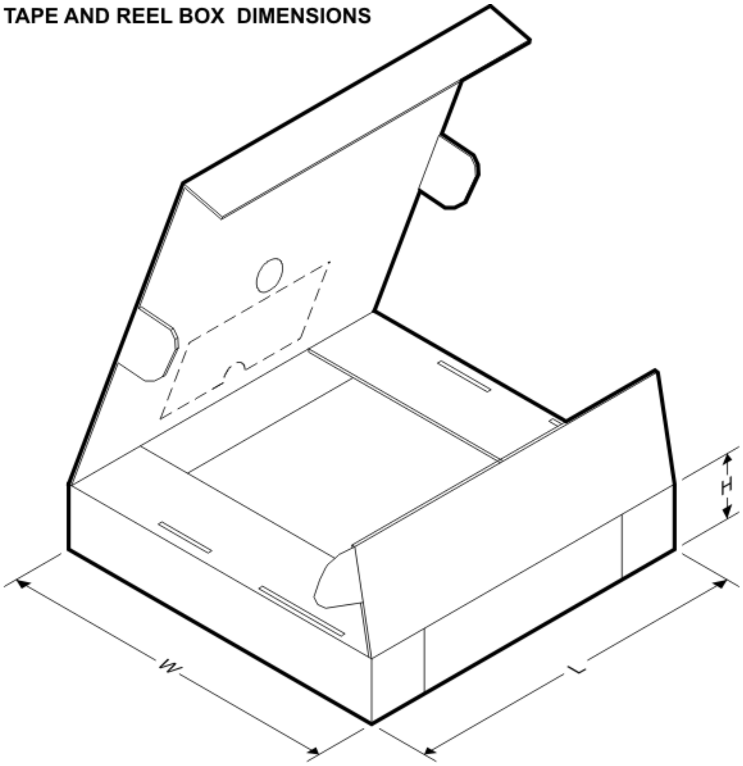
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1431CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

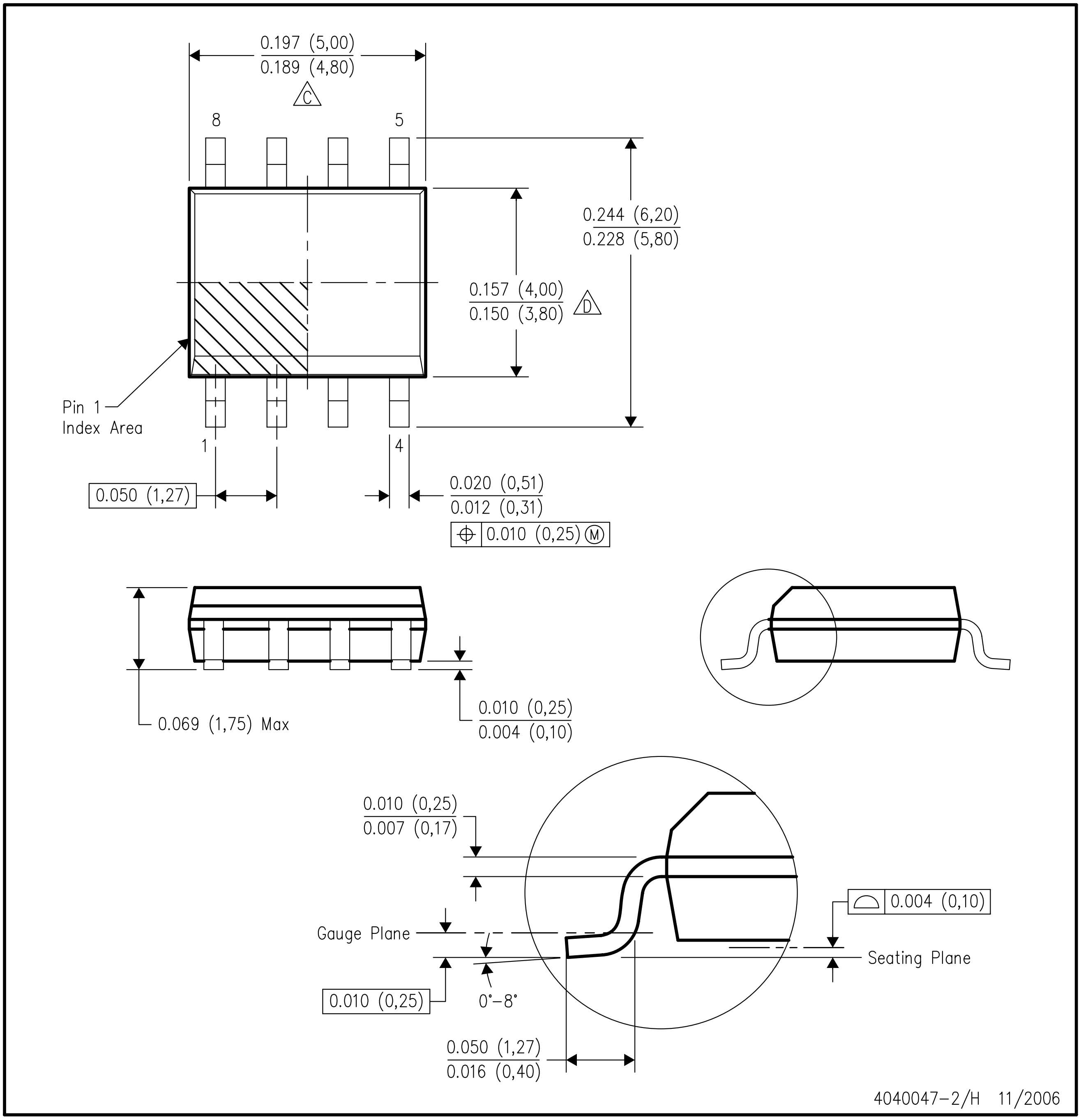
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1431CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL1431CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

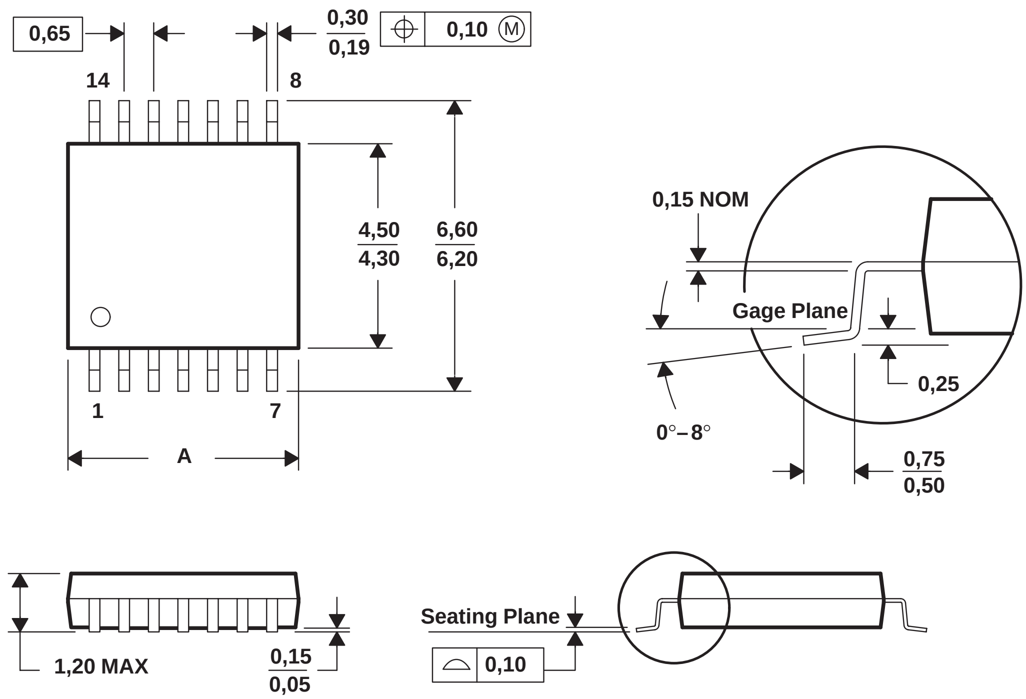
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



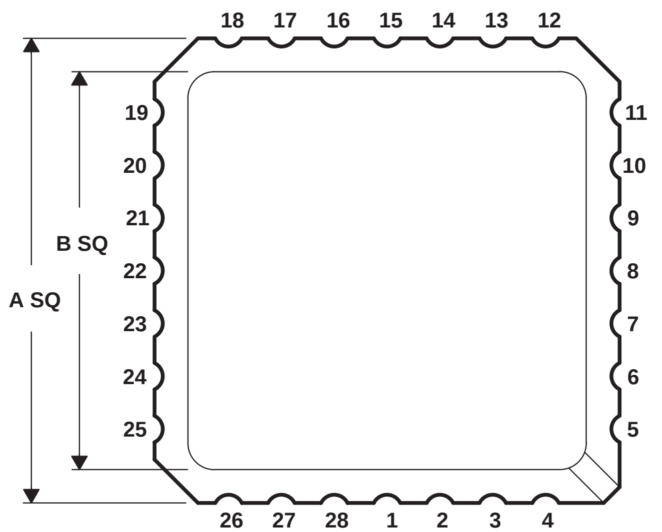
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

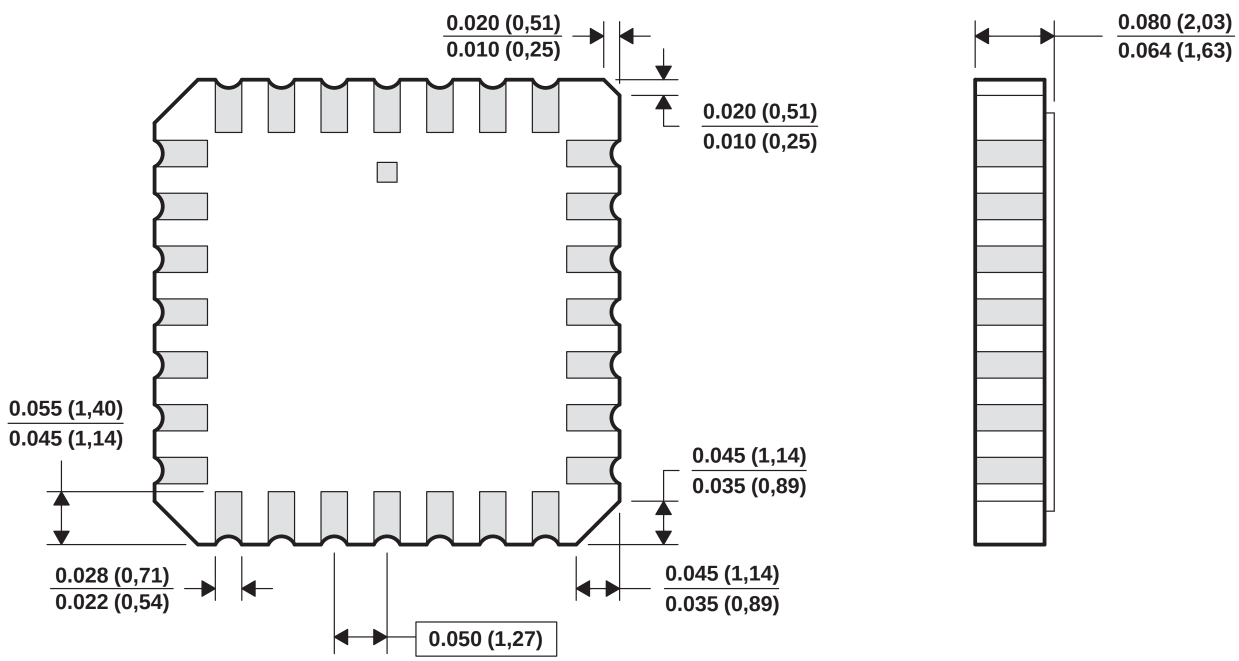
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



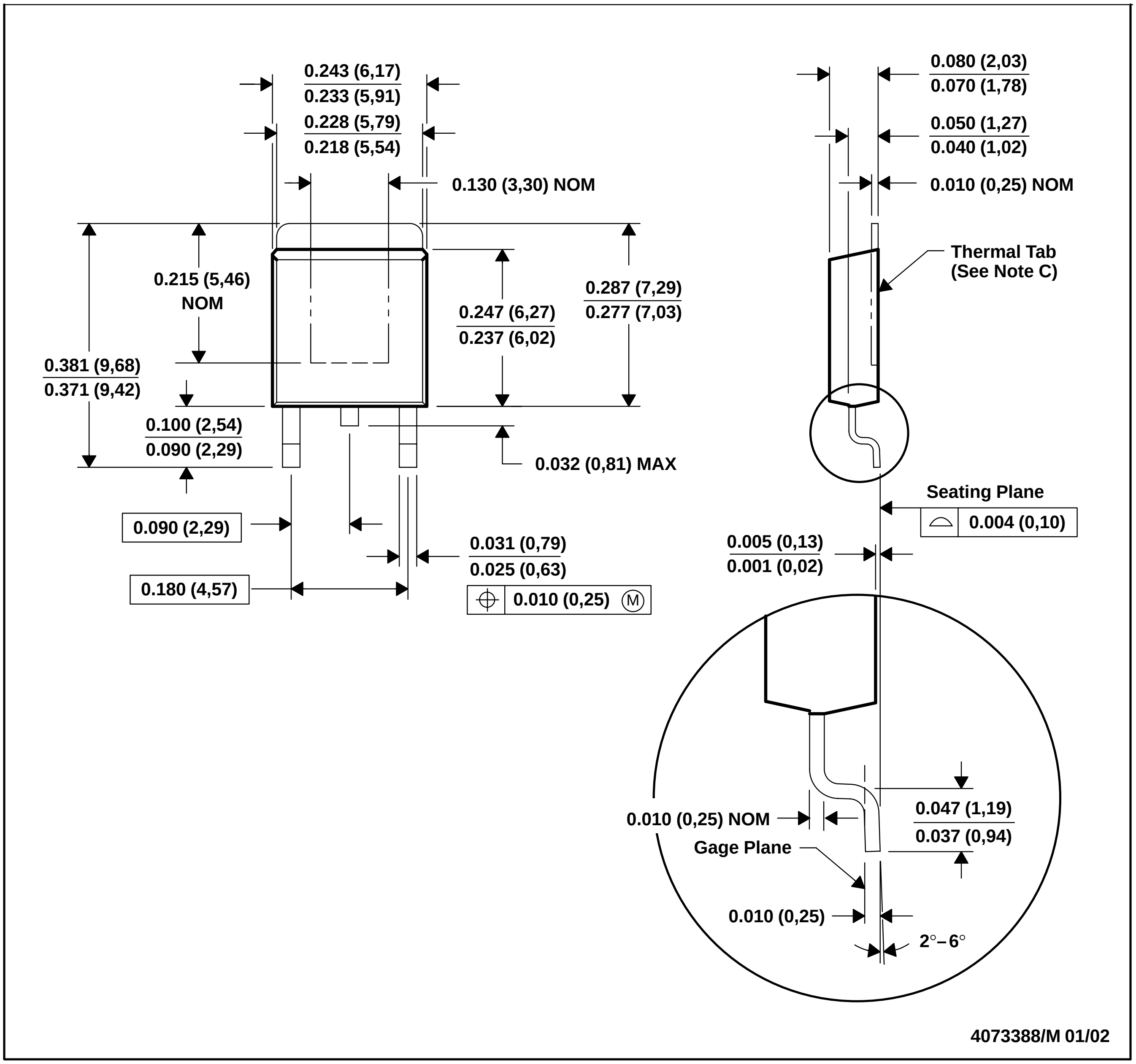
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

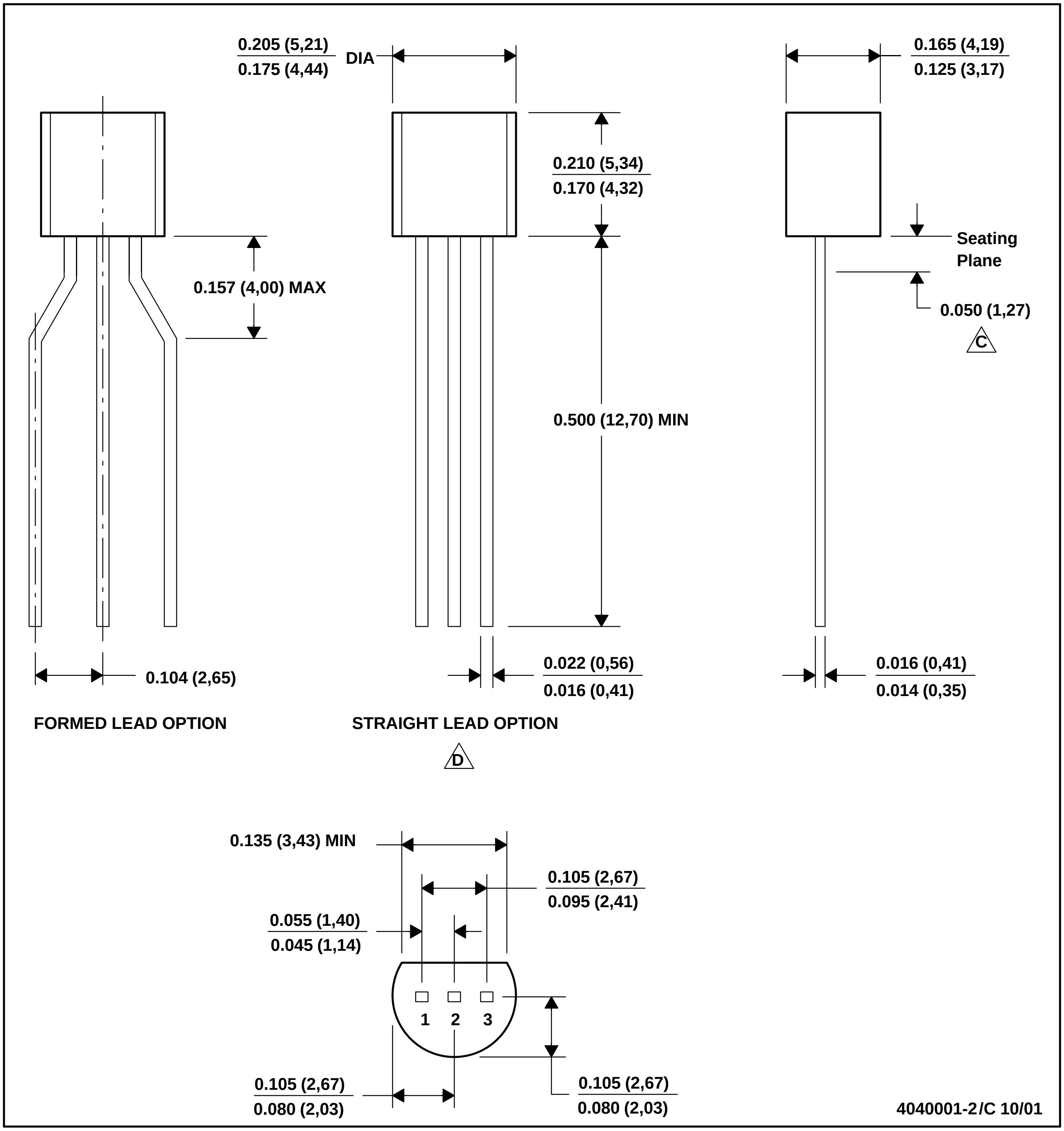
KTP (R-PSFM-G2) **PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC TO-252 variation AC.

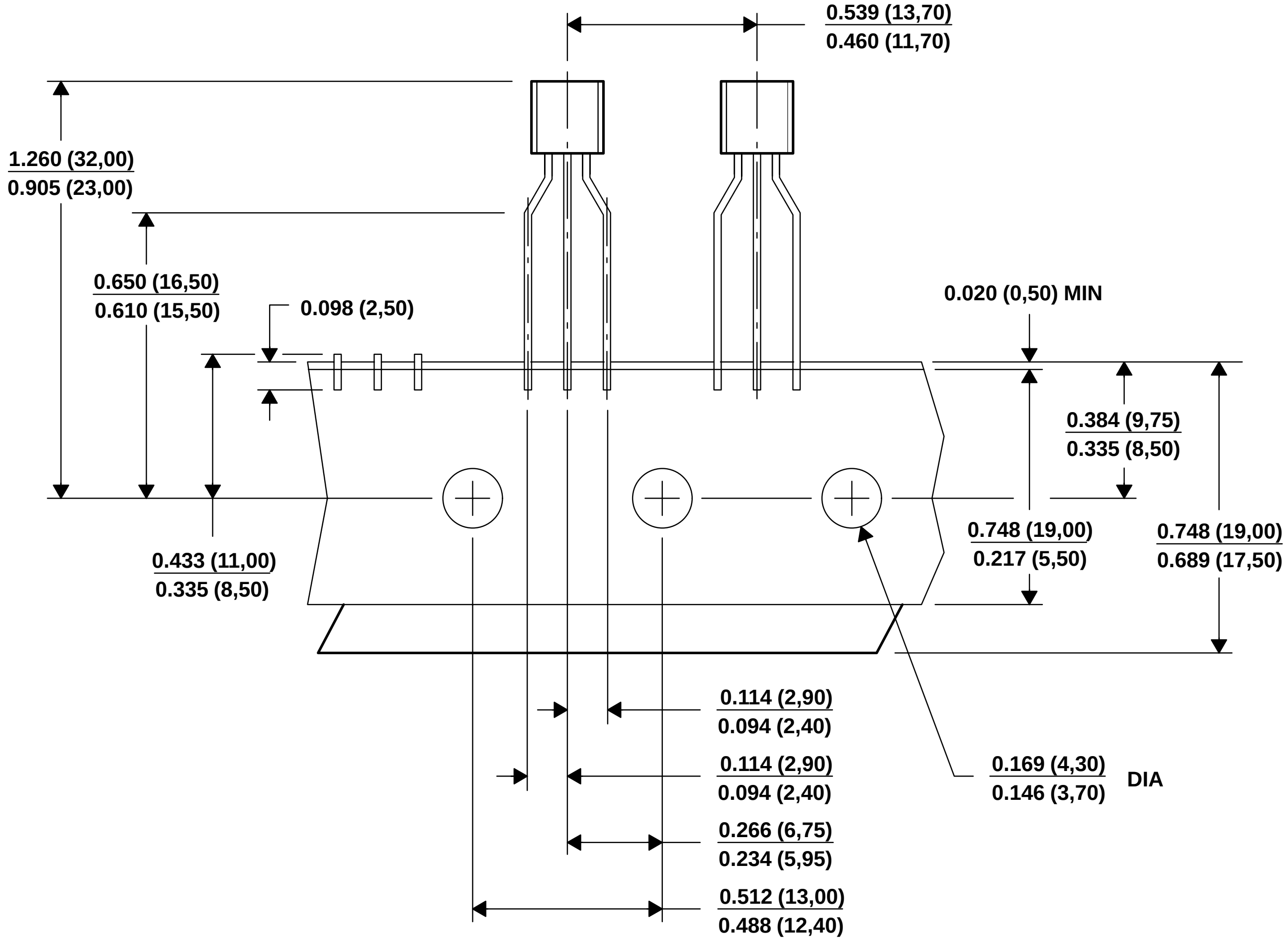
PowerFLEX is a trademark of Texas Instruments.

LP (O-PBCY-W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area
- D. FAlls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
- E. Shipping Method:
  - Straight lead option available in bulk pack only.
  - Formed lead option available in tape & reel or ammo pack.

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**

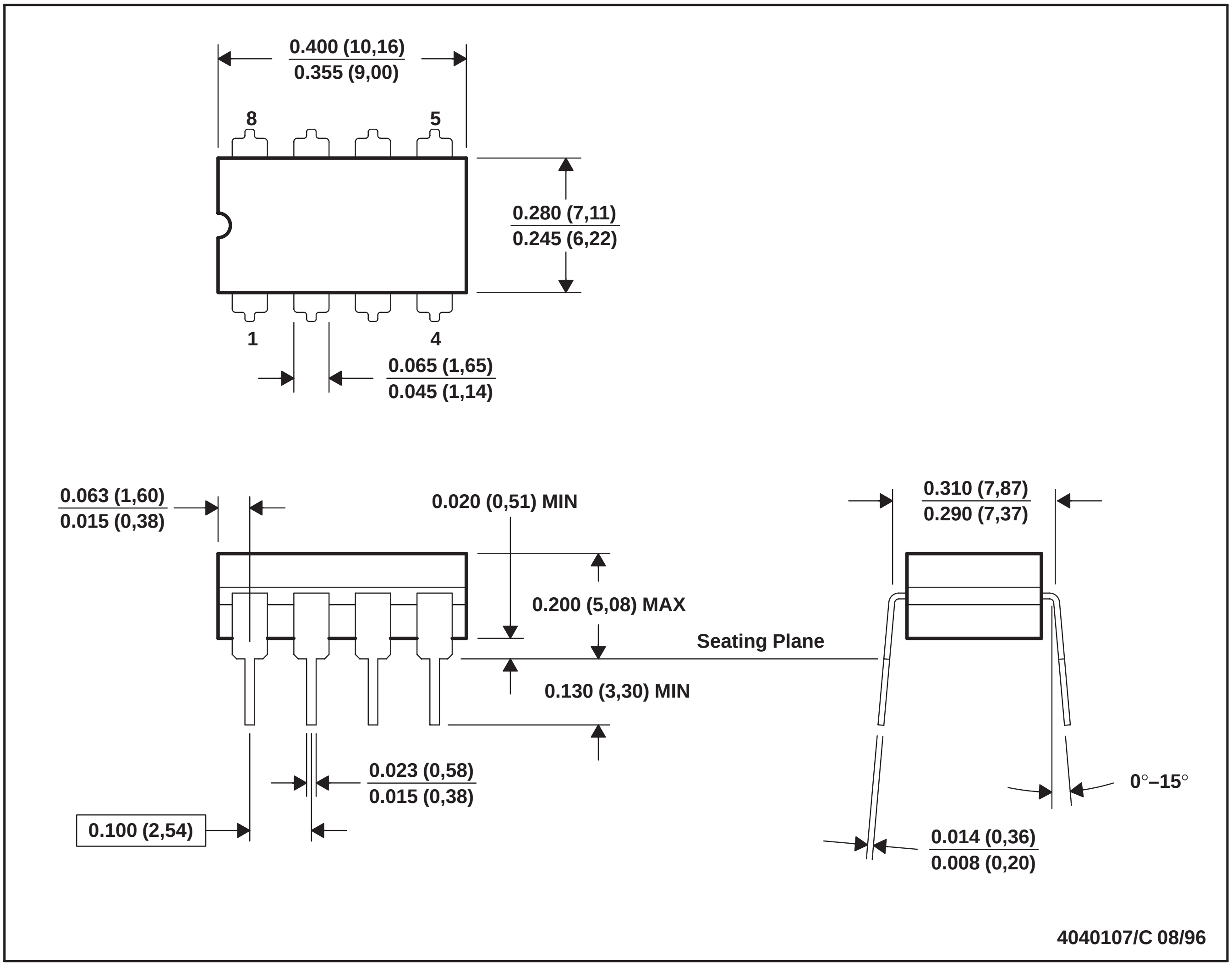


TAPE & REEL

4040001-3/C 10/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Format Lead Option package.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

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