

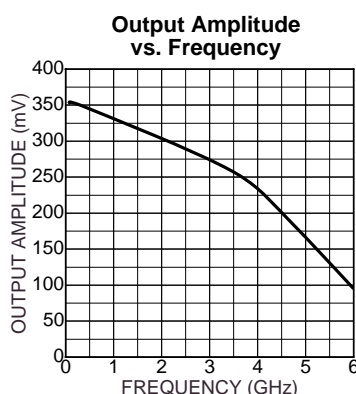
### FEATURES

- Selects among four differential inputs
- Guaranteed AC performance over temp and voltage:
  - DC-to > 3.2Gbps data rate throughput
  - < 600ps In-to-Out  $t_{pd}$
  - < 150ps  $t_r/t_f$
- Ultra low-jitter design:
  - < 1ps<sub>RMS</sub> random jitter
  - < 10ps<sub>PP</sub> deterministic jitter
  - < 10ps<sub>PP</sub> total jitter (clock)
  - < 0.7ps<sub>RMS</sub> crosstalk-induced jitter
- Unique input isolation design minimizes crosstalk
- Internal input termination
- Unique input termination and  $V_T$  pin accepts DC-Coupled and AC-Coupled inputs (LVDS, LVPECL, CML)
- 350mV LVDS output swing
- CMOS/TTL compatible MUX select
- Power supply 2.5V  $\pm 5\%$
- -40°C to +85°C temperature range
- Available in 32-pin (5mm  $\times$  5mm) MLF® package

### APPLICATIONS

- SONET/SDH channel select applications
- Fibre Channel multi-channel select applications
- Gigabit Ethernet multi-channel select

### TYPICAL PERFORMANCE



Precision Edge®

### DESCRIPTION

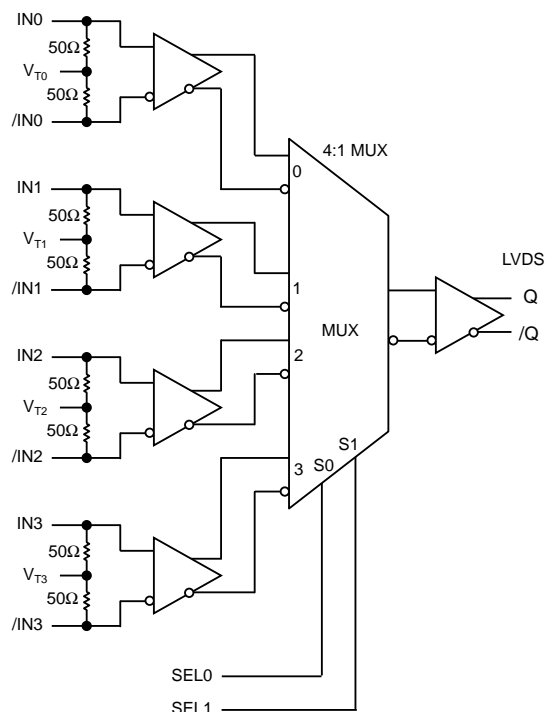
The SY89544U is a fast, low-jitter, 4:1 differential MUX with an LVDS (350mV) compatible output with guaranteed data rate throughput of 3.2Gbps over temperature and voltage.

The SY89544U differential inputs include a unique, 3-pin internal termination that allows access to the termination network through a  $V_T$  pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution.

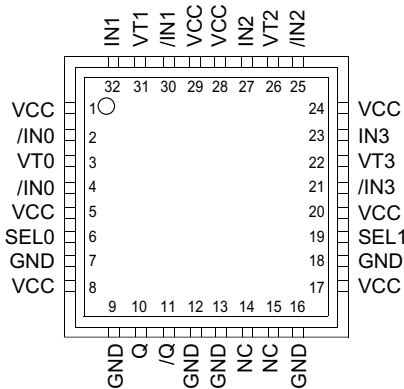
The SY89544U operates from a single 2.5V supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require a 3.3V supply, consider the SY89545L. For applications that require two differential outputs, consider the SY89546U or SY89547L. The SY89544U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

### FUNCTIONAL BLOCK DIAGRAM



## PACKAGE/ORDERING INFORMATION



32-Pin MLF®

Ordering Information<sup>(1)</sup>

| Part Number                    | Package Type | Operating Range | Package Marking                          | Lead Finish    |
|--------------------------------|--------------|-----------------|--|----------------|
| SY89544UMI                     | MLF-32       | Industrial      | SY89544U                                 | Sn-Pb          |
| SY89544UMITR <sup>(2)</sup>    | MLF-32       | Industrial      | SY89544U                                 | Sn-Pb          |
| SY89544UMG <sup>(3)</sup>      | MLF-32       | Industrial      | SY89544U with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY89544UMGTR <sup>(2, 3)</sup> | MLF-32       | Industrial      | SY89544U with Pb-Free bar-line indicator | Pb-Free NiPdAu |

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.
3. Recommended for new designs.

## PIN DESCRIPTION

| Pin Number                   | Pin Name                                   | Pin Function  |
|------------------------------|--|---|
| 4, 2, 32, 30, 27, 25, 23, 21 | IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3 | Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a $V_T$ pin through $50\Omega$ . Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to $V_{CC}$ and the complementary input to GND through a $1k\Omega$ resistor. The $V_T$ pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details. |
| 3, 31, 26, 22                | VT0, VT1, VT2, VT3                         | Input Termination Center-Tap: Each side of the differential input pair, terminates to a $V_T$ pin. The $V_{T0}$ , $V_{T1}$ , $V_{T2}$ , $V_{T3}$ pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.   |
| 6, 19                        | SEL0, SEL1                                 | These single-ended TTL/CMOS compatible inputs select the inputs to the multiplexers. Note that these inputs are internally connected to a $25k\Omega$ pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is $V_{CC}/2$ .   |
| 1, 5, 8, 17, 20, 24, 28, 29  | VCC  | Positive Power Supply: Bypass with $0.1\mu\text{F}  0.01\mu\text{F}$ low ESR capacitors. The $0.01\mu\text{F}$ capacitor should be as close to a $V_{CC}$ pin as possible.  |
| 10, 11                       | Q, /Q                                      | Differential Outputs: This LVDS output pair is the output of the device. It is a logic function of the IN0, IN1, IN0, IN1 and SEL0 inputs. Please refer to the "Truth Table" for details.   |
| 7, 9, 12, 13, 16, 18         | GND, Exposed pad                           | Ground: Ground pin and exposed pad must be connected to the same ground plane.  |
| 14, 15                       | NC   | No connect (unused pins).   |

**Absolute Maximum Ratings<sup>(1)</sup>**

|                                       |                   |
|---------------------------------------|-------------------|
| Supply Voltage ( $V_{CC}$ )           | –0.5V to +4.0V    |
| Input Voltage ( $V_{IN}$ )            | –0.5V to $V_{CC}$ |
| Termination Current <sup>(3)</sup>    |                   |
| Source or sink current on $V_T$       | ±100mA            |
| Input Current                         |                   |
| Source or sink current on IN, /IN     | ±50mA             |
| Lead Temperature (soldering, 20 sec.) | +260°C            |
| Storage Temperature (TS)              | –65°C to +150°C   |

**Operating Ratings<sup>(2)</sup>**

|   |                    |
|---|--------------------|
| Supply Voltage ( $V_{CC}$ )               | +2.375V to +2.625V |
| Ambient Temperature ( $T_A$ )             | –40°C to +85°C     |
| Package Thermal Resistance <sup>(4)</sup> |                    |
| MLF® ( $\theta_{JA}$ )                    |                    |
| Still-Air                                 | 35°C/W             |
| 500lfpm                                   | 28°C/W             |
| MLF® ( $\Psi_{JB}$ )                      |                    |
| Junction-to-Board                         | 20°C/W             |

**DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>**

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Unless otherwise stated.

| Symbol         | Parameter  | Condition                             | Min   | Typ | Max               | Units    |
|----------------|--|---------------------------------------|-------|-----|-------------------|----------|
| $V_{CC}$       | Power Supply                                     |                                       | 2.375 | 2.5 | 2.625             | V        |
| $I_{CC}$       | Power Supply Current                             | No load, Max. $V_{CC}$ <sup>(6)</sup> |       | 50  | 70                | mA       |
| $R_{DIFF\_IN}$ | Differential Input Resistance (IN-to-/IN)        |                                       | 80    | 100 | 120               | $\Omega$ |
| $R_{IN}$       | Input Resistance (IN-to- $V_T$ , /IN-to- $V_T$ ) |                                       | 40    | 50  | 60                | $\Omega$ |
| $V_{IH}$       | Input High Voltage (IN, /IN)                     |                                       | 1.2   |     | $V_{CC}$          | V        |
| $V_{IL}$       | Input Low Voltage (IN, /IN)                      |                                       | 0     |     | $V_{IH}-0.1$      | V        |
| $V_{IN}$       | Input Voltage Swing (IN, /IN)                    | Notes 7                               | 100   |     | $V_{CC}$          | mV       |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing  IN – /IN       | Notes 7                               | 200   |     | $2 \times V_{CC}$ | mV       |
| IN-to- $V_T$   | Voltage from Input to $V_T$                      |                                       |       |     | 1.8               | V        |

**Notes:**

1. Permanent device damage may occur if the ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\Psi_{JB}$  uses 4-layer  $\theta_{JA}$  in still-air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50 $\Omega$  pull-ups.
7. See “Single-Ended and Differential Swings” section for  $V_{IN}$  and  $V_{DIFF\_IN}$  definitions.

**LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS<sup>(9)</sup>**

$V_{CC} = 2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across Q and /Q, unless otherwise stated.

| Symbol           | Parameter                                     | Condition           | Min   | Typ | Max   | Units |
|------------------|---|---------------------|-------|-----|-------|-------|
| $V_{OH}$         | Output HIGH Voltage<br>(Q, /Q)                | See Figure 5a.      |       |     | 1.475 | V     |
| $V_{OL}$         | Output LOW Voltage<br>(Q, /Q)                 | See Figure 5a.      | 0.925 |     |       | V     |
| $V_{OUT}$        | Output Voltage Swing<br>(Q, /Q)               | See Figures 1a, 5a. | 250   | 350 |       | mV    |
| $V_{DIFF-OUT}$   | Differential Output Voltage Swing<br>  Q - /Q | See Figure 1b.      | 500   | 700 |       | mV    |
| $V_{OCM}$        | Output Common Mode Voltage<br>(Q, /Q)         | See Figure 5b.      | 1.125 |     | 1.275 | V     |
| $\Delta V_{OCM}$ | Change in Common Mode Voltage<br>(Q, /Q)      | See Figure 5b.      | -50   |     | +50   | mV    |

**LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS<sup>(9)</sup>**

$V_{CC} = 2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; unless otherwise stated.

| Symbol   | Parameter          | Condition | Min | Typ | Max      | Units   |
|----------|--------------------|-----------|-----|-----|----------|---------|
| $V_{IH}$ | Input HIGH Voltage |           | 2.0 |     | $V_{CC}$ | V       |
| $V_{IL}$ | Input LOW Voltage  |           |     |     | 0.8      | V       |
| $I_{IH}$ | Input HIGH Current |           |     |     | 40       | $\mu A$ |
| $I_{IL}$ | Input LOW Current  |           |     |     | -300     | $\mu A$ |

**Note:**

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**AC ELECTRICAL CHARACTERISTICS<sup>(10)</sup>**

$V_{CC} = 2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across Q and /Q, unless otherwise stated.

| Symbol       | Parameter                                    | Condition                  | Min | Typ | Max | Units             |
|--------------|--|----------------------------|-----|-----|-----|-------------------|
| $f_{MAX}$    | Maximum Operating Frequency                  | NRZ Data                   | 3.2 |     |     | Gbps              |
|              |  | $V_{OUT} \geq 200mV$ Clock |     | 4   |     | GHz               |
| $t_{pd}$     | Differential Propagation Delay               | IN-to-Q                    | 310 | 410 | 510 | ps                |
|              |  | SEL-to-Q                   | 200 | 400 | 700 | ps                |
| $t_{SKEW}$   | Input-to-Input Skew                          | <b>Note 11</b>             |     | 5   | 20  | ps                |
|              | Part-to-Part Skew                            | <b>Note 12</b>             |     |     | 200 | ps                |
| $t_{JITTER}$ | Data Random Jitter (RJ)                      | <b>Note 13</b>             |     |     | 1   | ps <sub>RMS</sub> |
|              | Deterministic Jitter (DJ)                    | <b>Note 14</b>             |     |     | 10  | ps <sub>P</sub>   |
|              | Clock Total Jitter (TJ)                      | <b>Note 15</b>             |     |     | 10  | ps <sub>P</sub>   |
|              | Cycle-to-Cycle Jitter                        | <b>Note 16</b>             |     |     | 1   | ps <sub>RMS</sub> |
|              | Crosstalk-Induced Jitter<br>Adjacent Channel | <b>Note 17</b>             |     |     | 0.7 | ps <sub>RMS</sub> |
| $t_r, t_f$   | Output Rise/Fall Time<br>(20% to 80%)        | At full output swing.      | 35  | 80  | 150 | ps                |

**Notes:**

10. Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC parameters are guaranteed by design and characterization.
11. Input-to-input skew is the difference in propagation delay between any two inputs to the output under identical conditions.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
13. Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 3.2Gbps.
14. Deterministic jitter is measured at 1.25Gbps and 3.2Gbps, with both K28.5 and 2<sup>23</sup>-1 PRBS pattern.
15. Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in 10<sup>12</sup> output edges will deviate by more than the specified peak-to-peak jitter value.
16. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
17. Crosstalk is measured at the output while applying two similar frequencies to adjacent inputs that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

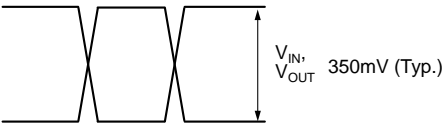


Figure 1a. Single-Ended Voltage Swing

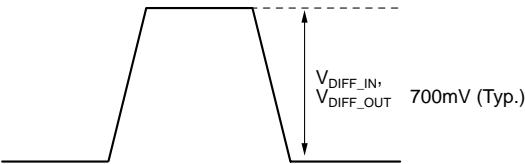


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

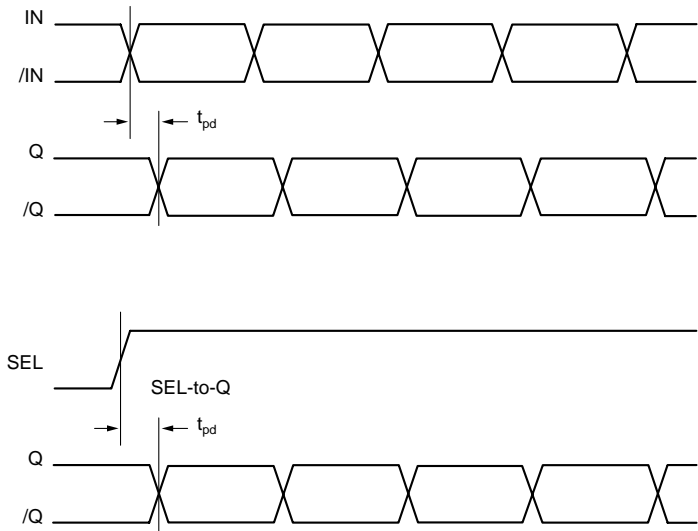
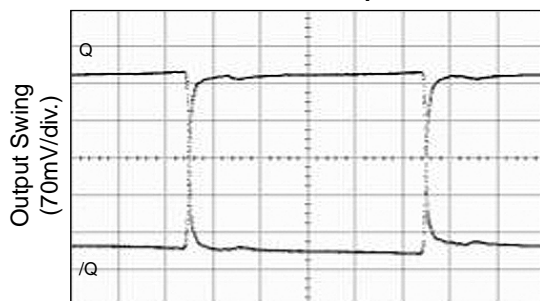
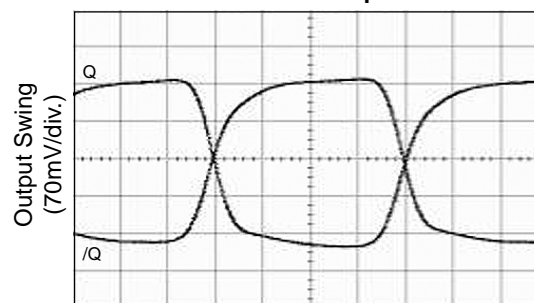
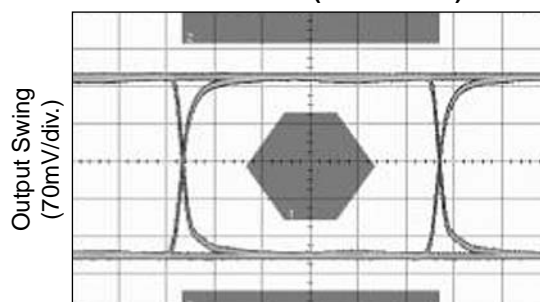
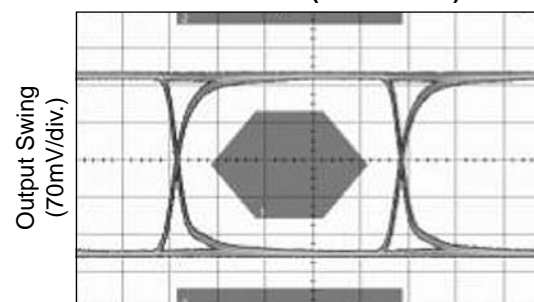
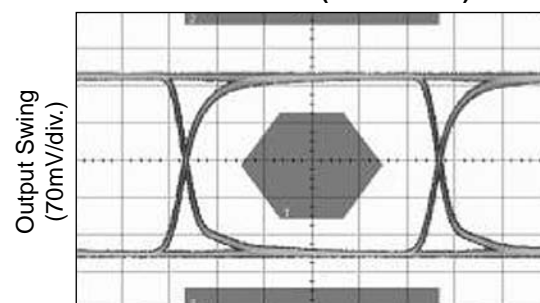
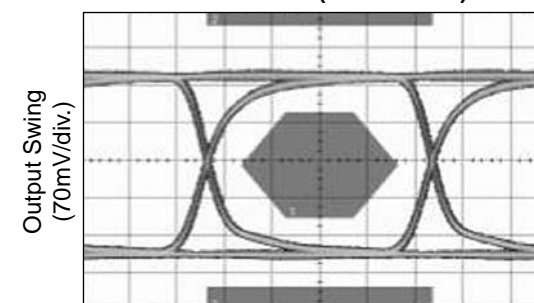
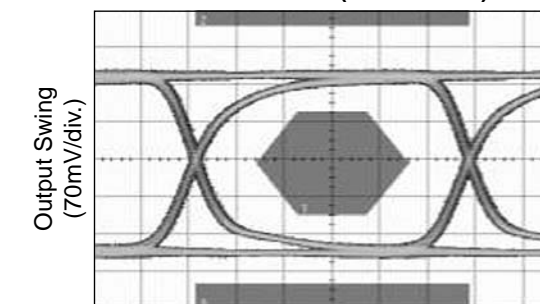
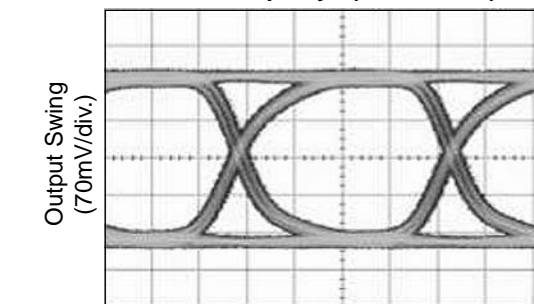


Figure 2. Timing Diagram

TRUTH TABLE

| IN0 | IN1 | IN2 | IN3 | SEL0 | SEL1 | Q | /Q |
|-----|-----|-----|-----|------|------|---|----|
| 0   | X   | X   | X   | 0    | 0    | 0 | 1  |
| 1   | X   | X   | X   | 0    | 0    | 1 | 0  |
| X   | 0   | X   | X   | 1    | 0    | 0 | 1  |
| X   | 1   | X   | X   | 1    | 0    | 1 | 0  |
| X   | X   | 0   | X   | 0    | 1    | 0 | 1  |
| X   | X   | 1   | X   | 0    | 1    | 1 | 0  |
| X   | X   | X   | 0   | 1    | 1    | 0 | 1  |
| X   | X   | X   | 1   | 1    | 1    | 1 | 0  |

**FUNCTIONAL CHARACTERISTICS** $V_{CC} = 2.5V$ ,  $T_A = 25^\circ C$ .**200MHz Output****2.5GHz Output****OC-12 Mask ( $2^{23}-1$  PRBS)****1xFC Mask ( $2^{23}-1$  PRBS)****1xGBE Mask ( $2^{23}-1$  PRBS)****2xFC Mask ( $2^{23}-1$  PRBS)****2xGBE Mask ( $2^{23}-1$  PRBS)****3.2Gbps Eye ( $2^{23}-1$  PRBS)**

## INPUT AND OUTPUT STAGE INTERNAL TERMINATION

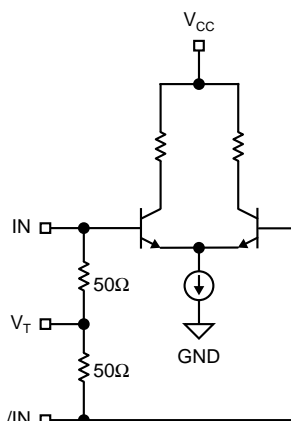


Figure 3. Simplified Differential Input Stage

## INPUT INTERFACE APPLICATIONS

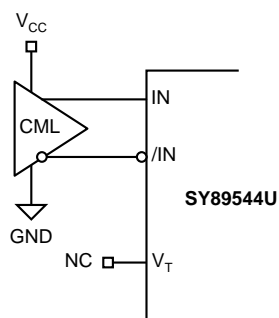


Figure 4a. CML Interface (DC-Coupled)

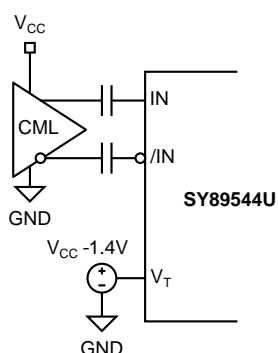


Figure 4b. CML Interface (AC-Coupled)

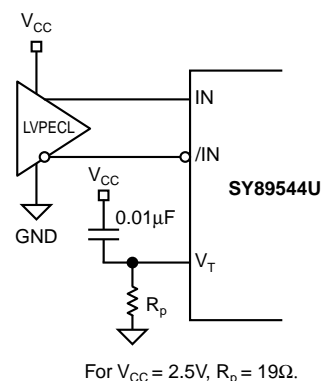


Figure 4c. LVPECL Interface (DC-Coupled)

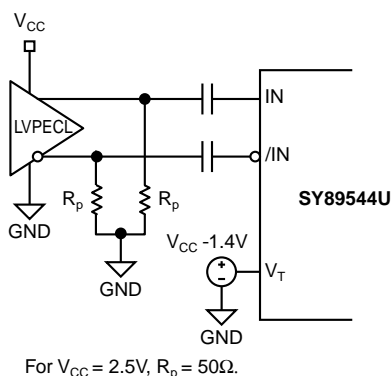


Figure 4d. LVPECL Interface (AC-Coupled)

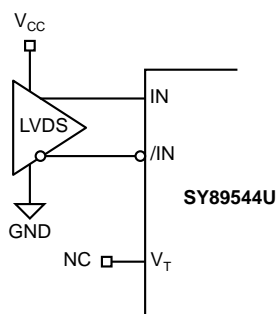


Figure 4e. LVDS Interface



OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in

ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

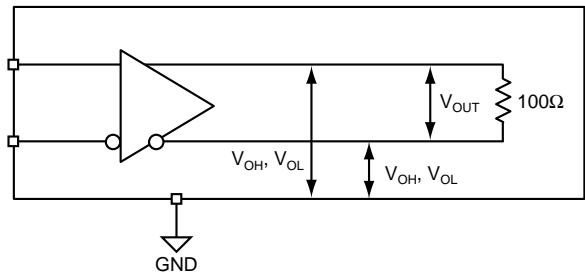


Figure 5a. LVDS Differential Measurement

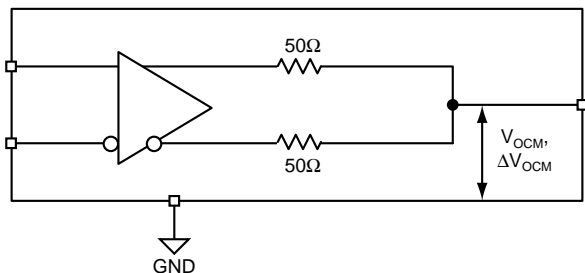
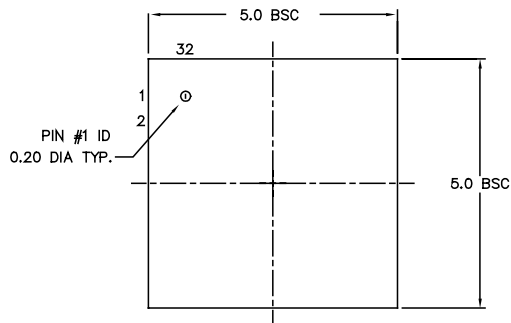


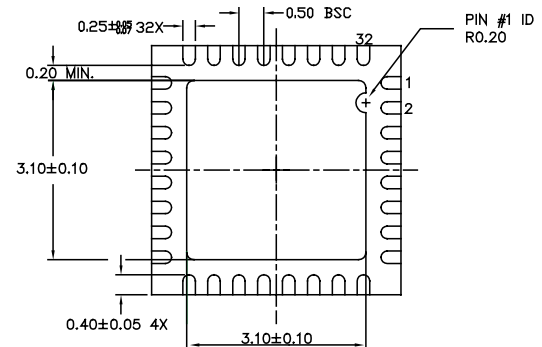
Figure 5b. LVDS Common Mode Measurement

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number   | Function   | Data Sheet Link  |
|---------------|--|--|
| SY89542U      | 2.5 V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination         | <a href="http://www.micrel.com/_pdf/HBW/sy89542u.pdf">http://www.micrel.com/_pdf/HBW/sy89542u.pdf</a>                                  |
| SY89543L      | 3.3V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Input Termination          | <a href="http://www.micrel.com/_pdf/HBW/sy89543l.pdf">http://www.micrel.com/_pdf/HBW/sy89543l.pdf</a>                                  |
| SY89545L      | 3.3V, 3.2Gbps 4:1 LVDS Multiplexer with Internal Input Termination                             | <a href="http://www.micrel.com/_pdf/HBW/sy89545l.pdf">http://www.micrel.com/_pdf/HBW/sy89545l.pdf</a>                                  |
| SY89546U      | 2.5V 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Input Termination | <a href="http://www.micrel.com/_pdf/HBW/sy89546u.pdf">http://www.micrel.com/_pdf/HBW/sy89546u.pdf</a>                                  |
| SY89547L      | 3.3V 3.2Gbps, Differential 4:1 LVDS Multiplexer with 1:2 Fanout and Internal Input Termination | <a href="http://www.micrel.com/_pdf/HBW/sy89547l.pdf">http://www.micrel.com/_pdf/HBW/sy89547l.pdf</a>                                  |
|               | MLF® Application Note  | <a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a> |
| HBW Solutions | New Products and Applications  | <a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>         |

**32-PIN MicroLeadFrame® (MLF-32)**

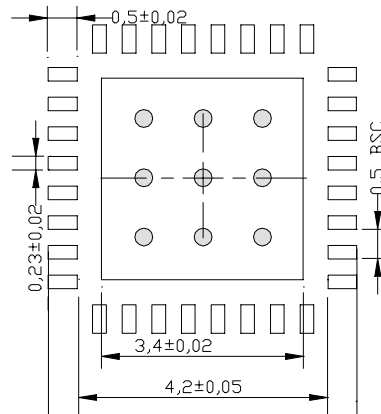
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Gray shaded circles indicates Thermal Via. Size should be .300 mm in diameter and via hole pitch is 1.0 mm and it should be connected to GND plane for maximum thermal characteristic.

## NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

Disclaimer: This is only a recommendation based on information available to Micrel from its suppliers. Actual land pattern may have to be significantly different due to various materials and processes used in PCB assembly. Micrel makes no representation or warranty of performance based on the recommended land pattern."

**PCB Thermal Consideration for 32-Pin MLF® Package**  
(Always solder, or equivalent, the exposed pad to the PCB)

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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