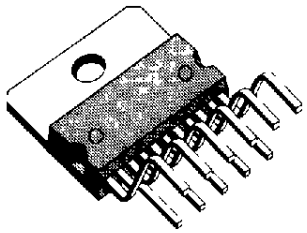
SGS-THOMSON MICROELECTRONICS

TEA2117

HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT FRAME YOKE DRIVE ± 1.5A DRIVING CURRENT
- LINE DARLINGTON DRIVING CAPABILITY
- BUILT-IN FRAME SEPARATOR WITHOUT EXTERNAL COMPONENTS
- INTEGRATED FLYBACK GENERATOR
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- VERY FEW EXTERNAL COMPONENTS
- HIGH DISSIPATION POWER PACKAGE
- SEPARATE POWER GROUND
- HORIZONTAL OSCILLATOR FREQUENCY RANGE FROM 15kHz TO 100kHz
- VERTICAL OSCILLATOR FREQUENCY RANGE FROM 30Hz TO 120Hz



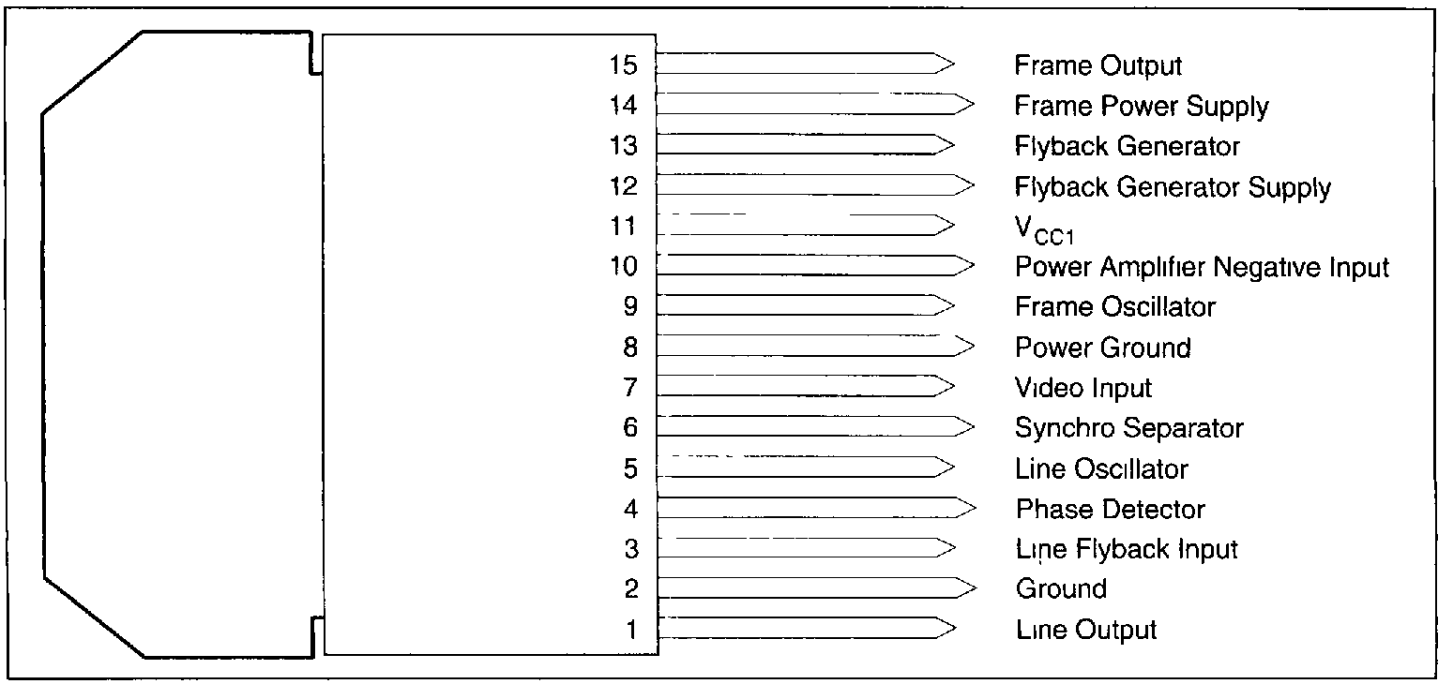
MULTIWATT 15
(Plastic Package)

ORDER CODE : TDA2117

DESCRIPTION

The TEA2117 is an horizontal and vertical deflection circuit. It is particularly intended for display video units. The TEA2117, with separate power ground, is particularly well-suited for high current applications.

PIN CONNECTIONS



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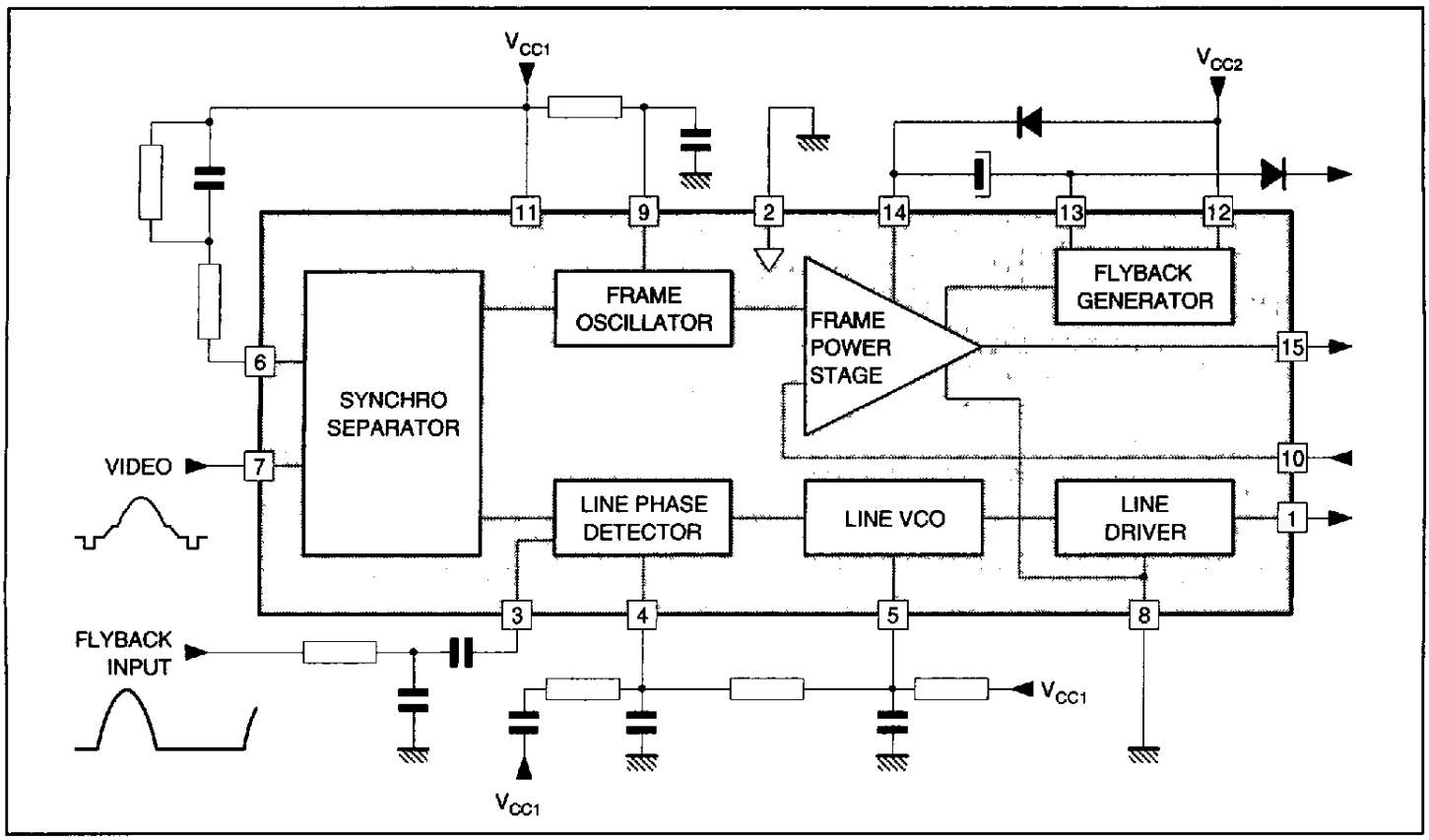
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATNGS

Symbol	Parameter	Value	Unit
V_{CC1}	Supply Voltage	20	V
V_{12}	Flyback Generator Supply Voltage	30	V
V_{14}	Frame Power Supply Voltage	60	V
I_{15}	Frame Output Current	± 1.5	A
V_1	Line Output Voltage (external)	60	V
I_{P1}	Line Output Peak Current	0.8	A
I_{C1}	Line Output Continuous Current	0.4	A
T_{stg}	Storage Temperature	– 40, + 150	°C
T_j	Max Operating Junction Temperature	150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}c)}$	Max Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j\text{-}a)}$	Typical Junction-ambient Thermal Resis.	40	°C/W
T_j	Max Recommended Junction Temperature	120	°C

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC1} = 10V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 11)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	8		20	V
VIDEO INPUT (Pin 7)					
V_7	Input Threshold Voltage (I_7 = – 1µA)		4		V
	Video Input Signal (see application diagram)	0.4		4	Vpp

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ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25°C, V_{CC1} = 10V

Symbol	Parameter	Min.	Typ.	Max.	Unit
LINE FLYBACK INPUT (Pin 3)					
V_3	Bias Voltage		2.7		V
Z_3	Input Impedance	4.5	6	8	kΩ
PHASE COMPARATOR (Pin 4)					
I_4	Output Current During Synchro Pulse		± 600		µA
I_{4R}	Current Ratio (positive/negative)	0.9	1.0	1.1	
LI4	Leakage Current	− 1		+ 1	µA
	Control Range Voltage	2 5		7	V
	Control Sensibility (see application diagram)		750		Hz/µs
	Pull in Range (see application diagram)		± 800		Hz
LINE OSCILLATOR (Pin 5)					
LT5	Low Threshold Voltage		3.2		V
HT5	High Threshold Voltage		6.6		V
BI5	Bias Current		50		nA
DR5	Discharge Impedance		800		Ω
FLP1	Free Running Line Period (R = 12kΩ tied to V_{CC1}, C = 6.8nF tied to Ground)	61 5	64	66.5	µs
FLP2	Free Running Line Period (R = 12.3kΩ, C = 2.2nF)		27		µs
0T5	Oscillator Threshold for Line Output Pulse Triggering		5		V
$\frac{\Delta T}{\Delta V}$	Supply Voltage Influence on Free-running Period		0.051		µs/V

T_{amb} = 25°C, V_{CC1} = 10V, V_{14} = 30V

Symbol	Parameter	Min.	Typ.	Max.	Unit
LINE OUTPUT (Pin 1)					
LV1	Saturation Voltage to Ground (I_1 = 200mA)		1.1	1.5	V
CPW	Output Pulse Width (line period = 64µs)	20	22	24	µs
FRAME OSCILLATOR (Pin 9)					
LT9	Low Threshold Voltage	1.8	2	2 3	V
HT9	High Threshold Voltage	2.6	3.1	3.6	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance		500		Ω
FFP1	Free Running Frame Period (R = 845kΩ tied to V_{CC1}, C = 180nF tied to Ground)	21.4	22 5	25	ms
FFP2	Free Running Frame Period (R = 425kΩ, C = 220nF)		14.3		ms
MFP	Minimum Frame Period (I_7 = − 100µA) with the Same RC	14.6	17	19	ms
FG	Frame Sawtooth Gain between Pin 9 and Non-inverting Input of the Frame Amplifier (internal)		− 0.4		
FRAME POWER SUPPLY (Pin 14)					
V_{14}	Operating Voltage (with flyback generator)	10		58	V
I_{14}	Supply Current (V_{14} = 30V)		16	25	mA
FLYBACK GENERATOR SUPPLY (Pin 12)					
V_{12}	Operating Voltage	10		30	V
FRAME OUTPUT					
LV15A LV15B	Saturation Voltage to Ground I_{15} = 0 1A I_{15} = 1A		60 0.4	0.8	mV V

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC1} = 10V, V_{14} = 30V) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME OUTPUT (continued)					
	Saturation Voltage to V_{CC2}				
HV15A	I_{15} = – 0.1A		1.3		V
HV15B	I_{15} = – 1A		1.7	2.4	V
	Saturation Voltage to V_{CC2} in Flyback Mode ($V_{15} > V_{14}$)				
FV15A	I_{15} = 0.1A		1.7		V
FV15B	I_{15} = 1A		2.6	4	V
FLYBACK GENERATOR (Pins 12 and 13)					
	Flyback Transistor on (output = high state) V13/12 with				
F2DA	$I_{13 \rightarrow 12}$ = 0.1A		1.6		V
F2DB	$I_{13 \rightarrow 12}$ = 1A		3	4	V
	Flyback Transistor on (output = high state) V12/13 with				
FSVA	$I_{12 \rightarrow 13}$ = 0.1A		0.9		V
FSVB	$I_{12 \rightarrow 13}$ = 1A		2	4	V
	Flyback Transistor off (output = V_{14} – 8V) V_{12} = V_{14} = 30V				
FCI	Leakage Current Pin 12			100	µA

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GENERAL DESCRIPTION

The TEA2117 performs all of the video and power functions required to provide signals for the direct drive of a line darlington and the frame yoke.

It contains :

- A synchronizing separator with the slice level of synchro separation determined by the external components.
- An integrated frame synchronizing separator without external components.
- A saw tooth generator for the frame with synchronization allowed during the last fourth of the free run period.
- A power amplifier for direct drive of the frame yoke with overload, short circuit and thermal protections.
- A line phase detector and a voltage control oscillator.
- An open collector output for the direct drive of a line darlington.
- Separate power ground (Pin 8)

SYNCHRONIZATION SEPARATOR CIRCUIT (Figure 1)

The sync-tip DC level on pin 7 is clamped to 3.8V. The slice level of sync-separation present on capacitor C1 depends on the value of resistor R1 and R2. When the video signal on pin 7 decreases under the capacitor voltage the transistors Q1 and Q2 provide current for the other parts of the circuit.

FRAME SEPARATOR (Figure 2)

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR (Figure 3)

The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The voltage control is applied on resistor R5.

PHASE COMPARATOR (Figure 4)

The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 3 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 3 superior to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternately negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning. (see Figure 5)

LINE OUTPUT (Pin1)

It is an open collector output which is able to drive pulse current of 500mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

FRAME OSCILLATOR (Figure 6)

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last fourth of the free run period. The input current during the charge of the capacitor is less than 100nA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.
Its positive input is directly connected to the invert of the frame saw tooth.

Figure 1

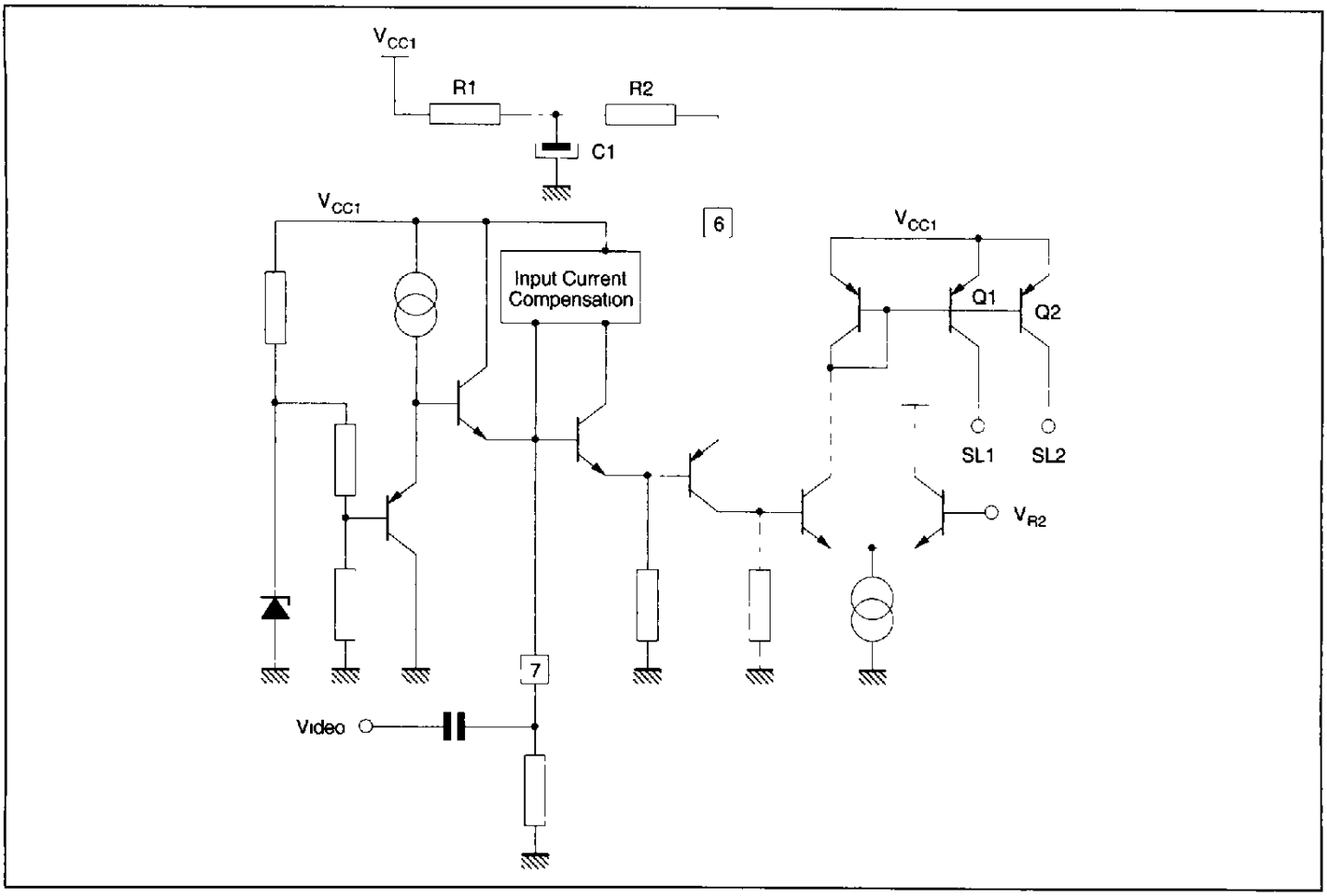

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Figure 2

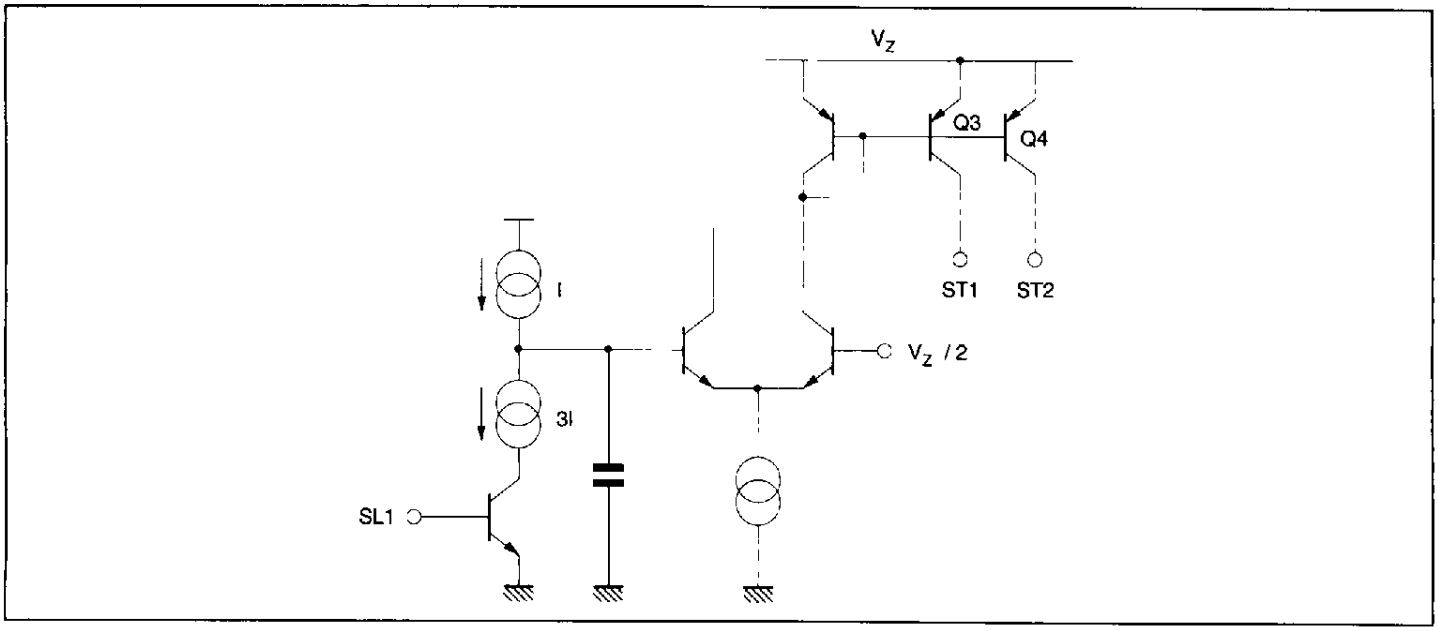

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Figure 3

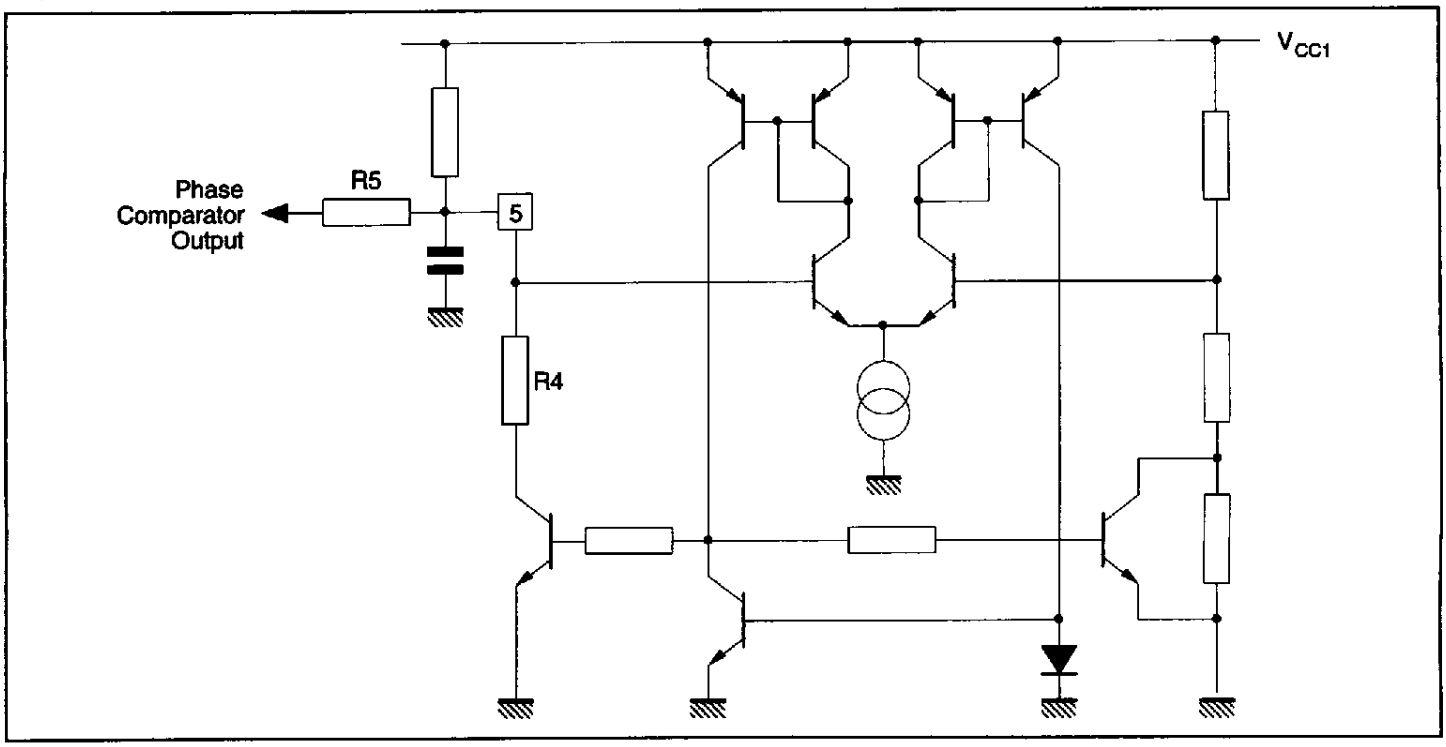

Figure 4

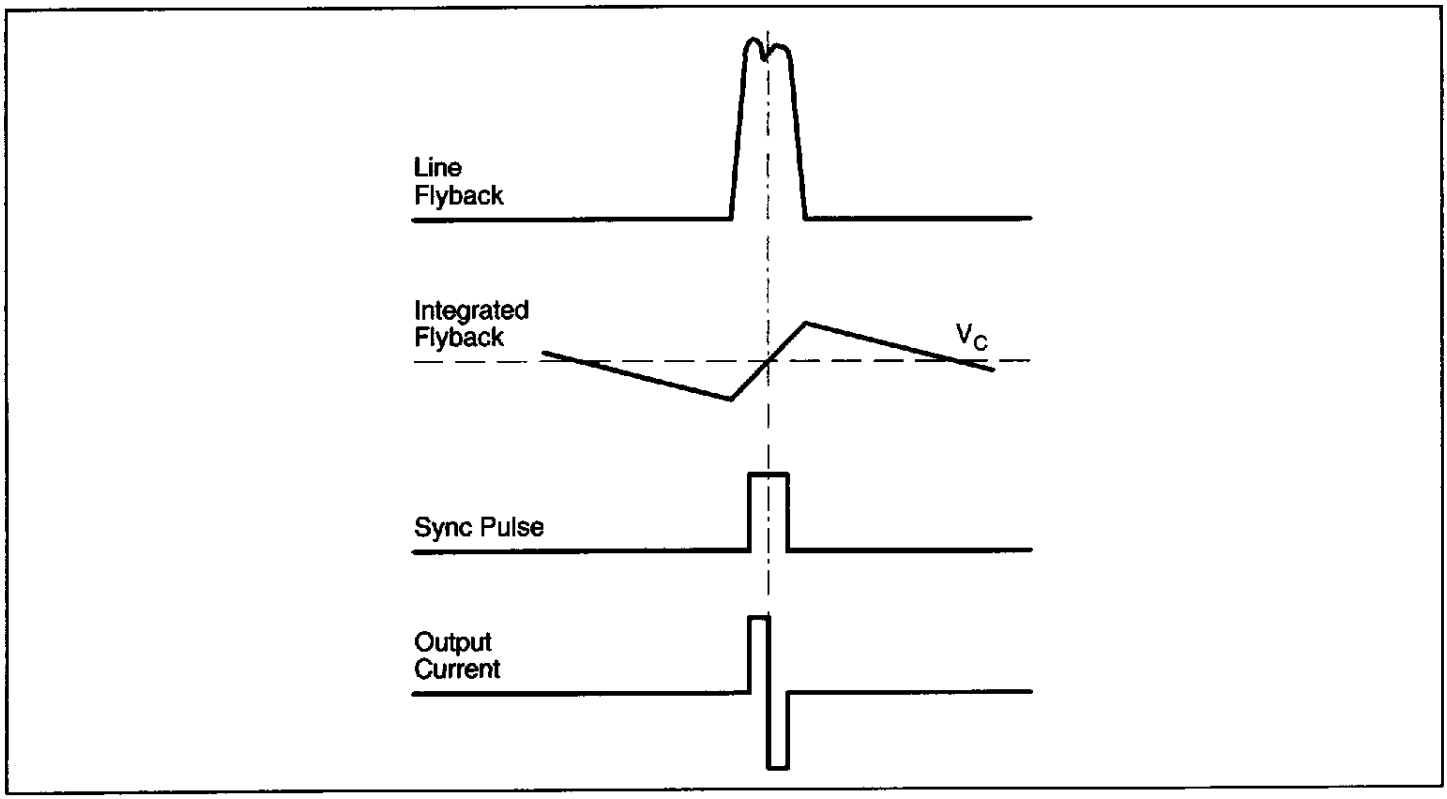

Figure 5

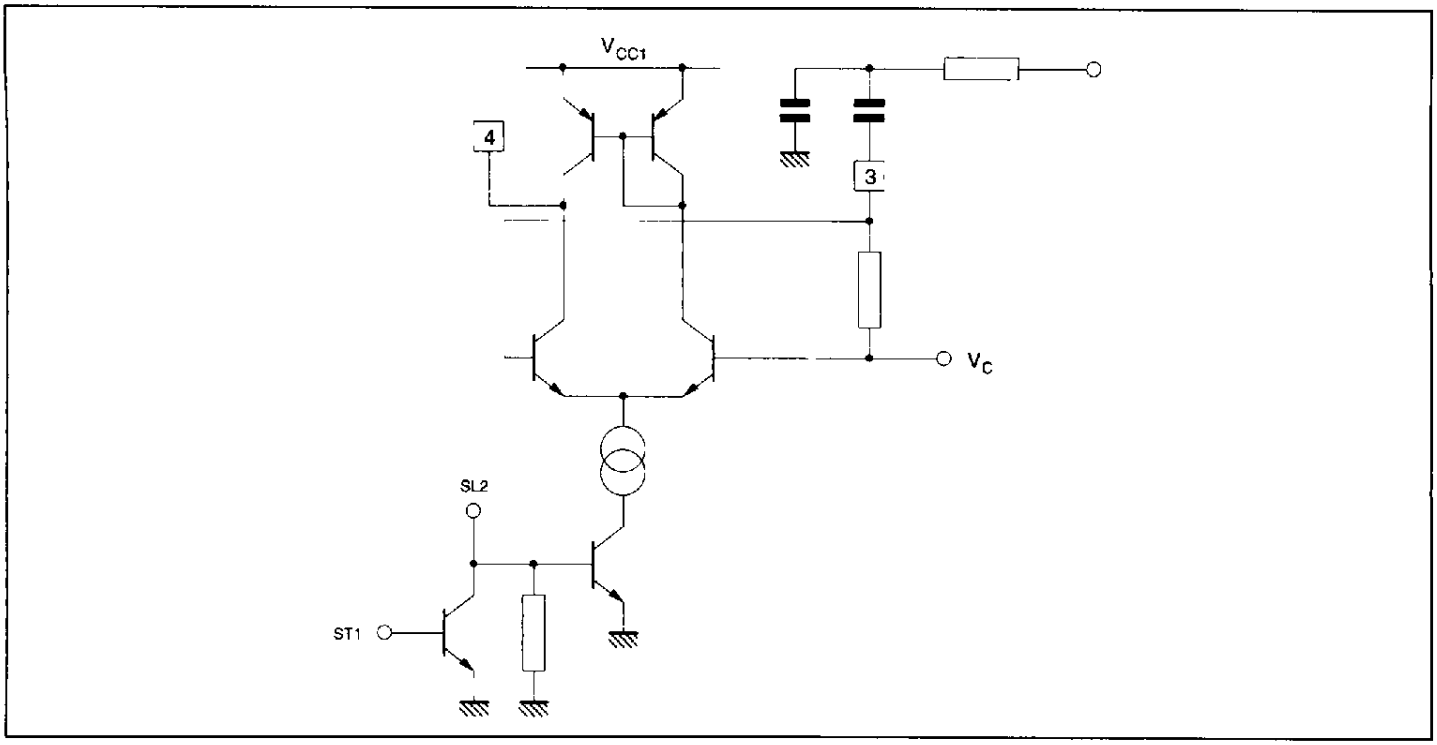

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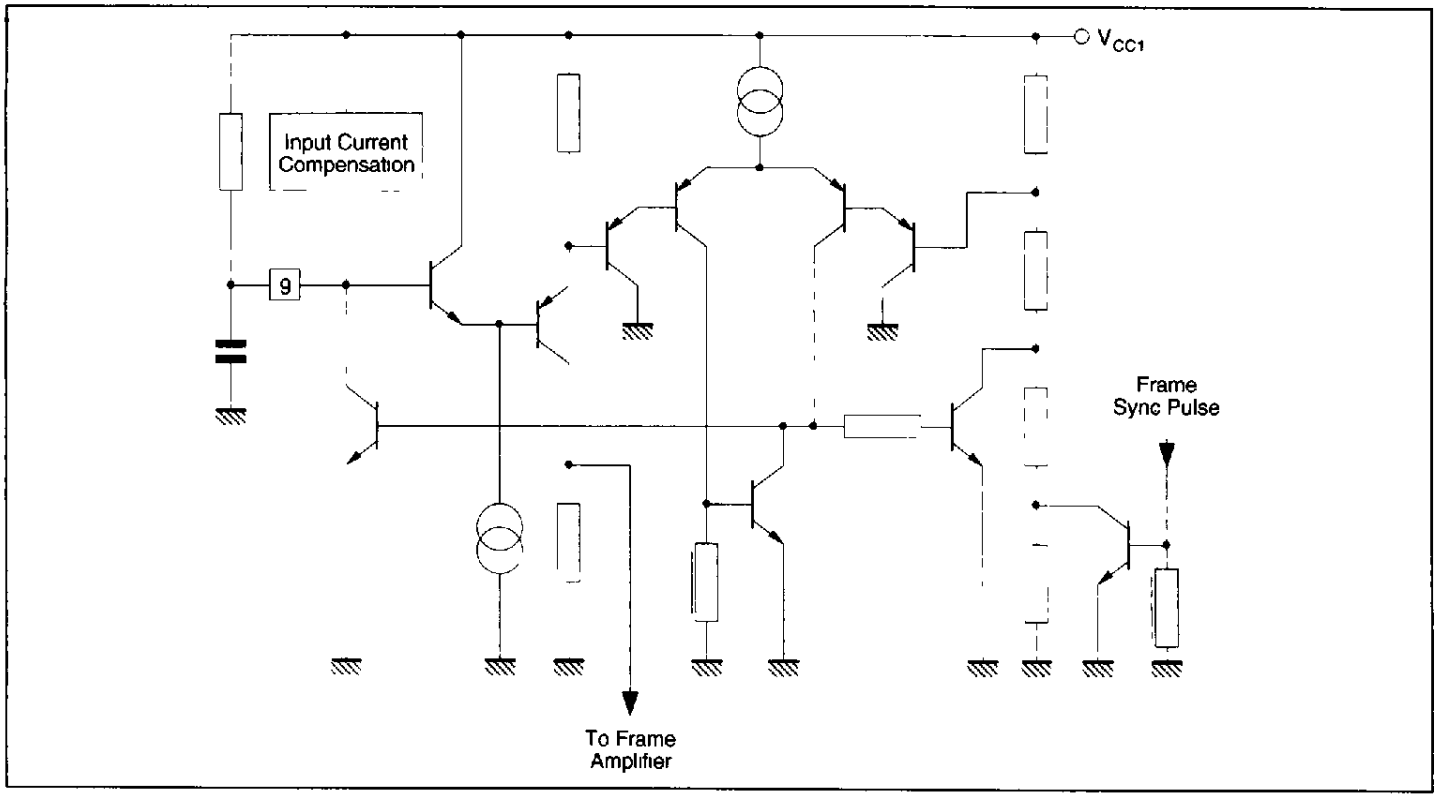
Figure 6



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APPLICATION DIAGRAM (without internal flyback generator)

TYPICAL BLACK-WHITE MONITOR APPLICATION FOR 14" - 90° SCREEN
(with yoke L = 5.8mH, R = 2.7Ω, I_{PP} = 2A), f_H = 31.kHz, f_V = 60/70Hz