TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9256APG, TC9256AFG, TC9257APG, TC9257AFG

PLL for DTS

The TC9256APG, TC9256AFG, TC9257APG and TC9257AFG are phase-locked loop (PLL) LSIs for digital tuning systems (DTS) with built-in two-modulus prescalers.

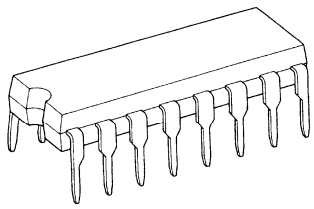
All functions are controlled through three serial bus lines.

These LSIs are used to configure high-performance digital tuning systems.

Features

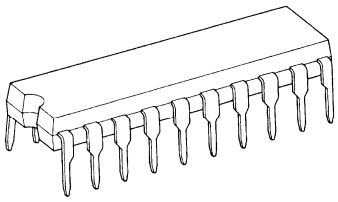
- Suitable for use in digital tuning systems in high-fi tuners and car stereos.
- Built-in prescalers operate at an input frequency ranging from 30 to 150 MHz during FM_{IN} input (with two-modulus prescaler) and at 0.5 to 40 MHz during AM_{IN} input (with two-modulus prescaler or direct dividing)
- 16-bit programmable counter, dual parallel output phase comparator, crystal oscillator and reference counter
- 3.6 MHz, 4.5 MHz, 7.2 MHz or 10.8 MHz crystal oscillators can be used.
- 15 possible reference frequencies (when using 4.5 MHz crystal)·ref. = 0.5 k, 1 k, 2.5 k, 3 k, 3.125 k, 3.90625 k, 5 k, 6.25 k, 7.8125 k, 9 k, 10 k, 12.5 k, 25 k, 50 k and 100 kHz.
- Built-in 20-bit general-purpose counter for such uses as measuring intermediate frequencies (IF_{IN1} and IF_{IN2}) and low-frequency pilot signal cycles (SC_{IN}). (No cycle measurement function is available on the TC9256APG and TC9256AFG.)
- High-precision (±0.55 to ±7.15 µs) PLL phase error detection
- Numerous general-purpose I/O pins for such uses as peripheral circuit control
- Four N-channel open-drain output ports (OFF withstanding voltage: 12 V) for such uses as control signal output. (TC9256APG and TC9256AFG have only three ports.)
- Standby mode function (turns off FM, AM and IF amps) to save current consumption
- All functions controlled through three serial bus lines
- CMOS structure with operating power supply range of V_{DD} = 5.0 ± 0.5 V.
- 16-pin DIP (TC9256APG), 20-pin DIP (TC9257APG), 16-pin SOP (TC9256AFG), 20-pin SOP (TC9257AFG) packages

TC9256APG



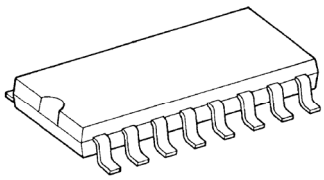
P-DIP16-300-2.54A

TC9257APG



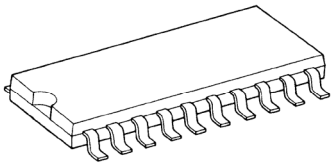
P-DIP20-300-2.54A

TC9256AFG



P-SOP16-300-1.27A

TC9257AFG

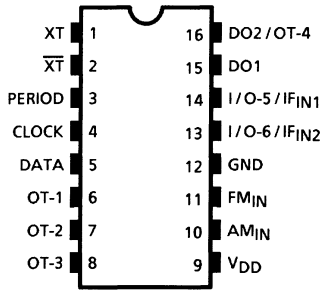


P-SOP20-300-1.27A

Weight
P-DIP16-300-2.54A: 1.0 g (typ.)
P-DIP20-300-2.54A: 1.24 g (typ.)
P-SOP16-300-1.27A: 0.16 g (typ.)
P-SOP20-300-1.27A: 0.48 g (typ.)

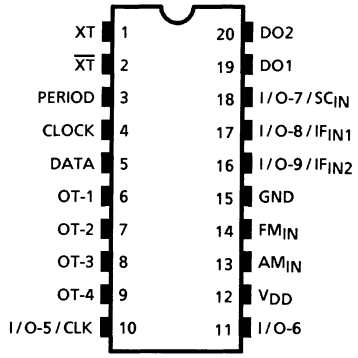
Pin Assignment (Top view)

TC9256APG, TC9256AFG



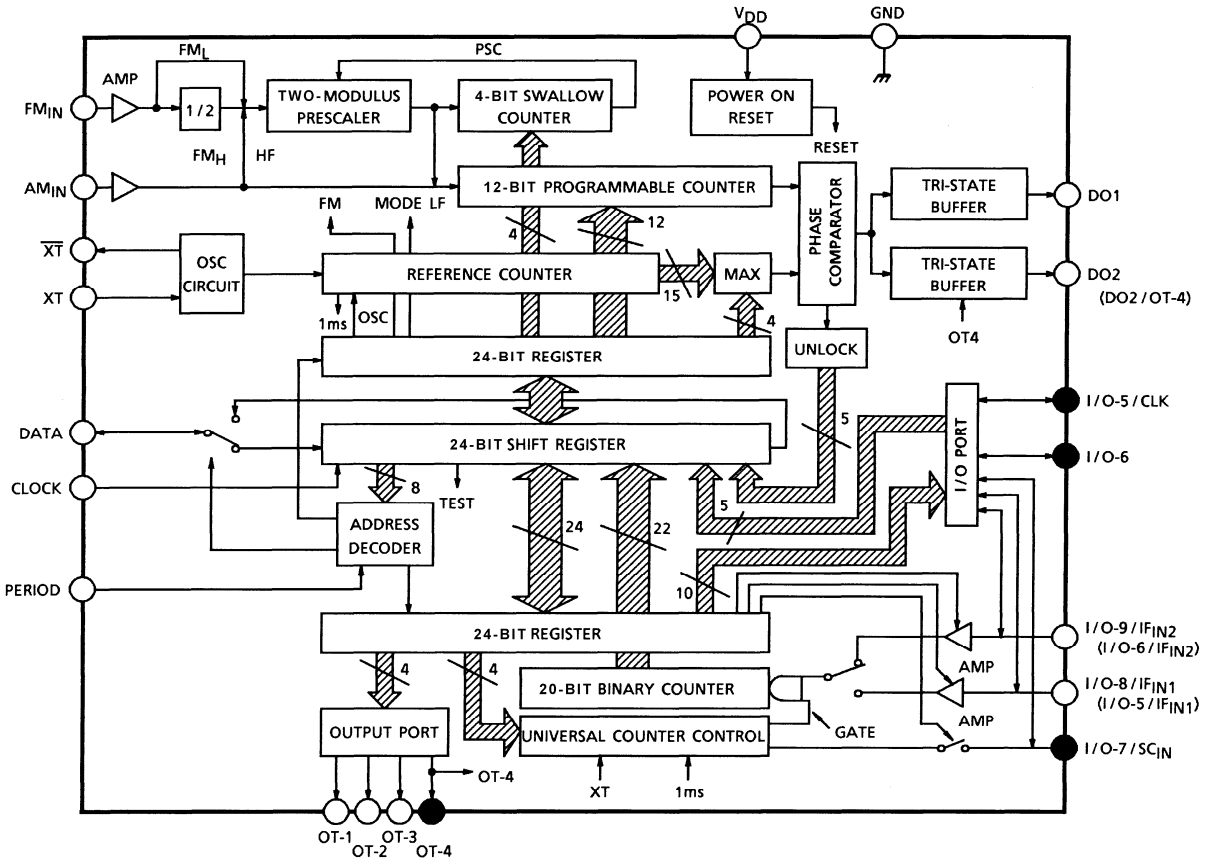
DIP-16PIN / SOP-16PIN

TC9257APG, TC9257AFG



DIP-20PIN / SOP-20PIN

Block Diagram

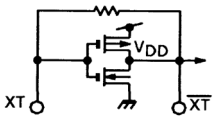
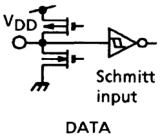
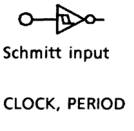
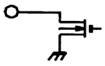
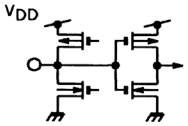
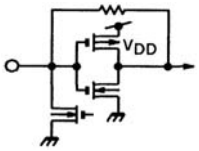
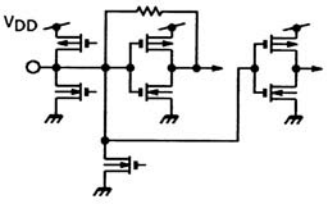


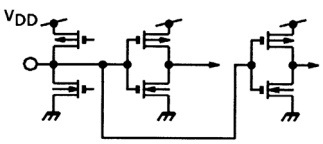
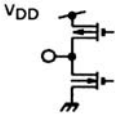
Note: There are no pins marked ● in the TC9256APG or TC9256AFG.

Pin names and numbers in parentheses apply to the TC9256APG and TC9256AFG.

Other pins are common to the TC9256APG, TC9256AFG, TC9257APG and TC9257AFG.

Pin Function

Pin No.	Symbol	Pin Name	Function	Circuit Diagram
1	XT	Crystal oscillator pins	Connects a 3.6 MHz, 4.5 MHz, 7.2 MHz or 10.8 MHz crystal oscillator to supply reference frequency and internal clock.	
2	$\overline{XT}$			
3	PERIOD	Period signal input	Serial I/O ports. These pins transfer data to and from the controller to set divisors and dividing modes, and to control the general-purpose counter and general-purpose I/O ports.	 
4	CLOCK	Clock signal input		
5	DATA	Serial data input/output		
6	OT-1	General-purpose output ports	N-channel open drain port pins, for such uses as control signal output. These pins are set to the OFF state when power is turned on. (On the TC9256APG and TC9256AFG, OT-4 can be used as a CMOS output pin by being switched with DO2.)	
7	OT-2			
8	OT-3			
9 (—)	OT-4			
10 (—)	I/O-5/CLK	General-purpose I/O ports	The CMOS structure allows free use of these ports for input or output. Ports are set for input when the power is turned on. On the TC9257APG and TC9257AFG, I/O-5 can be switched for use as a system clock output pin.	
11 (—)	I/O-6			
13 (10)	AM_{IN}	Programmable counter input	These pins input FM and AM band local oscillator signals.. These pins feature built-in amps. Connecting a capacitor permits low-amplitude operation.	
14 (11)	FM_{IN}			
16 (13)	I/O-9 (-6) /IF_{IN2}	General-purpose I/O ports /General-purpose counter frequency measurement input	General-purpose I/O port input/output pins. Can be switched for use as input pins to measure general-purpose counter frequencies. The frequency measurement function has such uses as measuring intermediate frequencies (IF). These pins feature built-in amps. Connecting a capacitor permits low-amplitude operation. Note: These pins are set for input when power is turned on.	
17 (14)	I/O-8 (-5) /IF_{IN1}			

Pin No.	Symbol	Pin Name	Function	Circuit Diagram
18 (—)	I/O-7/SC_{IN}	General-purpose I/O ports /General-purpose counter cycle measurement input	General-purpose I/O port input/output pin. Can be switched for use as signal input pin to measure low-frequency signal cycles. (Not available on the TC9256APG and TC9256AFG.) Note: This pin is set for input when power is turned on.	
19 (15)	DO1	Phase comparator output (General-purpose output ports)	These pins are for phase comparator tristate output. DO1 and DO2 are output in parallel. (On the TC9256APG and TC9256AFG, DO2 can be switched for use as a general-purpose output port.)	
20 (16)	DO2 (DO2/OT-4)			
15 (12)	GND	Power supply pins	Applies 5.0 V ± 10%.	—
12 (9)	V_{DD}			

Note 1: Pin numbers 1 to 8 are common to the TC9256APG, TC9256AFG, TC9257APG and TC9257AFG.

Note 2: Pin names and numbers in parentheses apply to the TC9256APG and TC9256AFG.

Functions and Operation

Serial I/O Ports

As the block diagram shows, the functions of the TC9256APG, TC9256AFG, TC9257APG and TC9257AFG are controlled by setting data in the 48 bits contained in each of the two sets of 24-bit registers. Each bit of data in these registers is transferred through the serial ports between the controller and the DATA, CLOCK and PERIOD pins. Each serial transfer consists of a total of 32 bits, with 8 address bits and 24 data bits.

Since all functions are controlled in units of registers, the explanation here focuses on the 8-bit addresses and functions of each register.

These registers consist of 24 bits and are selected by an 8-bit address.

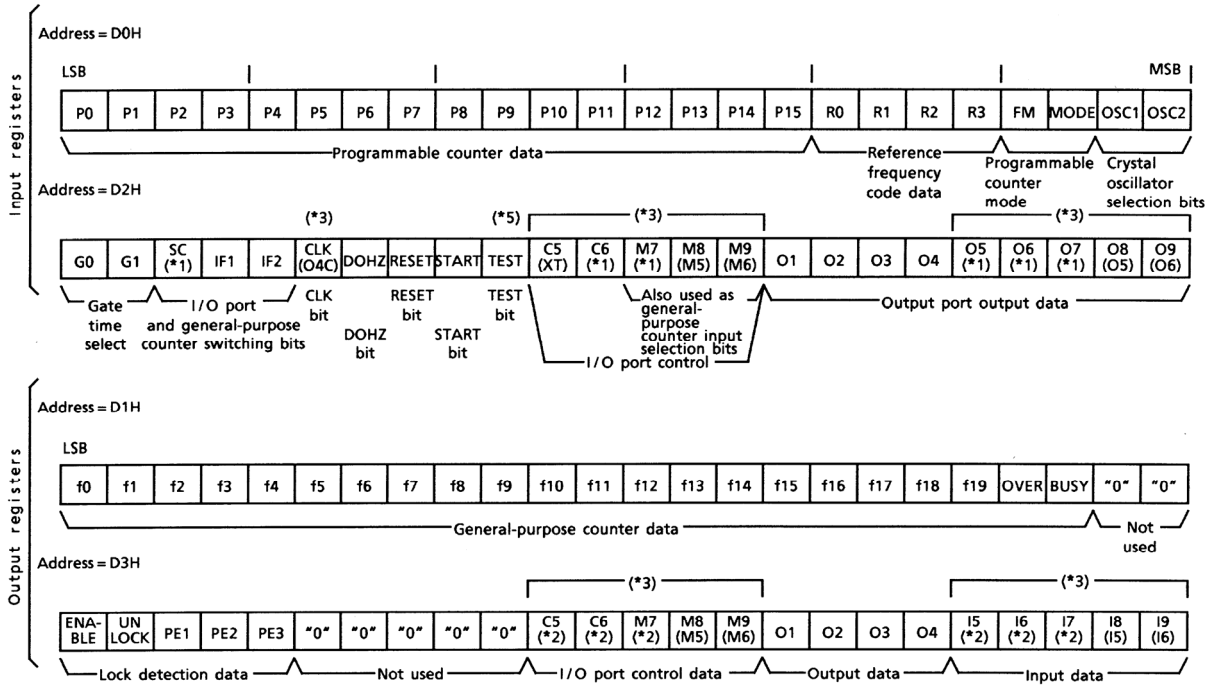
A list of the address assignments for each register is given below under Register Assignments.

Register	Address	24-Bit Composition	No. of Bits
Input Register 1	D0H	PLL divisor setting	16
		Reference frequency setting	4
		PLL input and mode setting	2
		Crystal oscillator selection	2
			Total 24
Input Register 2	D2H	General-purpose counter control (Including lock-detection bit control)	4
		I/O port and general-purpose counter switching bits	3
		I/O-5/CLK pin switching bit	1
		(DO2/OT-4 pin switching bit for TC9256APG and TC9256AFG)	1
		DO pin control	1
		TEST bit	5
		I/O port control (Also used as general-purpose counter input-selection bits)	9
		Output data	24
			Total
Output Register 1	D1H	General-purpose counter numeric data	22
		Not used	2
			Total 24
Output Register 2	D3H	Lock detection data	5
		I/O port control data	5
		Output data	4
		Input data (undefined during output port selection)	5
		Not used	5
			Total 24

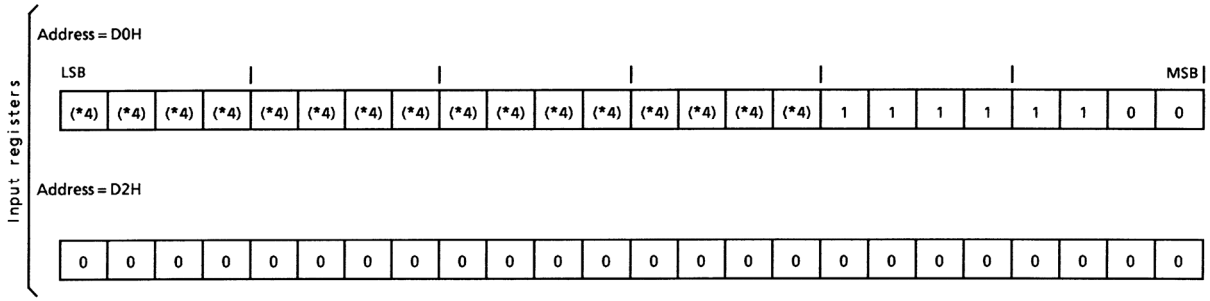
On the falling edge of the PERIOD signal, the input data is latched in register 1 or register 2 and the function is performed.

On the ninth falling edge of the CLOCK signal, the output data is latched in parallel in the output registers. The data are subsequently output serially from the data pin.

Register Assignments



When power is turned on, the input registers are set as shown below.



*1: This setting is not available on the TC9256APG and TC9256AFG.

*2: The data is “0” on the TC9256APG and TC9256AFG.

*3: Bit names in parentheses “( )” apply to the TC9256APG and TC9256AFG.

*4: Data is undefined.

*5: Set data to “0” for the TEST bit.

Serial Transfer Format

The serial transfer format consists of 8 address bits and 24 data bits (Figure 1). Addresses D0H to D3H are used.

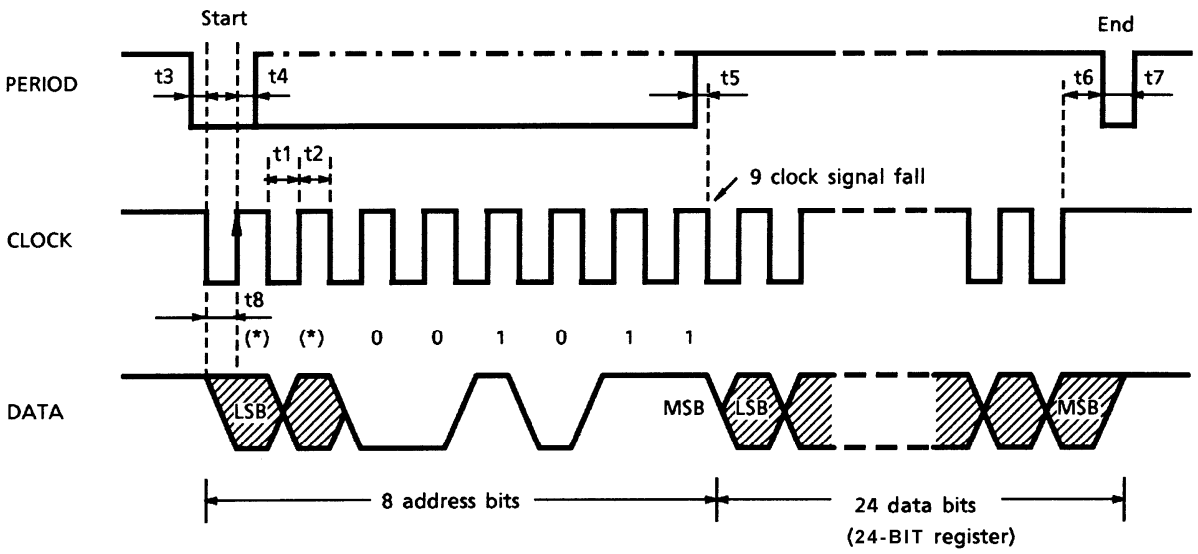


Figure 1

- Serial data transfer

  Serial data are transferred in sync with the clock signal. In the idle state, the PERIOD, CLOCK and DATA pin lines are all set to "H" level. When the period signal is at "L" level, serial data transfer starts at the falling edge of the clock signal. Data transfer ends when the period signal is set to "L" level while the clock signal is at "H" level. Once serial data transfer has begun, however, no more than 8 falls of the clock signal can occur during the time the period signal is at "L" level.

  Since the receiving side receives the serial data as valid data at the rising edge of the clock signal, it is effective for the sending side to produce output in sync with the falling edge of the clock signal.

  To receive serial data from the output registers (D1H, D3H), set the serial data output to high impedance after the 8-bit address is output but before the next falling edge of the clock signal.

  Data reception subsequently continues until the period signal becomes "L" level; data transfer ends just before the rising edge of the period signal. Therefore, the data pin must have an open-drain or tristate interface.

Note 1: When power is turned on, some internal circuits have undefined states. To set the internal circuit state, execute a dummy data transfer before performing regular data transfer.

Note 2: Times t1 to t8 have the following values:

t1 ≧ 1.0 μs

t2 ≧ 1.0 μs

t3 ≧ 0.3 μs

t4 ≧ 0.3 μs

t5 ≧ 0.3 μs

t6 ≧ 1.0 μs

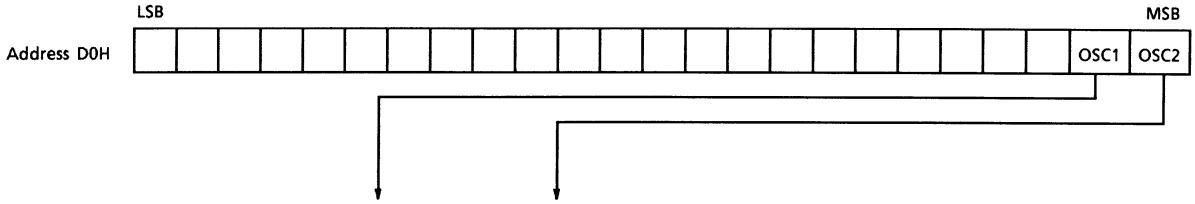
t7 ≧ 1.0 μs

t8 ≧ 0.3 μs

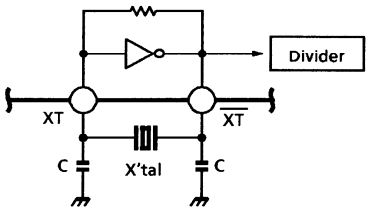
Note 3: Asterisks represent numbers taken from addresses, as in D*H.

Crystal Oscillator Pins (XT, $\overline{XT}$)

As Figure 2 shows, the clock required for internal operation is produced by connecting a crystal oscillator between capacitors. Use the crystal oscillator selection bit to select an oscillating frequency of 3.6 MHz, 4.5 MHz, 7.2 MHz or 10.8 MHz to match that of the crystal oscillator being used.



OSC1	OSC2	OSCILLATOR FREQUENCY
0	0	3.6 MHz
1	0	4.5 MHz
0	1	7.2 MHz
1	1	10.8 MHz



C = 30 pF typ.

Figure 2

Note: 3.6 MHz (OSC1 = "0" and OSC2 = "0") is set when power is turned on. The crystal is not oscillating at this time because the system is in standby mode.

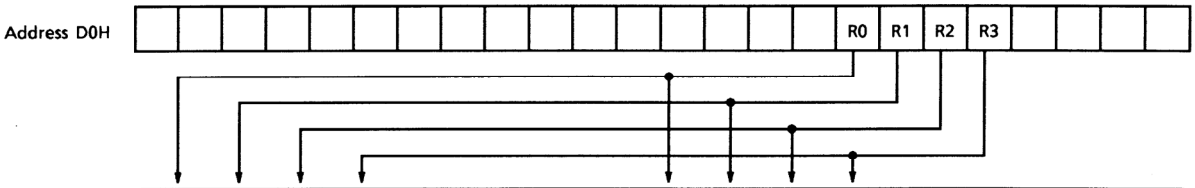
Reference Counter (Reference Frequency Divider)

The reference counter section consists of a crystal oscillator and a counter.

A crystal oscillator frequency of 3.6 MHz, 4.5 MHz, 7.2 MHz or 10.8 MHz can be selected. A maximum of 15 reference frequencies can be generated.

1. Setting Reference Frequency

The reference frequency is set using bits R0 to R3.



R0	R1	R2	R3	REFERENCE FREQUENCY	R0	R1	R2	R3	REFERENCE FREQUENCY
0	0	0	0	0.5 kHz	0	0	0	1	*7.8125 kHz
1	0	0	0	1 kHz	1	0	0	1	9 kHz
0	1	0	0	2.5 kHz	0	1	0	1	10 kHz
1	1	0	0	3 kHz	1	1	0	1	12.5 kHz
0	0	1	0	3.125 kHz	0	0	1	1	25 kHz
1	0	1	0	*3.90625 kHz	1	0	1	1	50 kHz
0	1	1	0	5 kHz	0	1	1	1	100 kHz
1	1	1	0	6.25 kHz	1	1	1	1	Standby mode (*1)

Note 1: Reference frequencies marked with an asterisk “*” can only be generated with a 4.5 MHz crystal oscillator.

Note 2: (*1) Standby mode

Standby mode occurs when bits R0, R1, R2 and R3 are all set to “1”. In standby mode, the programmable counter stops, and FM, AM and IF_{IN} (when IF_{IN} is selected) are set to “amp off” state (pins at “L” level). This saves current consumption when the radio is turned off. The DO pins become high impedance during standby mode.

During standby mode, the I/O ports (I/O-5 to I/O-9) and output ports (OT1 to OT4) can be controlled and the crystal oscillator can be turned on and off.

Note 3: The system is set to standby mode when power is turned on. At this time, the crystal oscillator is not oscillating and the I/O ports are set to input mode.

Programmable Counter

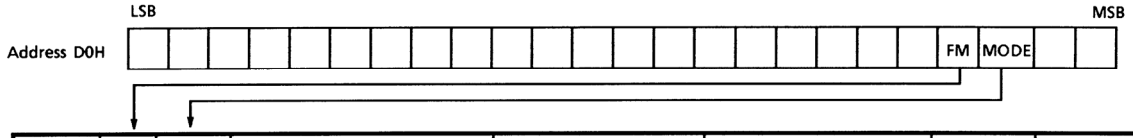
The programmable counter section consists of a 1/2 prescaler, a two-modulus prescaler and a 4 bit + 12 bit programmable binary counter.

1. Setting of Programmable Counter

16 bits of divisor data and 2 bits indicating the dividing mode are set in the programmable counter.

(1) Setting dividing mode

The FM and MODE bits are used to select the input pin and the dividing mode (pulse-swallow mode or direct dividing mode). There are fourtypes of mode, as shown in the table below. Select one based on the frequency band being used.

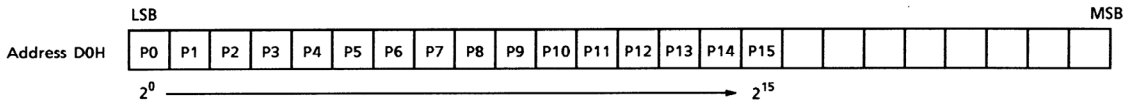


MODE	FM	MODE	DIVIDING MODE	TYPICAL RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT PIN	FREQUENCY
LF	0	0	Direct dividing mode	LW, MW, SWL	0.5 to 20 MHz	AM_{IN}	n
HF	0	1	Pulse-swallow mode	SWH	1 to 40 MHz		
FM_L	1	0		FM	30 to 130 MHz 30 to 150 MHz	FM_{IN}	
FM_H	1	1	1/2 + pulse-swallow mode	FM	30 to 130 MHz		2·n

(2) Setting divisor

The divisor for the programmable counter is set as binary data in bits P0 to P15.

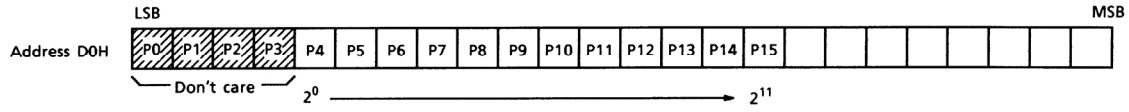
- Pulse-swallow mode (16 bits)



Divisor setting range (pulse-swallow mode): n = 210H to FFFFH (528 to 65535)

Note: In the 1/2 + pulse-swallow mode, the actual divisor is twice the programmed value.

- Direct dividing mode (12 bits)



Divisor setting range (direct dividing mode): n = 10H to FFFH (16 to 4095)
With the direct dividing mode, data P0 to P3 are don't-care and bit P4 is the LSB.

2. Prescaler and Programmable Counter Circuit Configuration

(1) Pulse-swallow mode circuit configuration

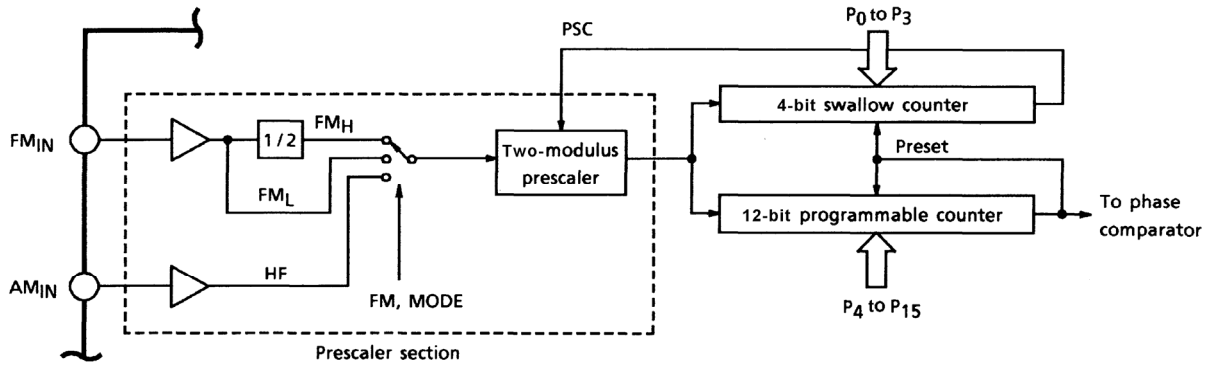


Figure 3

This circuit consists of a two-modulus prescaler, a 4-bit swallow counter and a 12-bit programmable counter. During FM_{IN} (FM_H mode), a 1/2 prescaler is added to the preceding step.

(2) Circuit configuration for the direct dividing method

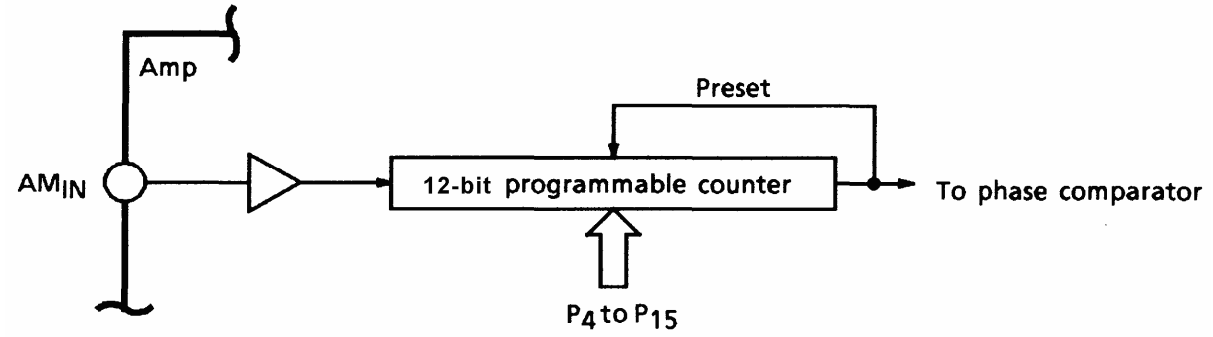


Figure 4

In the direct dividing mode, the prescaler section is bypassed and the 12-bit programmable counter is used.

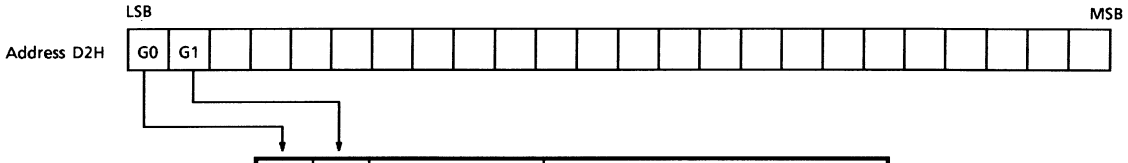
Note: Both FMIN and AMIN have built-in amps. Connecting a capacitor permits low-amplitude operation.

General-Purpose Counter

The general-purpose counter is a 20-bit counter. It has such uses as counting AM/FM band intermediate frequencies (IF) and detecting auto-stop signals during auto-search tuning. It also features a cycle measurement function for such uses as measuring low-frequency pilot signal cycles. The TC9256APG and TC9256AFG do not have the cycle measurement function (SC_{IN} mode). General-purpose counter pins can also be used as I/O ports.

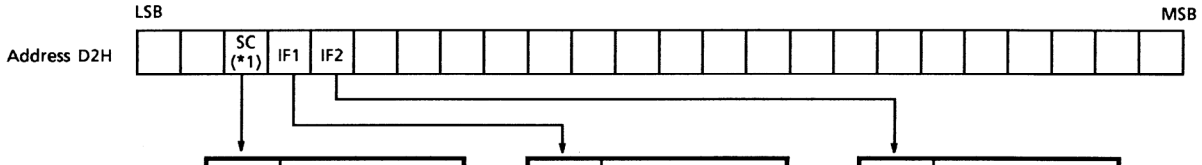
1. General-Purpose Counter Control Bits

(1) Bits G0 and G1 ..... Used for selecting the general-purpose counter gate time.



G0	G1	GATE TIME	CYCLE MEASUREMENT PULSE
0	0	1 ms	50 kHz
1	0	4 ms	150 kHz
0	1	16 ms	900 kHz
1	1	64 ms	Crystal oscillator frequency

(2) Bits SC, IF1 and IF2..... I/O port and general-purpose counter switching bits.
The functions of the following pins are switched by data.



SC (*1)	I/O-7 / SC_{IN} (*1)
1	SC_{IN}
0	I/O-7

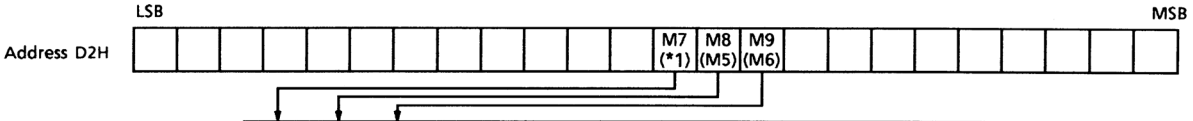
IF1	I/O-8 / IF_{IN1} (I/O-5 / IF_{IN1})
1	IF_{IN1}
0	I/O-8 (I/O-5)

IF2	I/O-9 / IF_{IN2} (I/O-6 / IF_{IN2})
1	IF_{IN2}
0	I/O-9 (I/O-6)

Note 1: Pin names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

Note 2: Bits marked with "(*1)" cannot be set on the TC9256APG and TC9256AFG.

(3) Bits M7, M8 and M9 ..... M7 (*1) sets the state for pin I/O-7/SC_{IN}; M8 (M5) sets the state for pin I/O-8/IF_{IN1}; M9 (M6), for pin I/O-9/IF_{IN2}.
These operations are valid when bits SC, IF1 and IF2 are all set to 1.



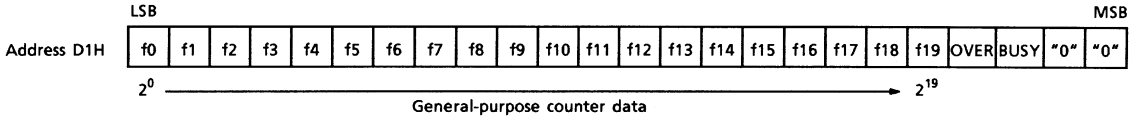
M7 (*1)	M8 (M5)	M9 (M6)	PIN STATES (When bits SC, IF1 and IF2 are all set to "1")		
			SC_{IN}	IF_{IN1}	IF_{IN2}
0	0	0	Input disabled	Input pulled down	Input pulled down
(*)	(*)	1			Input enabled
(*)	1	0		Input enabled	Input pulled down
1	0	0	Input enabled	Input pulled down	

Note1: Bits marked with an asterisk "(*)" are don't-care.

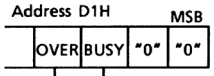
Note2: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

Note3: Bits marked with (*1) cannot be set on the TC9256APG and TC9256AFG.

(4) Bits f0 to f19 ..... The general-purpose counter results can be read in binary from bits f0 to f19 of the output register (D1H).



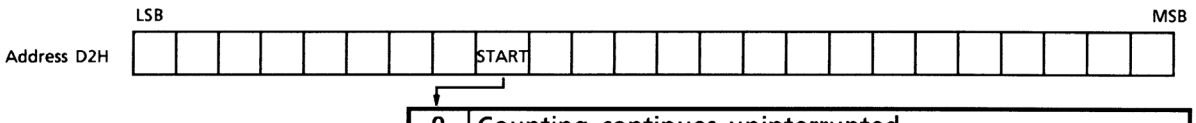
(5) OVER and BUSY bits ..... Detect the operating state of the general-purpose counter.



	BIT DATA = "1"	BIT DATA = "0"
General-purpose counter operation monitor bit	General-purpose counter busy	General-purpose counter ended counting
General-purpose counter overflow detection bit	Counted value in general-purpose counter $\geqq 2^{20}$ (Overflow state)	Counted value in general-purpose counter $\leqq 2^{20} - 1$

Note: When using the general-purpose counter, confirm that the BUSY bit is "0" (counting is ended) and the OVER bit is "0" (general-purpose counter data is normal) before referring to the contents of the general-purpose counter result bits (f0 to f19).

(6) START bit ..... When the data is set to "1", the general-purpose counter is reset; then counting start.



0	Counting continues uninterrupted.
1	Counting starts after general-purpose counter is reset.

2. General-Purpose Counter Circuit Configuration

The general-purpose counter section consists of input amps, a gate time control circuit and a 20-bit binary counter.

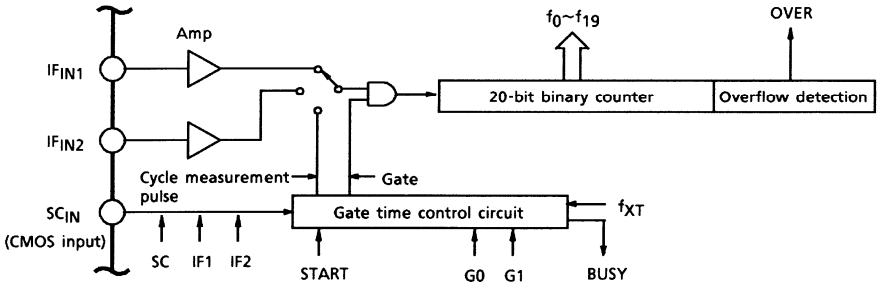
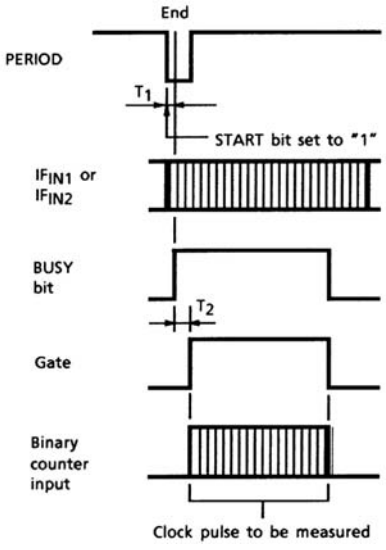
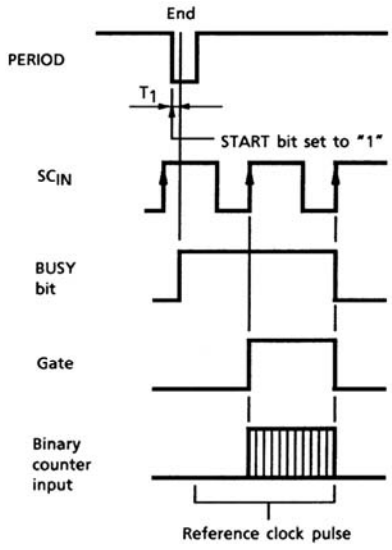


Figure 5

3. General-Purpose Counter Measurement Timing



Frequency Measurement Timing Chart



Cycle Measurement Timing Chart

$0 < T_1 \leqq 0.25$ (μs), $0 < T_2 \leqq 1$ (ms)

Figure 6

Note1: IF_{IN1} and IF_{IN2} input have built-in amps. Connecting a capacitor permits low-amplitude operation.

Note2: SC_{IN} is configured for CMOS input; therefore input signals should be logic level.

General-Purpose I/O Ports

These LSIs feature general-purpose output and I/O ports that are controlled through the serial ports.

Input/Output Form	TC9256APG, TC9256AFG	TC9257APG, TC9257AFG	Input/Output Configuration
Output ports	Dedicated: 3 ports Maximum: 4 ports (1 port for CMOS output)	Dedicated: 4 ports	N-channel open-drain output
I/O ports	Maximum: 2 ports	Dedicated: 1 port Maximum: 5 ports	CMOS input/output

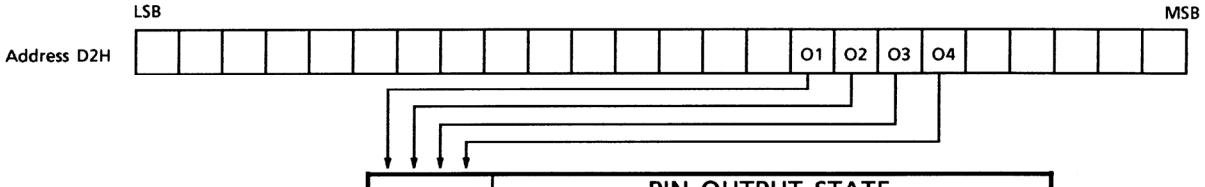
1. General-Purpose Output Ports (OT-1to OT-4)

Pins OT-1to OT-4 are general-purpose dedicated output ports used for control signal output. They are configured for N-channel open-drain output and have an off withstanding voltage of 12 V.

The data set in bits O1to O4 of the input register (D2H) are output in parallel from their corresponding dedicated output port pins OT-1to OT-4. The TC9256APG and TC9256AFG do not have the dedicated output port OT-4, but setting the input register (D2H) CLK (O4C) bit to "1" converts pin DO2 into an output port OT-4 (configured for CMOS output).

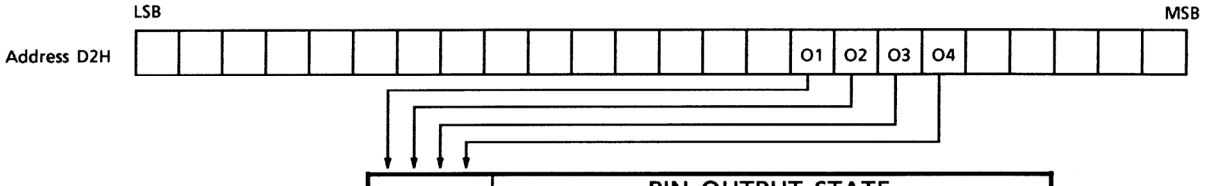
The data set in bits O1to O4 of the input register (D2H) can also be read from the DATA pins as output register (D3H) serial data O1to O4.

(1) TC9257APG and TC9257AFG



O1to O4	PIN OUTPUT STATE OT-1 to OT-4
0	High impedance (N-channel open drain output = off)
1	"L" level (N-channel open drain output = on)

(2) TC9256APG and TC9256AFG

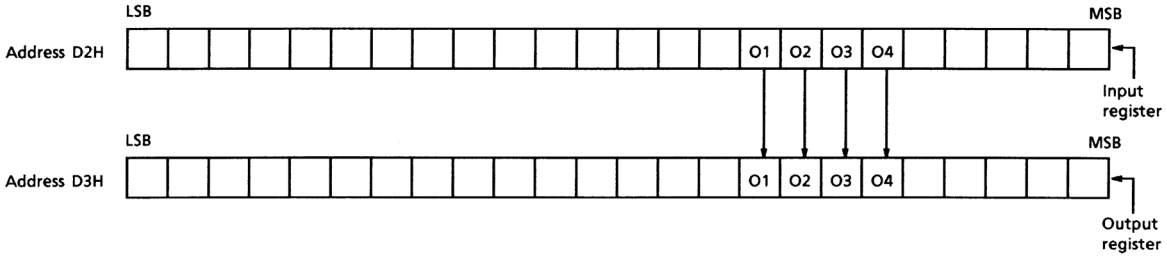


O1to O4	PIN OUTPUT STATE OT-1 to OT-4
0	High impedance (N-channel open drain output = off)
1	"L" level (N-channel open drain output = on)

Note 1: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

Note 2: (*1) indicates the output state when the DO2/OT-4 pin is switched for use as an OT-4 output pin (configured for CMOS output).

(3) Output register ..... The data set in bits O1 to O4 of the input register can be read as serial data O1 to O4 from the output register (D3H).



2. General-Purpose I/O Ports (I/O-5 to I/O-9)

Pins I/O-5 to I/O-9 are general-purpose I/O ports used for control signal input and output. They are configured for CMOS input and output.

These I/O ports are set for input or output using bits C5, C6 and M7 to M9 of the input register (D2H).

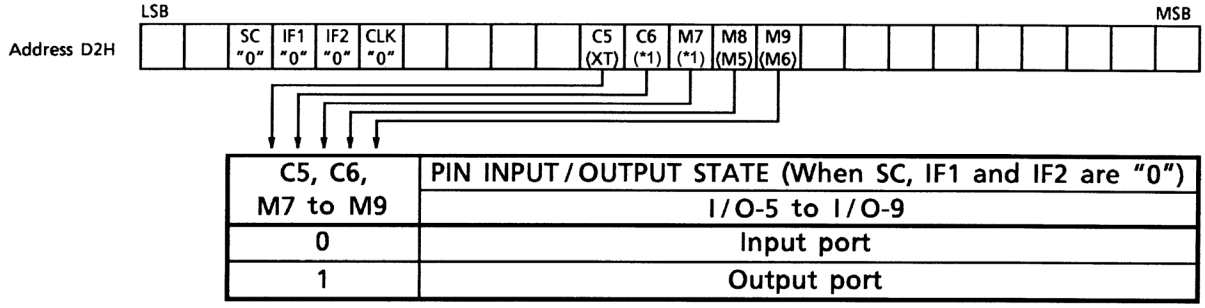
Setting bits C5, C6 and M7 to M9 to "0" sets these ports for input. Data input in parallel from I/O-5to I/O-9 are latched in the internal register at the ninth falling edge of the serial clock signal. The data can then be read as serial data I5 to I9 from the DATA pins.

Setting bits C5, C6 and M7 to M9 to "1" sets these ports for output.

Data set in bits O5 to O9 of the input register (D2H) is output in parallel from their corresponding general-purpose I/O port pins I/O-5 to I/O-9.

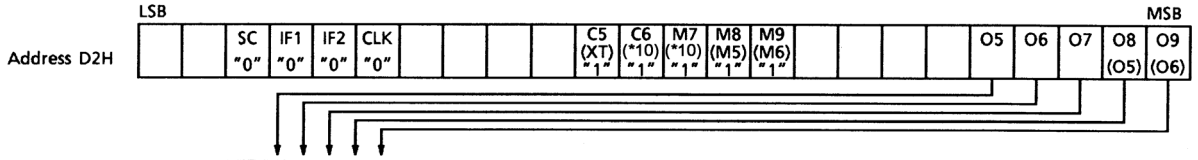
These operations are valid when bits SC, IF1, IF2 and CLK are all set to "0".

(1) TC9257APG and TC9257AFG



C5, C6, M7 to M9	PIN INPUT/OUTPUT STATE (When SC, IF1 and IF2 are "0")
	I/O-5 to I/O-9
0	Input port
1	Output port

- Setting data for output ports



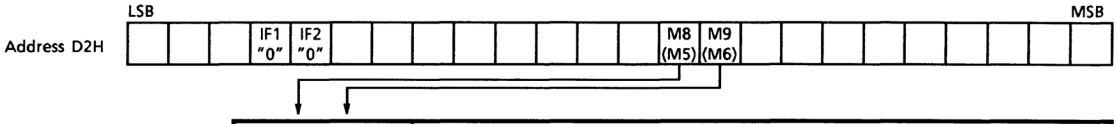
O5 to O9	PIN OUTPUT STATE (When SC, IF1 and IF2 are "0")
	I/O-5 to I/O-9
0	"L" level
1	"H" level

Note1: On TC9257APG and TC9257AFG, pins I/O-7to I/O-9 also serve as general-purpose counter input pins. Therefore, bits SC, IF1 and IF2 of the input register (D2H) must be set to "0" when pins I/O-7to I/O-9 are used for I/O ports. Since pin I/O-5 also serves as the CLK pin, the CLK bit of the input register (D2H) must be set to "0" when pin I/O-5 is used as an I/O port.

Note2: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

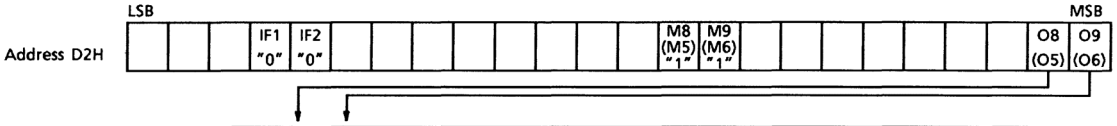
Note3: Bits marked with (*1) cannot be set on the TC9256APG and TC9256AFG.

(2) TC9256APG and TC9256AFG



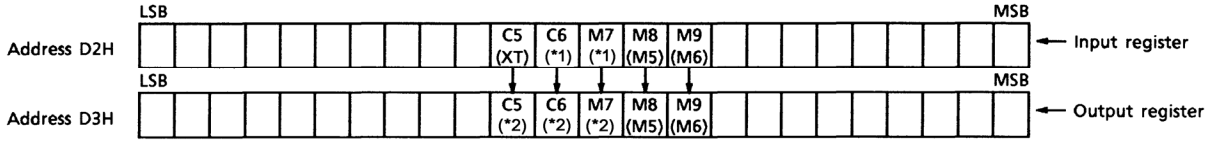
M5, M6	PIN INPUT / OUTPUT STATE (When IF1 and IF2 are "0")
	I/O-5, I/O-6
0	Input port
1	Output port

- Setting data for output ports

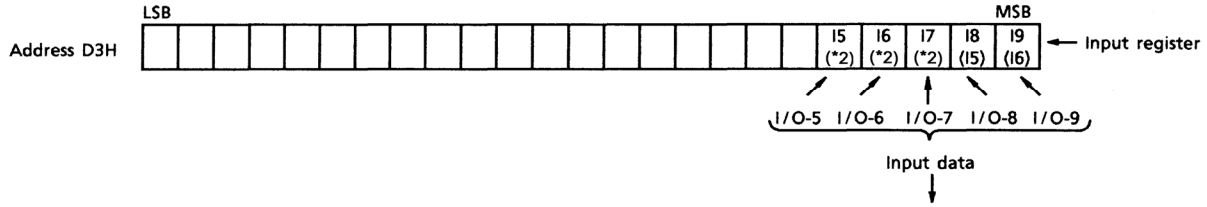


O5, O6	PIN OUTPUT STATE (When IF1 and IF2 are "0")
	I/O-5, I/O-6
0	"L" level
1	"H" level

(3) Output register ..... Data set in bits C5, C6 and M7to M9 of the input register (D2H) can be read as serial data C5, C6 and M7to M9 from the output register (D3H).



Data input in parallel from pins I/O-5 to I/O-9 can be read as serial data I5 to I9 from the output register (D3H).



INPUT PORTS (I/O-5 to I/O-9)	BIT DATA (I5 to I9)
"L" level	0
"H" level	1

Note1: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

Note2: Bits marked with (*1) cannot be set on the TC9256APG and TC9256AFG.

Data is "0" for bits marked with (*2) on the TC9256APG and TC9256AFG.

Note3: When pins I/O-5 to I/O-9 are used for output, the data in I5~I9 of the output register (D3H) is undefined.

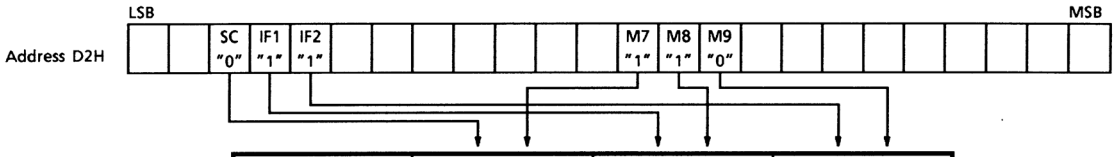
Note4: When power is turned on, input register (D2H) I/O port control bits C5, C6 and M7 to M9 and output data bits O5 to O9 are set to "0".

(General-purpose I/O ports are set as input ports. Pins used both as general-purpose I/O ports and general-purpose counter input are set for I/O port input. The output state of general-purpose output ports is set to high impedance (N-channel open drain output = off).

Note5: On TC9256APG and TC9256AFG, pins I/O-5 and I/O-6 also serve as general-purpose counter input pins. Therefore, bits IF1 and IF2 of input register 2 must be set to "0" when these pins are used as I/O ports.

A typical example of data setting for general-purpose counter and I/O port use is shown below.

- TC9257APG and TC9257AFG



PIN NAME	I/O-7 / SC_{IN}	I/O-8 / IF_{IN1}	I/O-9 / IF_{IN2}
Pin function	I/O-7	IF_{IN1}	IF_{IN2}
Pin input/ output state	Output port	Input enabled	Input pulled down

As shown above, the pins can be switched as required to enable use as an I/O port or general-purpose counter.

Phase Comparator

The phase comparator outputs the phase error after comparing the phase difference of the reference frequency signal supplied by the reference counter and the divided output from the programmable counter. The frequencies and phase differences of these two signals are then equalized by passing them through low-pass filters. These signals then control the VCOs.

The filter constants can be customized for FM and AM bands since the signals are output in parallel from the phase comparator then pass through the two tristate buffer pins, DO1 and DO2.

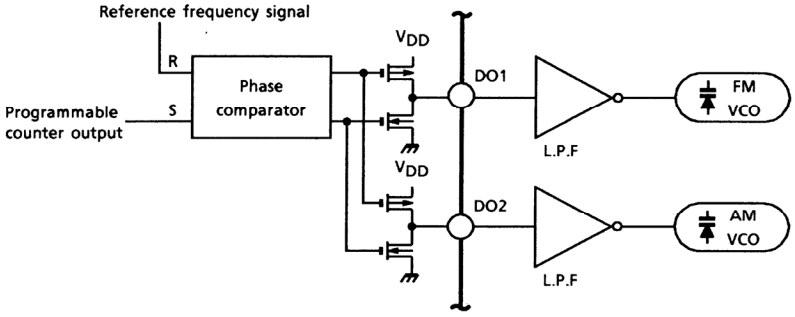


Figure 7

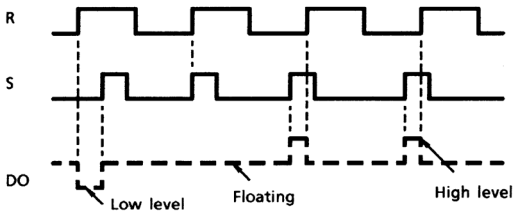


Figure 8 DO Output Timing Chart

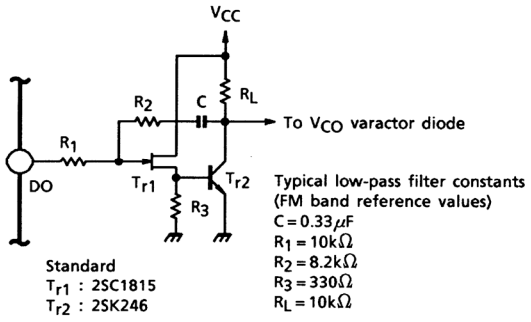


Figure 9 Typical Active Low-Pass Filter Circuit

The figures above show the DO output timing chart and a typical active low-pass filter circuit featuring a Darlington connection between the FET and transistor.

The filter circuit shown above is just one example. Actual circuits should be designed based on the band composition and the properties desired from the system.

Note: On the TC9256APG and TC9256AFG, pin DO2 can be switched for use as pin OT-4.

Lock Detection Bits

The lock detection bits detect locked states in the PLL system. These systems have an unlock detection bit (unlock bit), which is used to detect, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. These systems also have phase error detection bits (bits PE1to PE3), which are capable of more precise detection (±0.55 μs to ±7.15 μs).

1. Unlock Detection Bit (UNLOCK)

This bit detects, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. When there is no lock, that is, when the reference frequency and the divided output of the programmable counter are not the same, unlock F/F is set.

Unlock F/F is reset every time the input register (D2H) unlock reset bit (RESET) is set to "1".

After unlock F/F has been reset in this way, locked state can be detected by checking the unlock detection bit (UNLOCK) of the output register (D3H). After unlock F/F has been reset, the unlock detection bit must be checked after a time interval exceeding the reference frequency cycle. This is because the reference frequency cycle inputs the lock detection strobe to unlock F/F. If the time interval is short, the correct locked state cannot be detected. Therefore, the output register (D3H) has a lock enable bit (ENABLE). This bit is reset every time the input register (D2H) reset bit is set to "1", and set to "1" through the lock detection timing. That is, the locked state is correctly detected when the lock enable bit (ENABLE) is "1".

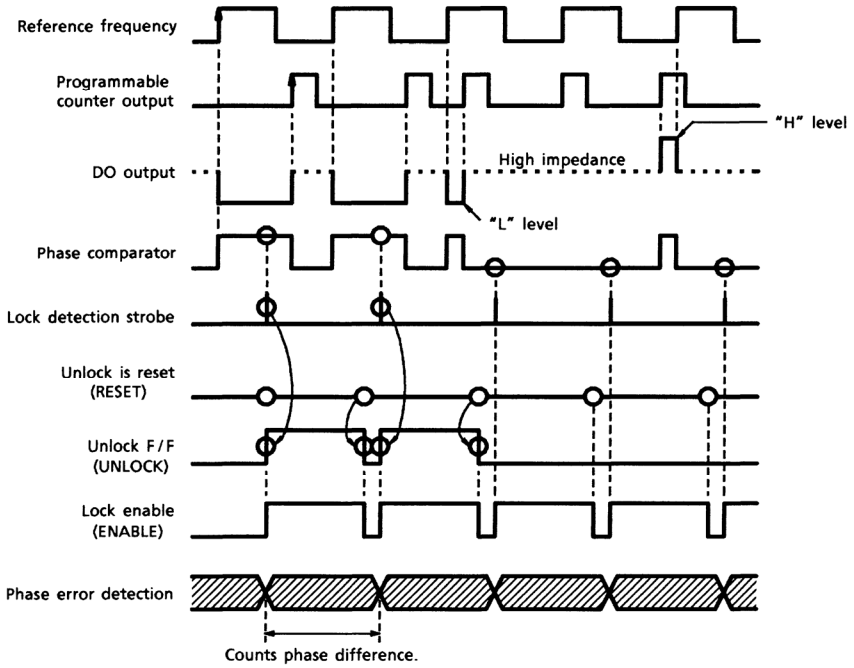
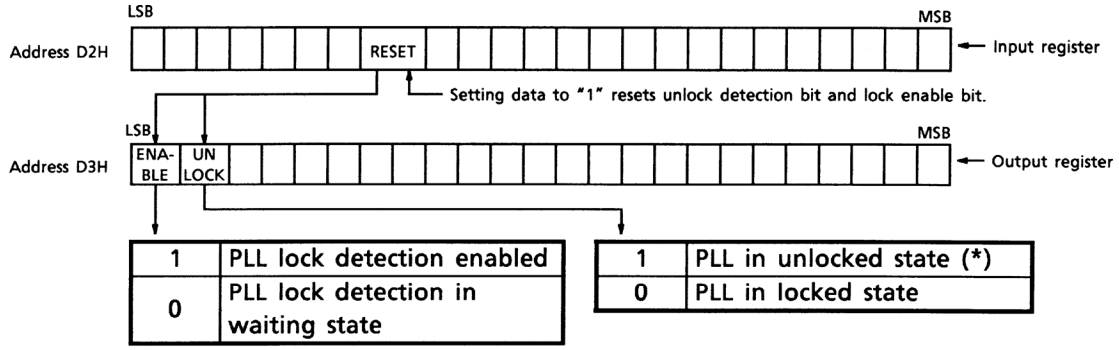


Figure 10



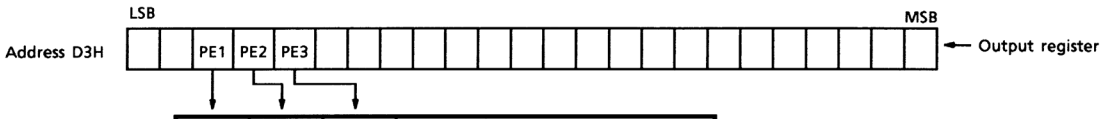
1	PLL lock detection enabled
0	PLL lock detection in waiting state

1	PLL in unlocked state (*)
0	PLL in locked state

Note: The asterisk "(*)" indicates an error state of over 180° phase difference relative to the reference frequency.

2. Phase Error Detection Bits (PE1to PE3)

The unlock bit detects, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. The phase error detection bits (bits PE1to PE3) are capable of precise phase error detection of ±0.55 to ±7.15 μs using the reference frequency cycle. (If the UNLOCK bit is set to "1" and the phase difference relative to the reference frequency is over 180°, bits PE1 to PE3 cannot correctly detect the phase error. Therefore, bits PE1to PE3 are normally used when the UNLOCK bit is set to "0".) Bits PE1to PE3 detects phase error normally when the phase difference is −180°to 180° relative to the reference frequency cycle.



PE1	PE2	PE3	PHASE ERROR (PE)
0	0	0	PE < ±0.55μs
0	0	1	±0.55μs ≦ PE < ±1.65μs
0	1	0	±1.65μs ≦ PE < ±2.75μs
0	1	1	±2.75μs ≦ PE < ±3.85μs
1	0	0	±3.85μs ≦ PE < ±4.95μs
1	0	1	±4.95μs ≦ PE < ±6.05μs
1	1	0	±6.05μs ≦ PE < ±7.15μs
1	1	1	±7.15μs ≦ PE

The phase error data can be read from the output register (D3H) as serial data PE1 to PE3.

The following is a typical lock detection operation. It shows the operation flow from locked state to frequency change with a phase error greater than ±4.95 μs and less than ±6.05 μs.

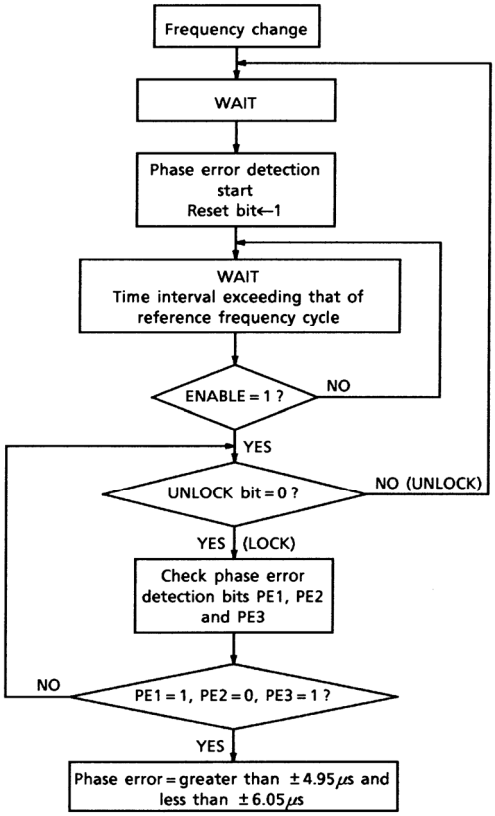


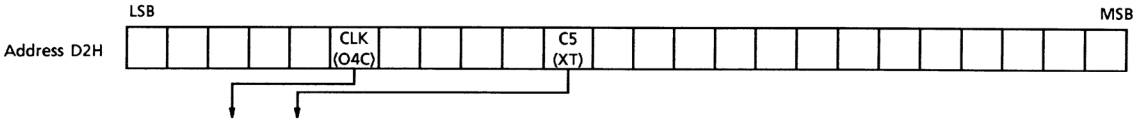
Figure 11

Other Control Bits

1. CLK (O4C) and C5 (XT) Bits ..... Control bits that switch the function for the I/O-5/CLK pin on the TC9257APG and TC9257AFG, and the OT-4/DO2 pin on the TC9256APG and TC9256AFG.

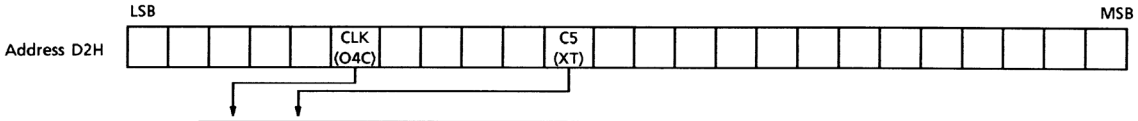
(1) On the TC9257APG and TC9257AFG, the CLK bit controls switching of the I/O-5 pin and CLK pin.

- When bits R0 to R3 of the input register (D0H) are all set to "1" (standby mode)



CLK	C5	I/O-5/CLK PIN STATE		CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	I/O port	Input port	Oscillator circuit off
0	1		Output port	
1	0	CLK output	System clock off (CLK at "L" level)	Oscillator circuit on
1	1		System clock output (*)	

- When one of bits R0 to R3 of the input register (D0H) is set to "0" (not standby mode)



CLK	C5	I/O-5/CLK PIN STATE		CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	I/O port	Input port	Oscillator circuit on
0	1		Output port	
1	0	CLK output	System clock output (*)	
1	1			

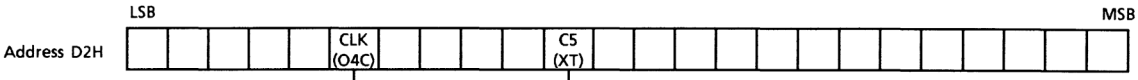
Note1: The system clock output marked with an asterisk "(*)" refers to output of the crystal oscillator frequencies listed below.

Crystal Oscillator (MHz)	System Clock (kHz)	Duty (%)
10.8	600	50
7.2		
3.6		
4.5	750	

Note2: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

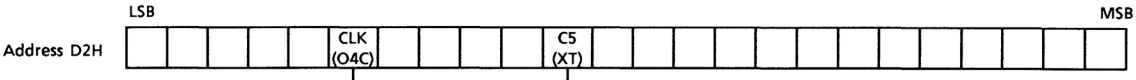
(2) On the TC9256APG and TC9256AFG, the O4C bit controls switching of the DO2 pin and OT-4 pin.

- When bits R0 to R3 of the input register (D0H) are all set to "1" (standby mode)



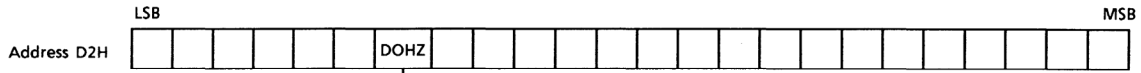
O4C	XT	DO2 / OT-4 PIN STATE	CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	DO2 output	Oscillator circuit off
0	1		Oscillator circuit on
1	0	OT-4 output	Oscillator circuit off
1	1		Oscillator circuit on

- When one of bits R0 to R3 of the input register (D0H) is set to "0" (not standby mode)



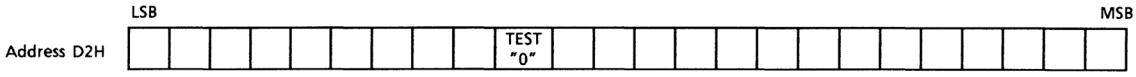
O4C	XT	DO2 / OT-4 PIN STATE	CRYSTAL OSCILLATOR CIRCUIT STATE
0	0	DO2 output	Oscillator circuit on
0	1		
1	0	OT-4 output	
1	1		

2. DOHZ Bit ..... Controls the DO2 pin output state.



0	DO2 output in normal operation (phase comparison error output)
1	DO2 output fixed at high impedance

3. TEST Bit ..... Data should normally be set to "0".



Note: Bit names in parentheses "( )" apply to the TC9256APG and TC9256AFG.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
N-ch open-drain OFF withstanding voltage	V_{OFF}	13	V
Power dissipation	P_D	300 (200)	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

( ): Flat package

Electrical Characteristics (unless otherwise specified, Ta = –40 to 85°C, V_{DD} = 4.5 to5.5 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Operating power supply voltage	V_{DD1}	—	PLL operation (normaloperation)	4.5	5.0	5.5	V
Operating power supply current	I_{DD1}	—	V_{DD} = 5.0 V, XT = 10.8 MHz, FM_{IN} = 150 MHz	—	7	15	mA

Standby mode

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Crystal oscillation frequency supply voltage	V_{DD2}	—	PLL OFF (operating crystal oscillation)	4.0	5.0	5.5	V
Operating power supply current	I_{DD2}	—	V_{DD} = 5.0 V, XT = 10.8 MHz, PLL OFF	—	0.8	1.5	mA
Operating power supply current	I_{DD3}	—	V_{DD} = 5.0 V, XT stop, PLL OFF	—	120	240	μA

Operating frequency range

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Crystal oscillation frequency	f_{XT}	—	Connect crystal resonator to XT- XT pin	3.6	~	10.8	MHz
FM_{IN} (FM_H, FM_L)	f_{FM}	—	FM_H, FM_L mode, V_{IN} = 0.2 V_{p-p}	30	~	130	MHz
FM_{IN} (FM_L)	f_{FML}	—	FM_L mode, V_{IN} = 0.3 V_{p-p}	30	~	150	MHz
AM_{IN} (HF)	f_{HF}	—	HF mode, V_{IN} = 0.2 V_{p-p}	1	~	40	MHz
AM_{IN} (LF)	f_{LF}	—	LF mode, V_{IN} = 0.2 V_{p-p}	0.5	~	20	MHz
IF_{IN1}, IF_{IN2}	f_{IF}	—	V_{IN} = 0.2 V_{p-p}	0.1	~	15	MHz
SC_{IN}	f_{SC}	—	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, Square wave input	—	~	100	kHz

Operating input amplitude range

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
FM_{IN} (FM_H, FM_L)	V_{FM}	—	FM_H, FM_L mode, f_{IN} = 30 to 130 MHz	0.2	~	V_{DD} – 0.5	V_{p-p}
FM_{IN} (FM_L)	V_{FML}	—	FM_L mode, f_{IN} = 30 to 150 MHz	0.3	~	V_{DD} – 0.5	V_{p-p}
AM_{IN} (HF)	V_{HF}	—	HF mode, f_{IN} = 1 to 40 MHz	0.2	~	V_{DD} – 0.5	V_{p-p}
AM_{IN} (LF)	V_{LF}	—	LF mode, f_{IN} = 0.5 to 20 MHz	0.2	~	V_{DD} – 0.5	V_{p-p}
IF_{IN1}, IF_{IN2}	V_{IF}	—	f_{IN} = 0.1 to 15 MHz	0.2	~	V_{DD} – 0.5	V_{p-p}

OT1 to OT4 N-ch open drain

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Output current	“L” level	I_{OL1}	—	V_{OL} = 1.0 V	5.0	10.0	—	mA
OFF-leak current		I_{OFF}	—	V_{OFF} = 12 V	—	—	2.0	μA

I/O-5 to I/O-9, SC_{IN}

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Input voltage	“H” level	V_{IH1}	—	—	0.7 V_{DD}	~	V_{DD}	V
	“L” level	V_{IL1}		—	0	~	0.3 V_{DD}	
Input current	“H” level	I_{IH}	—	V_{IH} = 5 V	—	—	2.0	μA
	“L” level	I_{IL}		V_{IL} = 0 V	—	—	–2.0	
Output current	“H” level	I_{OH4}	—	V_{OH} = 4.0 V (except SC_{IN})	–2.0	–4.0	—	mA
	“L” level	I_{OL4}		V_{OL} = 1.0 V (except SC_{IN})	2.0	4.0	—	

PERIOD, CLOCK, DATA

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Input voltage	“H” level	V_{IH2}	—	—	0.8 V_{DD}	~	V_{DD}	V
	“L” level	V_{IL2}		—	0	~	0.2 V_{DD}	
Input current	“H” level	I_{IH}	—	V_{IH} = 5 V	—	—	2.0	μA
	“L” level	I_{IL}		V_{IL} = 0 V	—	—	–2.0	
Output current	“H” level	I_{OH5}	—	V_{OH} = 4.0 V (DATA)	–1.0	–3.0	—	mA
	“L” level	I_{OL5}		V_{OL} = 1.0 V (DATA)	1.0	3.0	—	

DO1, DO2

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Input current	"H" level	I_{OH3}	—	V_{OH} = 4.0 V	−2.0	−4.0	—	mA
	"L" level	I_{OL3}		V_{OL} = 1.0 V	2.0	4.0	—	
Tristate lead current		I_{TL}	—	V_{TLH} = 5 V, V_{TLL} = 0 V	—	—	±1.0	μA

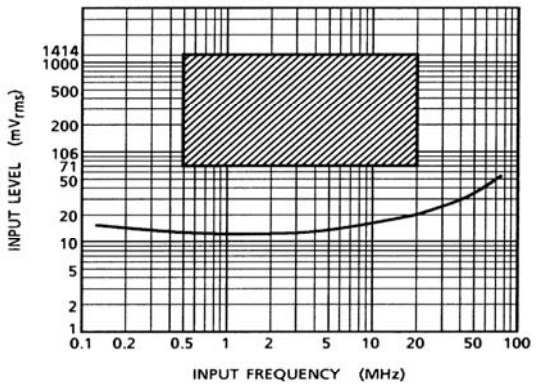
$\overline{XT}$

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Output current	"H" level	I_{OH2}	—	V_{OH} = 4.0 V	−0.1	−0.3	—	mA
	"L" level	I_{OL2}		V_{OL} = 1.0 V	0.1	0.3	—	

Input feedback resistance

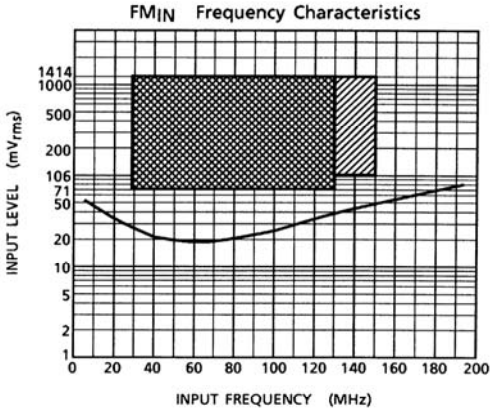
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Input feedback resistance	Rf1	—	FM_{IN}, AM_{IN}, IF_{IN} (Ta = 25°C)	350	700	1400	kΩ
	Rf2		XT- $\overline{XT}$ (Ta = 25°C)	500	1000	4000	

AM_{IN} (LF) Frequency Characteristics



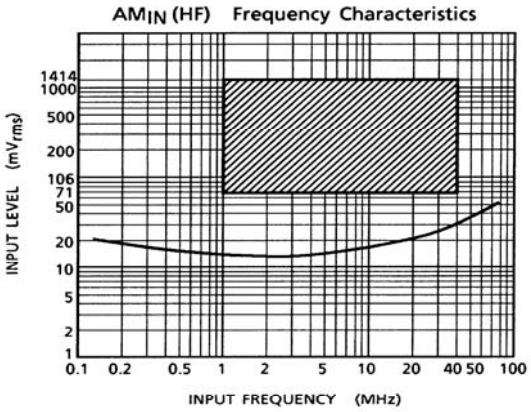
(Note) Operating Guarantee Range (V_{DD} = 4.5 to 5.5 V, Ta = −40 to 85°C)
Standard Characteristics (V_{DD} = 5 V, Ta = 25°C)

FM_{IN} Frequency Characteristics



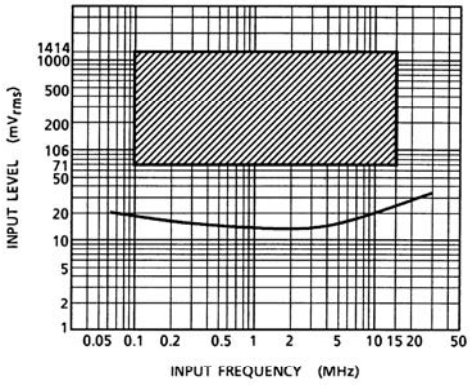
(Note) FM_{IN} : FM_H + FM_{IN} : FM_L } Operating Guarantee Range (V_{DD} = 4.5 to 5.5 V, Ta = −40 to 85°C)
Standard Characteristics (V_{DD} = 5 V, Ta = 25°C)

AM_{IN} (HF) Frequency Characteristics



(Note) Operating Gaurantee Range (V_{DD} = 4.5 to 5.5 V, Ta = −40 to 85°C)
Standard Characteristics (V_{DD} = 5 V, Ta = 25°C)

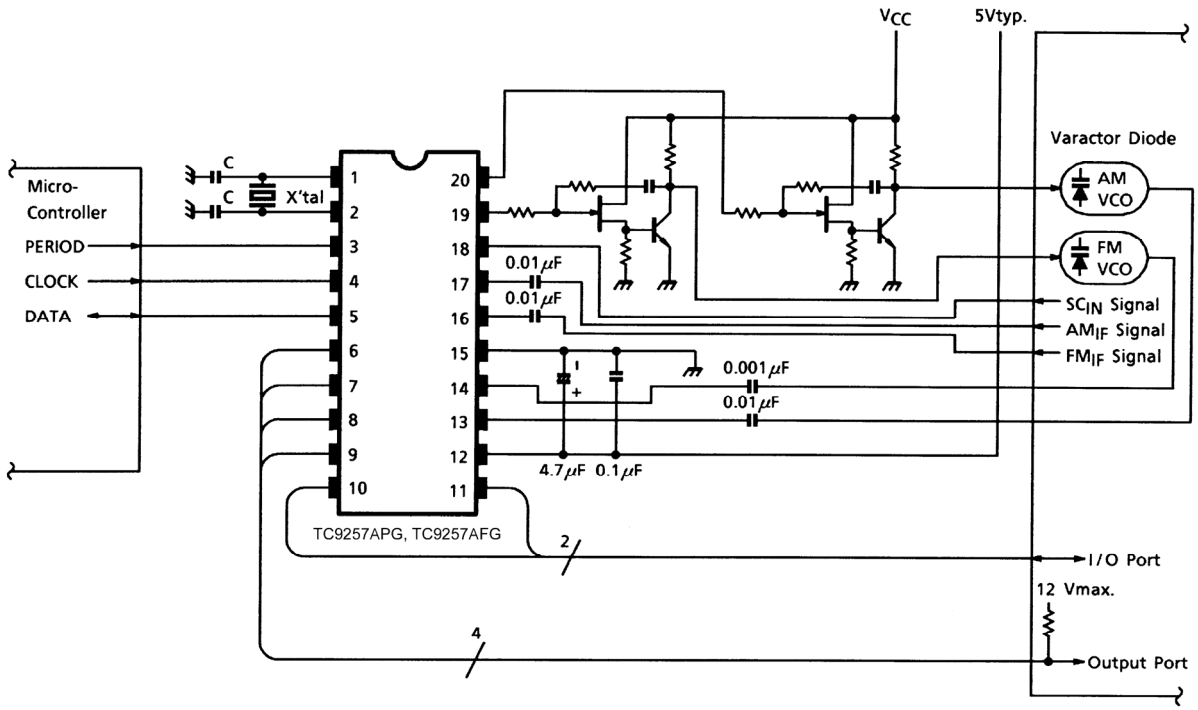
IF_{IN} Frequency Characteristics



(Note) Operating Guarantee Range (V_{DD} = 4.5 to 5.5 V, Ta = −40 to 85°C)
Standard Characteristics (V_{DD} = 5 V, Ta = 25°C)

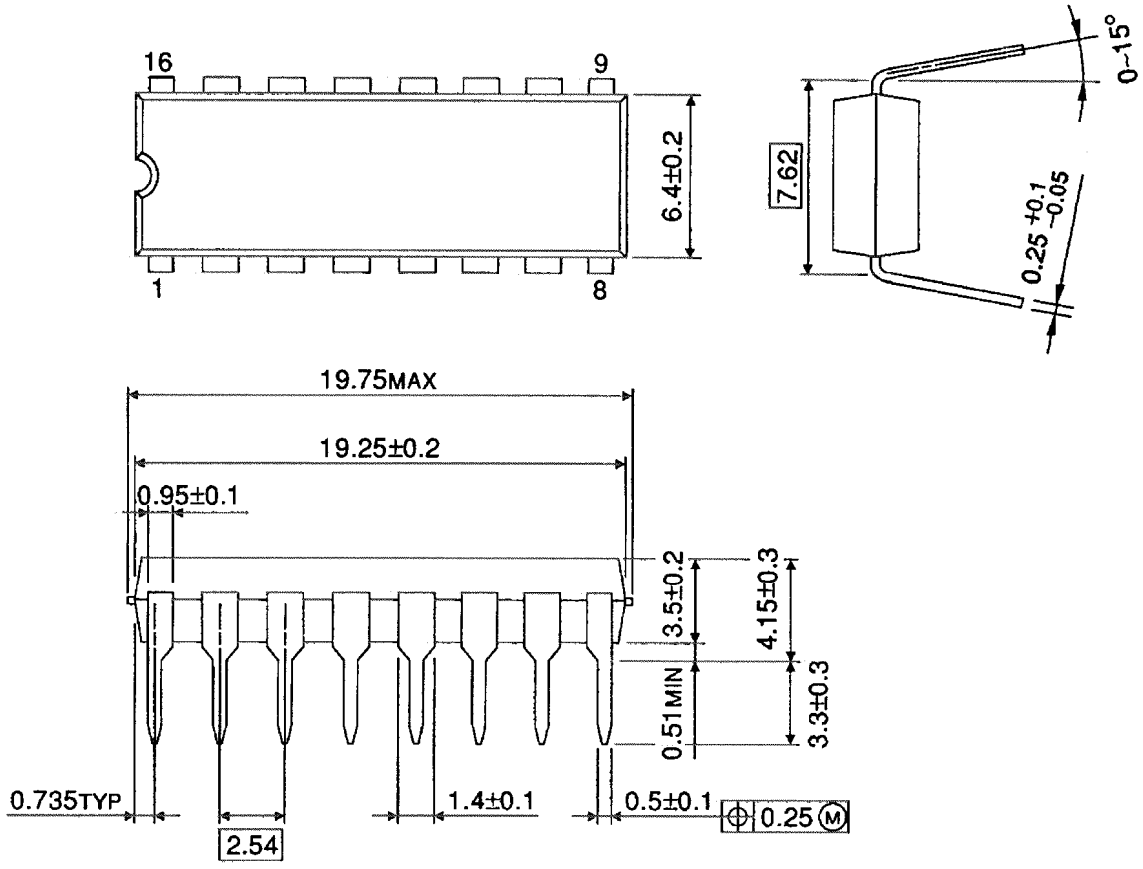
Application Circuit

(Sample circuit containing TC9257APG and TC9257AFG)



Package Dimensions

P-DIP16-300-2.54A Unit : mm

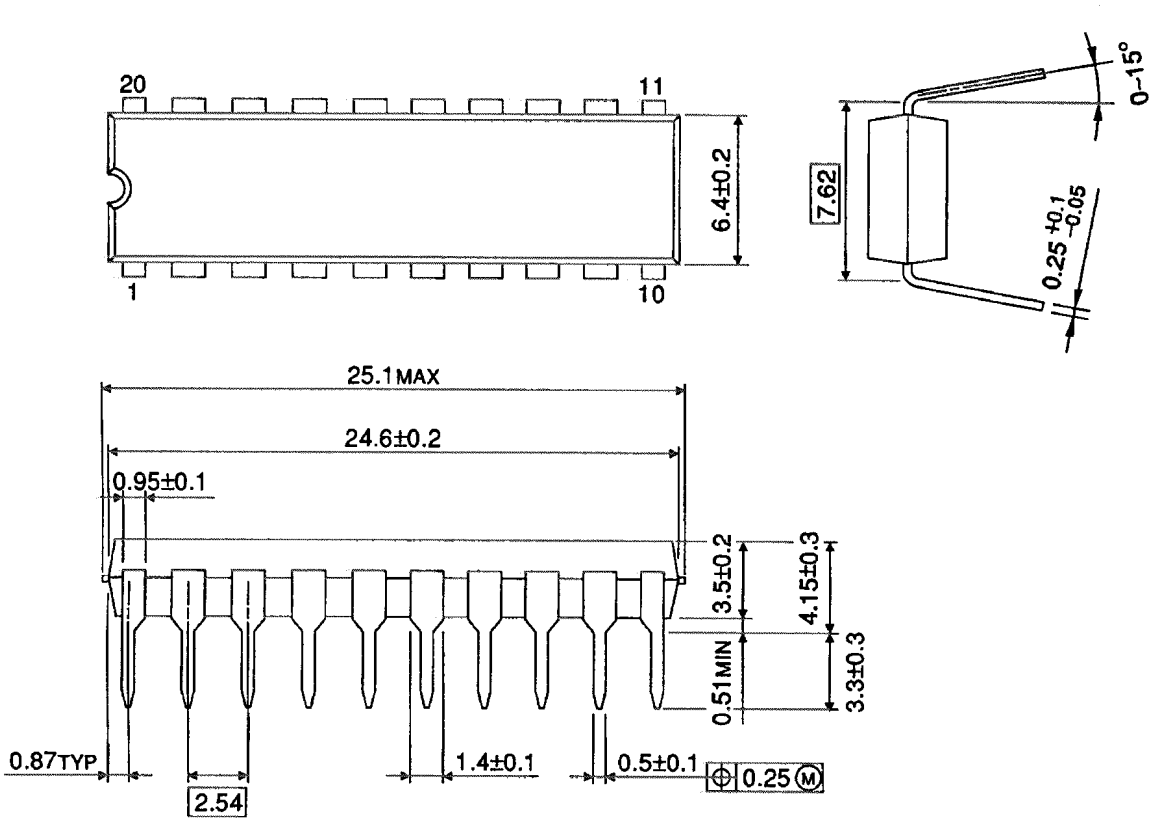


Weight: 1.0 g (typ.)

(Note): Palladium plate

Package Dimensions

P-DIP20-300-2.54A Unit : mm

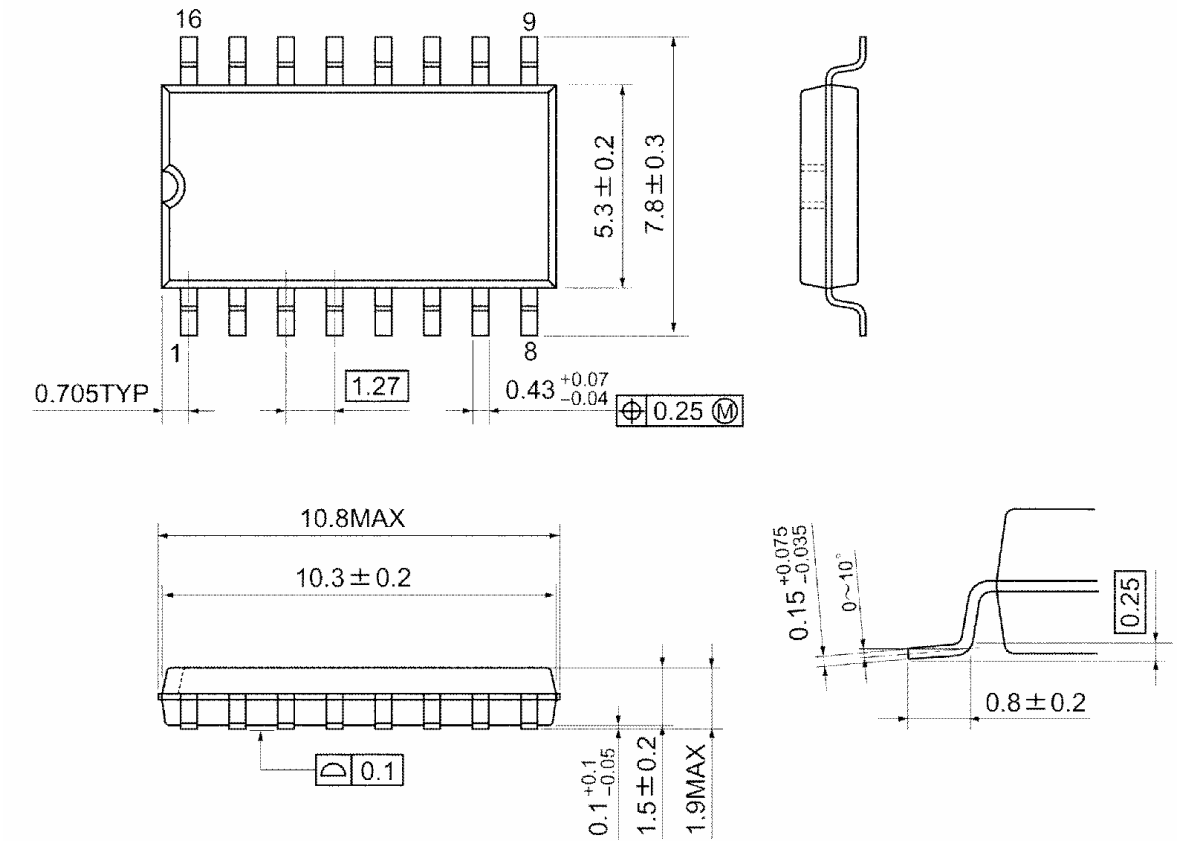


Weight: 1.24 g (typ.)

(Note): Palladium plate

Package Dimensions

P-SOP16-300-1.27A **Unit : mm**

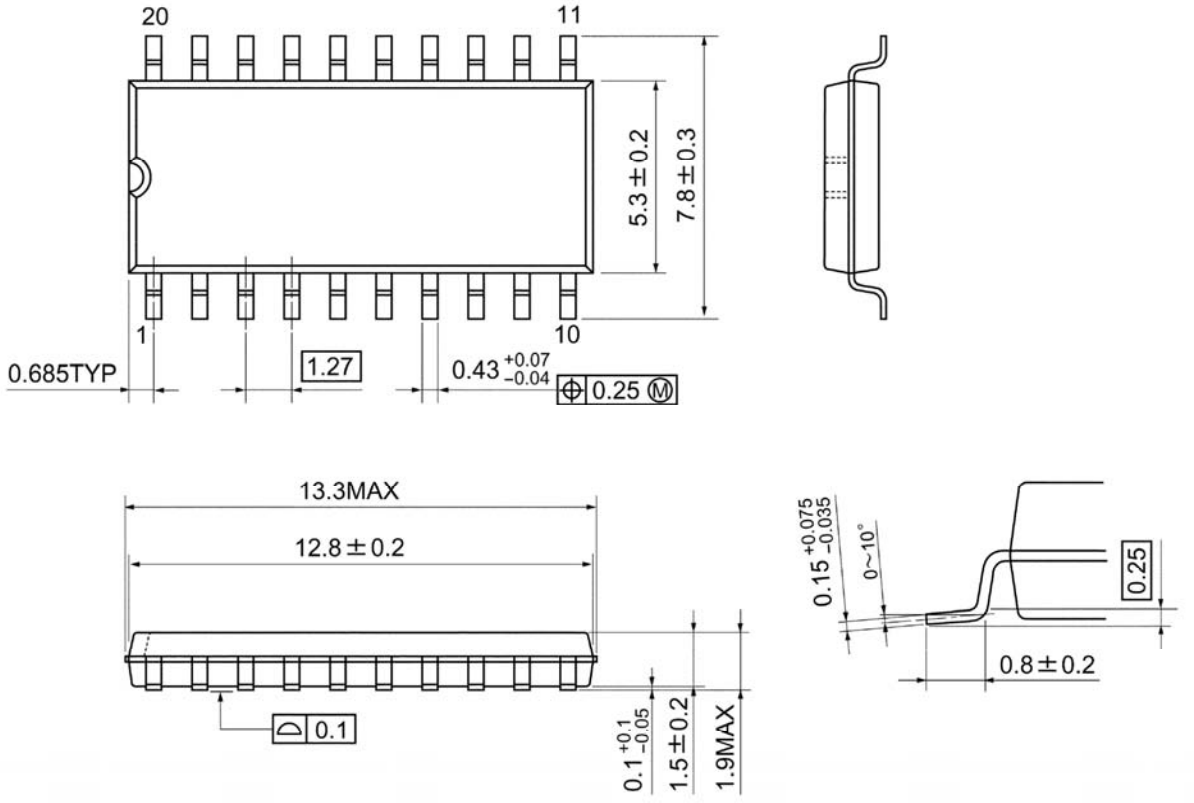


Weight: 0.16 g (typ.)

(Note): Palladium plate

Package Dimensions

P-SOP20-300-1.27A **Unit : mm**



Weight: 0.48 g (typ.)

(Note): Palladium plate

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060116EBA

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About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux