

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4015BP, TC4015BF, TC4015BFN

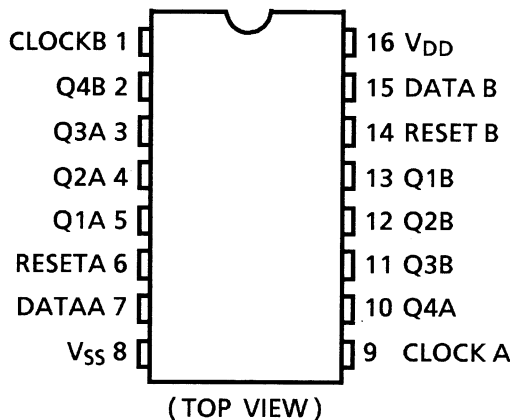
TC4015B Dual 4-Stage Static Shift Register (with serial input/parallel output)

TC4015B contains two circuits of 4 stage shift registers and the independent output is driven from each stage. As all the D type flip-flops of every stage have common RESET input, asynchronous clear operation can be achieved by an external signal at arbitrary timing. The flip-flop of each stage is triggered by rising edge of CLOCK input.

RESET input of "H" level resets the contents of all the stages to "L" regardless of CLOCK and DATA inputs and all of data outputs Q1 through Q4 become "L".

This can be used for converting serial data to parallel one and for ring counters of any numbering systems.

Pin Assignment



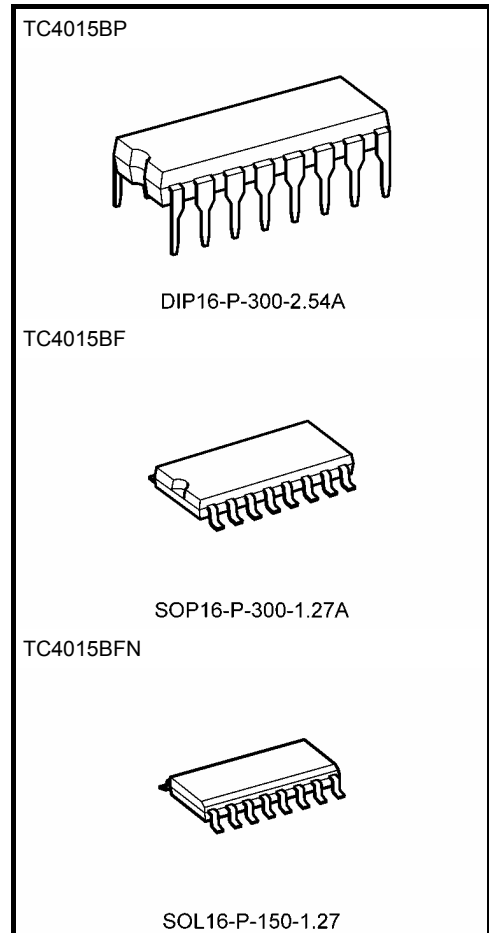
Truth Table

Inputs			Outputs			
CLOCK Δ	DATA	RESET	Q1	Q2	Q3	Q4
	L	L	L	Q1	Q2	Q3
	H	L	H	Q1	Q2	Q3
	*	L	No Change			
*	*	H	L	L	L	L

Δ : Level change

*: Don't care

Note: xxxFN (JEDEC SOP) is not available in Japan.

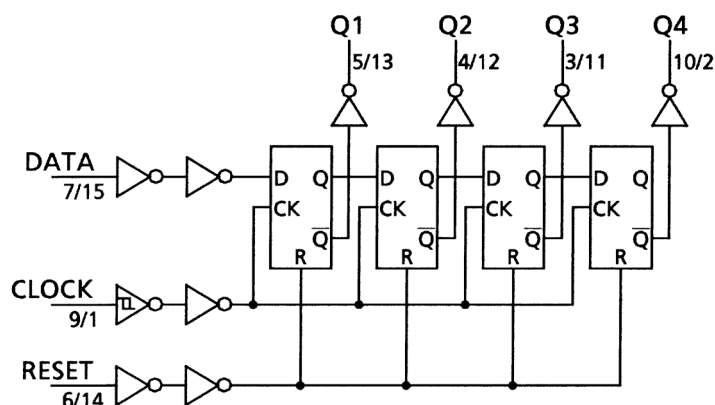


Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

Logic Diagram

1/2 TC4015B



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC input current	I_{IN}	± 10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges ($V_{SS} = 0 \text{ V}$) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics ($V_{SS} = 0$ V)

Characteristics	Sym- bol	Test Condition	V_{DD} (V)	-40°C		25°C			85°C		Unit
				Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage	V_{OH}	$ I_{OUT} < 1 \mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage	V_{OL}	$ I_{OUT} < 1 \mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output high current	I_{OH}	$V_{OH} = 4.6$ V	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5$ V	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5$ V	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5$ V	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output low current	I_{OL}	$V_{OL} = 0.4$ V	5	0.61	—	0.51	1.2	—	0.42	—	mA
		$V_{OL} = 0.5$ V	10	1.50	—	1.30	3.2	—	1.10	—	
		$V_{OL} = 1.5$ V	15	4.00	—	3.40	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage	V_{IH}	$V_{OUT} = 0.5$ V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0$ V, 9.0 V	10	7.0	—	7.0	5.50	—	7.0	—	
		$V_{OUT} = 1.5$ V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT} < 1 \mu A$									
Input low voltage	V_{IL}	$V_{OUT} = 0.5$ V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0$ V, 9.0 V	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5$ V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT} < 1 \mu A$									
Input current	"H" level	I_{IH}	$V_{IH} = 18$ V	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" level	I_{IL}	$V_{IL} = 0$ V	18	—	-0.1	—	-10^{-5}	-0.1	—	
Quiescent supply current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	5	—	0.005	5	—	150	μA
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	

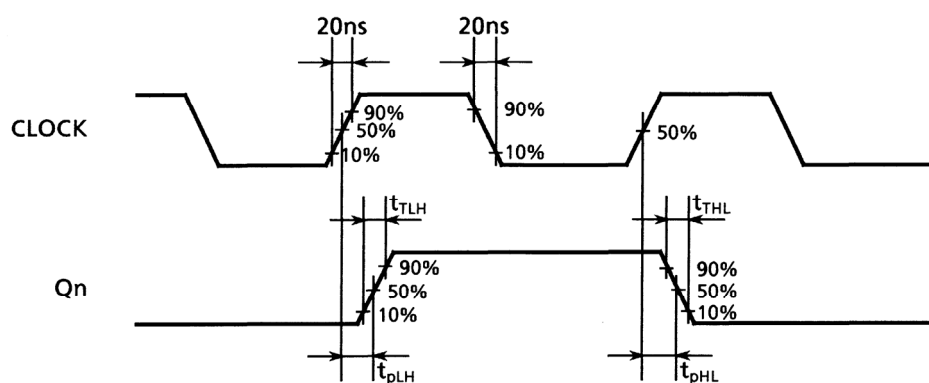
Note: All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

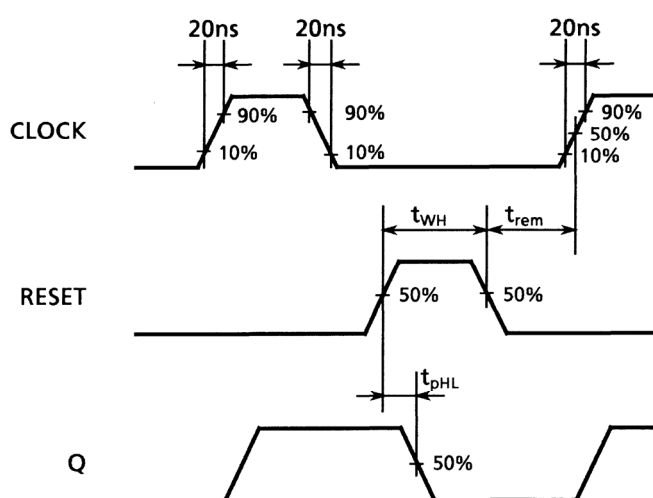
Characteristics	Symbol	Test Condition	V _{DD} (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t _{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output transition time (high to low)	t _{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time (CLOCK-Q)	t _{pLH} t _{pHL}	—	5	—	130	320	ns
			10	—	60	160	
			15	—	50	120	
Propagation delay time (RESET-Q)	t _{pHL}	—	5	—	90	400	ns
			10	—	45	200	
			15	—	40	160	
Max clock frequency	f _{CL}	—	5	3.0	8	—	MHz
			10	6.0	17	—	
			15	8.5	20	—	
Min clock pulse width	t _w	—	5	—	35	180	ns
			10	—	25	80	
			15	—	20	50	
Min pulse width (RESET)	t _{WH}	—	5	—	50	200	ns
			10	—	25	80	
			15	—	20	60	
Min set-up time (DATA-CLOCK)	t _{SU}	—	5	—	8	70	ns
			10	—	4	40	
			15	—	0	30	
Min hold time (DATA-CLOCK)	t _H	—	5	—	6	60	ns
			10	—	5	30	
			15	—	4	20	
Min removal time (RESET-CLOCK)	t _{rem}	—	5	—	0	80	ns
			10	—	0	30	
			15	—	0	20	
Max clock input rise time	t _{rCL}	—	5	No limit			μs
Max clock input fall time	t _{fCL}		10				
			15				
Input capacitance	C _{IN}	—		—	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics

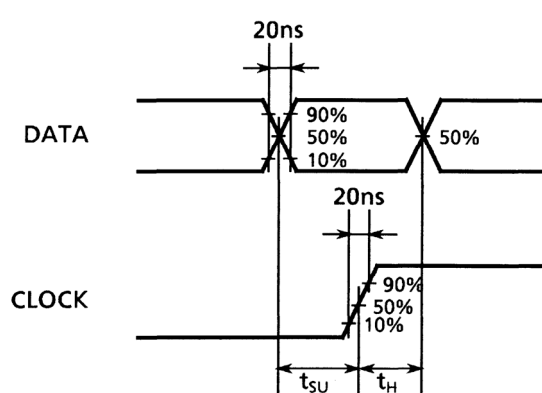
Waveform 1



Waveform 2



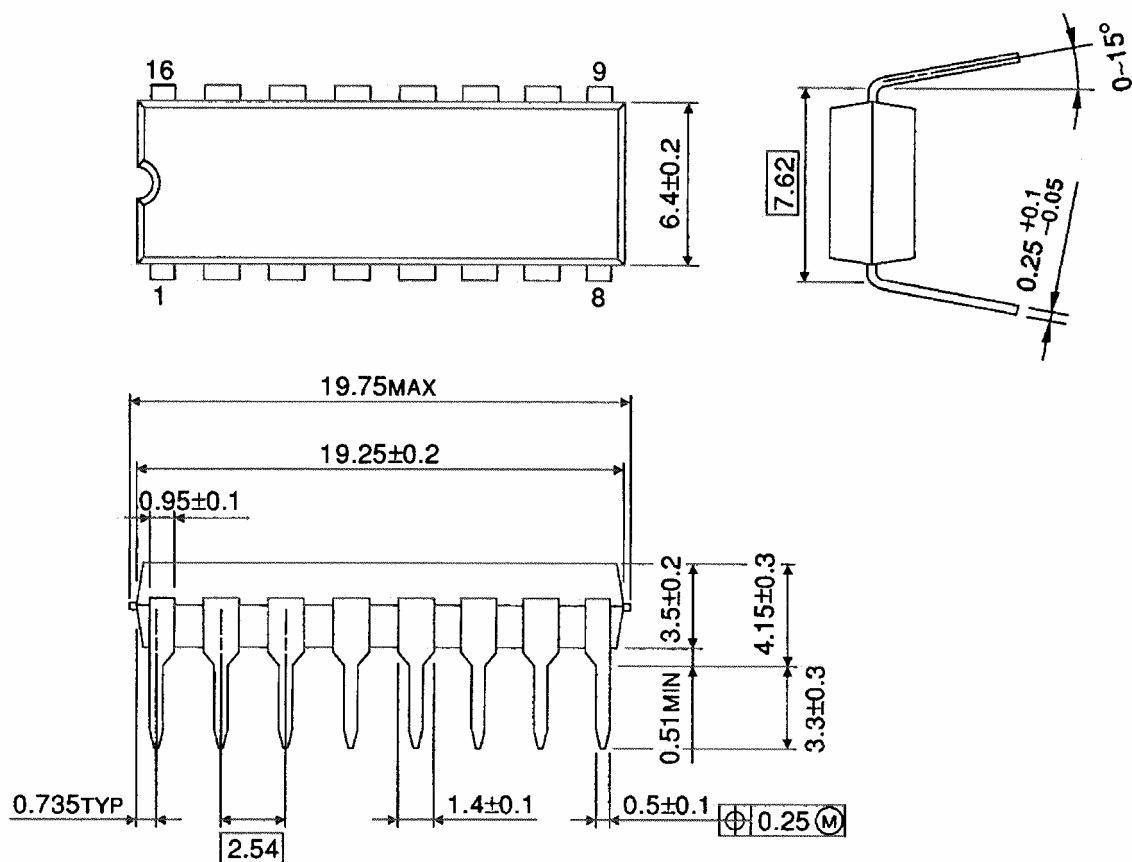
Waveform 3



Package Dimensions

DIP16-P-300-2.54A

Unit : mm

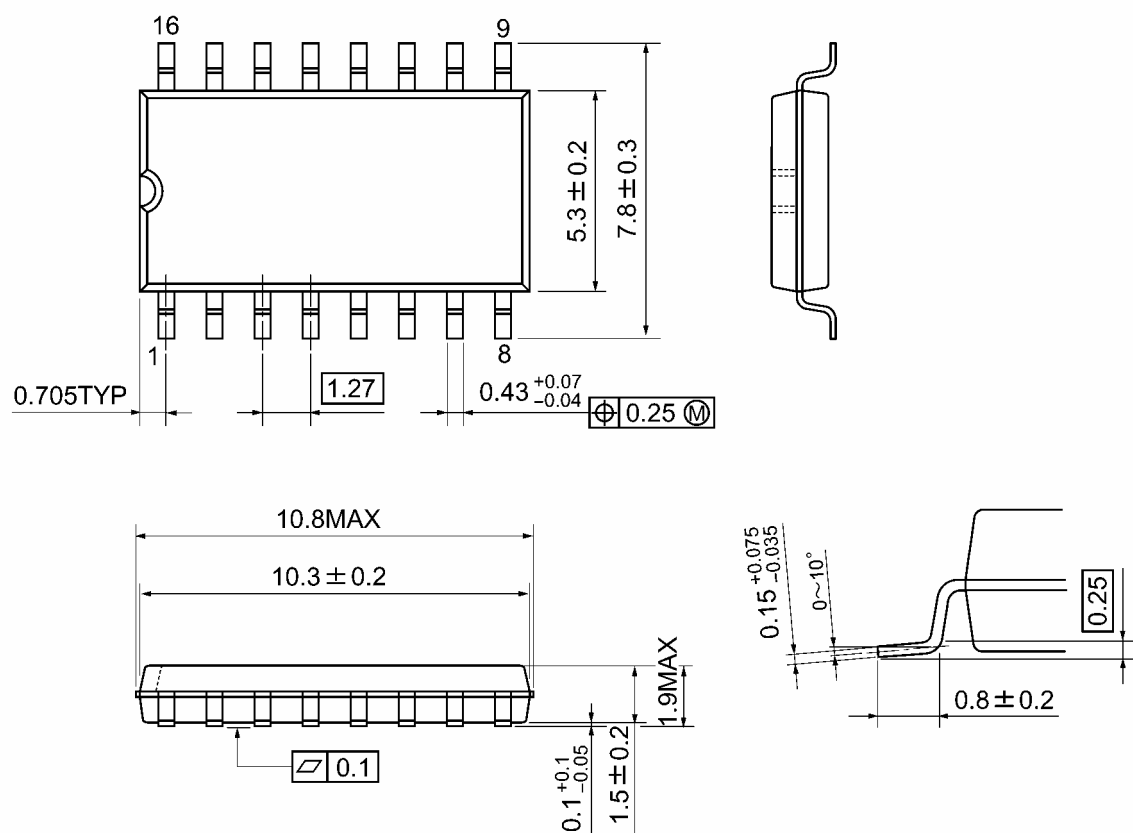


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

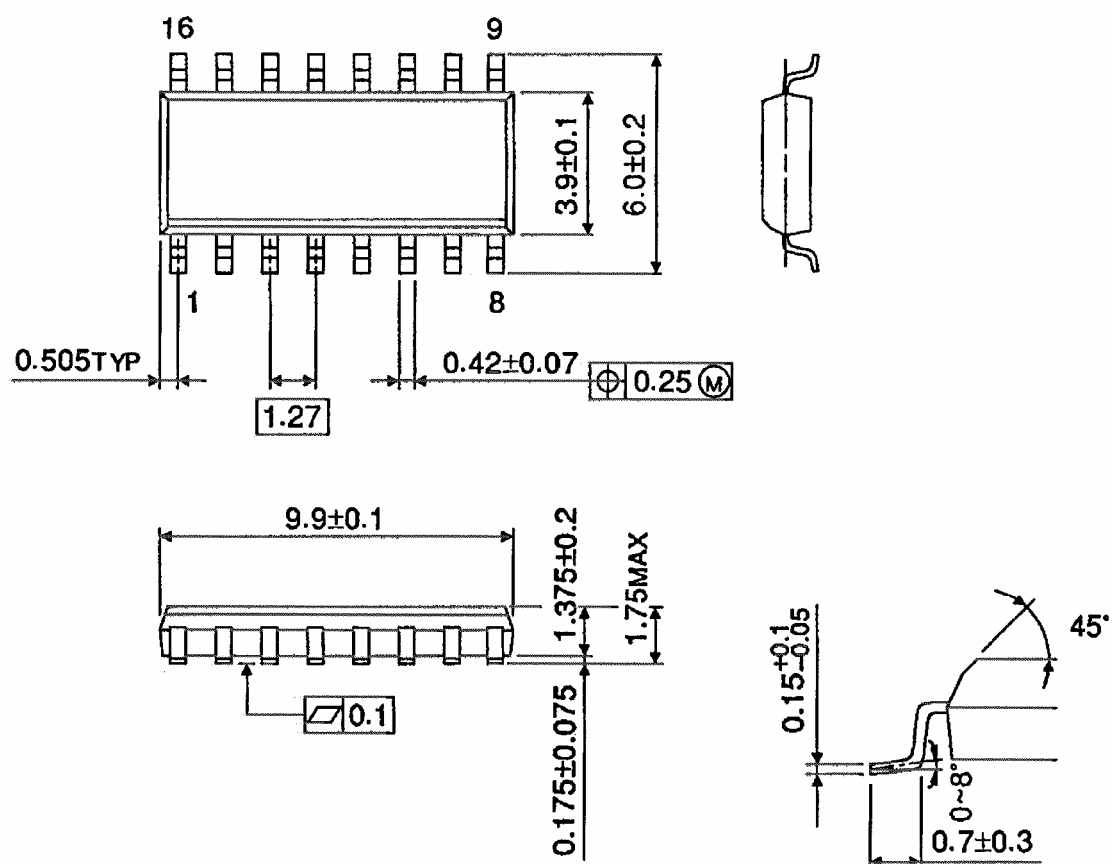


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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20070701-EN GENERAL

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