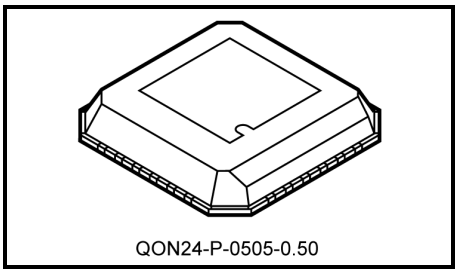
TOSHIBA Bipolar Linear IC Silicon Monolithic

TA2170FLG

Low Current Consumption Headphone Amplifier (Built-in Input Selector)

The TA2170FLG is a stereo headphone amplifier built-in selector switch for three inputs.

The mute switch is built into each of the three inputs, and a single or mixer output can be selected for the output.



QON24-P-0505-0.50

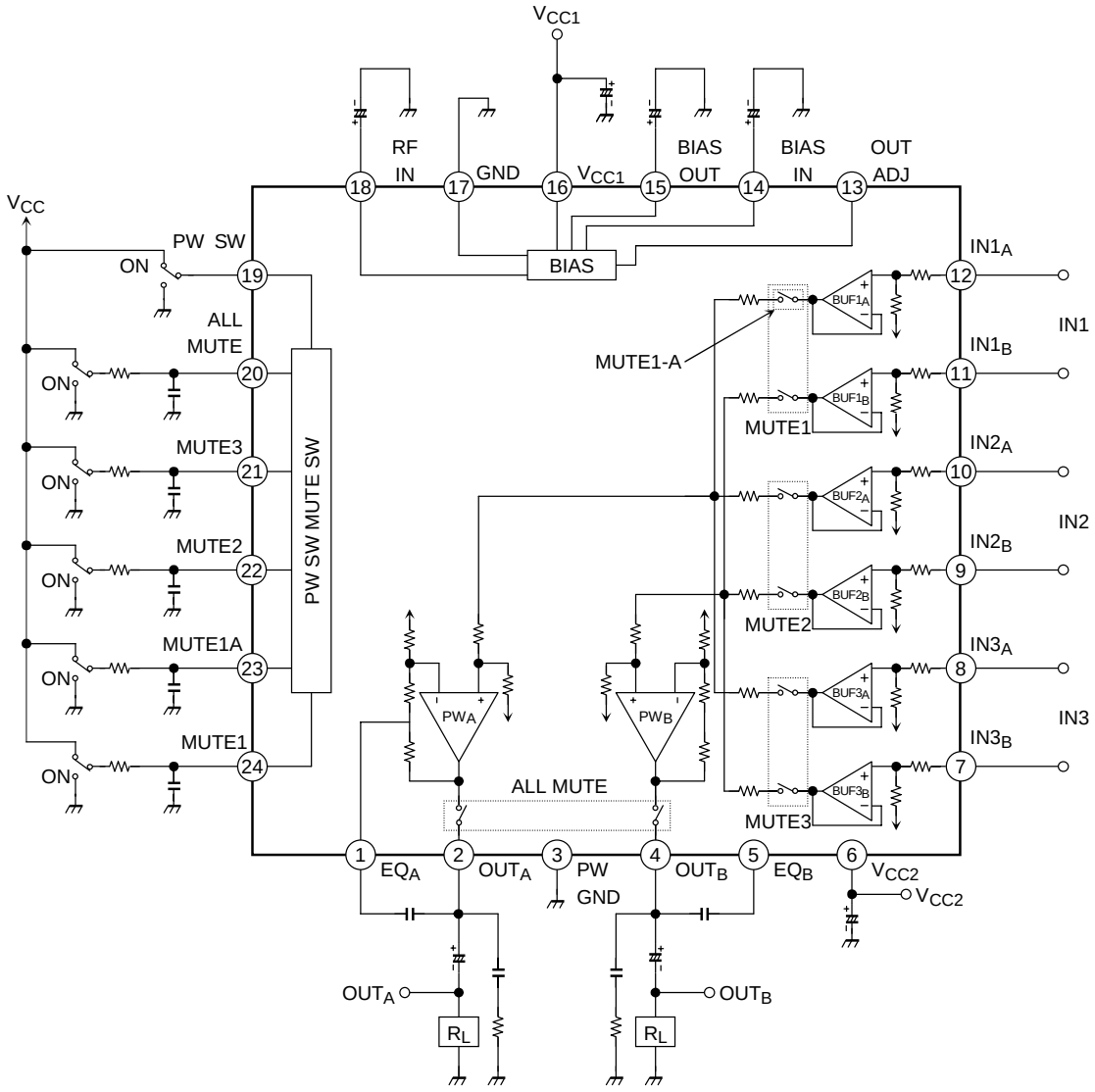
Weight: 0.05 g (typ.)

Marking: 2170G

Features

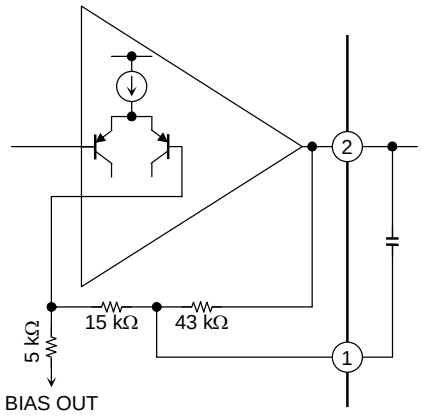
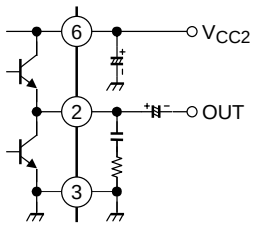
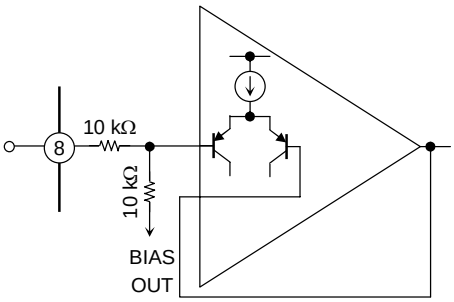
- Low current consumption
  V_{CC} = 3 V, f = 1 kHz, R_L = 32 Ω, typ.
  - No signal mode
    I_{CCQ} = 0.9 mA (1-input mode)
    I_{CCQ} = 1.0 mA (2-input mode)
    I_{CCQ} = 1.1 mA (3-input mode)
  - 0.1 mW × 2 ch
    I_{CC} = 2.2 mA (1-input mode)
    I_{CC} = 2.3 mA (2-input mode)
    I_{CC} = 2.4 mA (3-input mode)
  - 0.5 mW × 2 ch
    I_{CC} = 4.1 mA (1-input mode)
    I_{CC} = 4.2 mA (2-input mode)
    I_{CC} = 4.3 mA (3-input mode)
- G_V = −0.3 dB (1-input mode, typ.)
- Built-in signal level adjustment circuit to eliminate any perceptible change in volume whether single or mixer output is used.
- Built-in power switch
- Built-in all mute switch
- Built-in mute switch at each buffer amplifier
- Built-in one side mute switch at buffer amplifier 1
- Operating supply voltage range (Ta = 25°C): $V_{CC1\ (opr)}$ = 1.8 to 4.5 V
  $V_{CC2\ (opr)}$ = 0.9 to 4.5 V

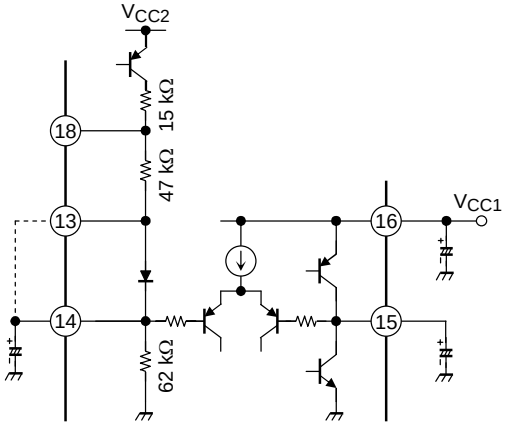
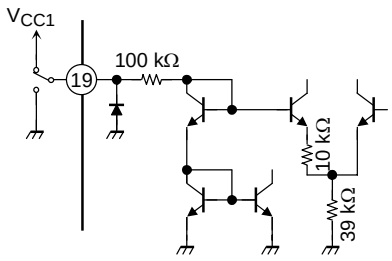
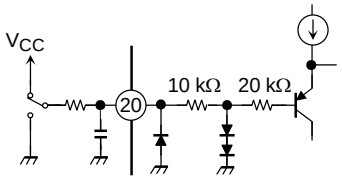
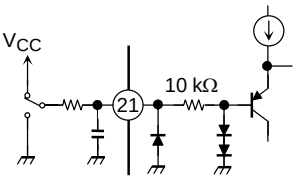
Block Diagram



Pin Descriptions

Pin Voltage: Typical pin voltage for a test circuit when no input signal is applied, $V_{CC1} = V_{CC2} = 3$ V, Ta = 25°C

Pin No. & Name		Function	Internal Circuit	Pin Voltage (V)
1	EQ_A	Low-pass compensation pins		1.15
5	EQ_B			
2	OUT_A	Outputs from power amplifier		1.15
4	OUT_B			
3	PW GND	GND for power drive stage		0
6	V_{CC2}	V_{CC} for power drive stage		3
7	$IN3_B$	Inputs to buffer amplifier 3		1.15
8	$IN3_A$			
9	$IN2_B$	Inputs to buffer amplifier 2		1.15
10	$IN2_A$			
11	$IN1_B$	Inputs to buffer amplifier 1		1.15
12	$IN1_A$			

Pin No. & Name		Function	Internal Circuit	Pin Voltage (V)
13	OUT ADJ	DC output voltage adjustment Either connect this pin or leave it open, depending on the level of V_{CC2}. If the power supply of a 1.5-V system is applied to V_{CC2}, connect this pin to BIAS IN (pin 14). If the power supply of a 3-V system is applied to V_{CC2}, leave this pin open.		1.85
14	BIAS IN	Bias circuit input		1.15
15	BIAS OUT	Bias circuit output		1.15
16	V_{CC1}	V_{CC} for everything other than the power drive stage		3
18	RF IN	Ripple filter input		2.7
17	GND	—	—	0
19	PW SW	Power switch (IC ON: H level IC OF : L level Refer to Application Note 4.		3
20	ALL MUTE	All mute switch (Mute ON: L level Mute OFF: H level Refer to Application Note 4.		—
21	MUTE3	Mute switch of buffer amplifier 3 (Mute ON: L level Mute OFF: H level Refer to Application Note 4.		—
22	MUTE2	Mute switch of buffer amplifier 2 (Mute ON: L level Mute OFF: H level Refer to Application Note 4.		—
23	MUTE1A	Mute switch of buffer amplifier 1A (Mute ON: L level Mute OFF: H level This switch is used for turning on A channel mutes for buffer amplifier 1. Refer to Application Note 4.		—
24	MUTE1	Mute switch of buffer amplifier 1 (Mute ON: L level Mute OFF: H level Refer to Application Note 4.		—

Application Notes

1. Mute switch and voltage gain

This IC is designed to ensure there is no perceptible change in volume whether a single output or several outputs are used.

When the input signal to the three buffer amplifiers is the same and in a linear domain, the relation between the mute switches and voltage gain is as follows:

Test condition: V_{CC} = 3 V, f = 1 kHz, V_{in} = −20 dBV, theoretical value.

(1) 1-input mode

MUTE SW				Attenuation to an input signal (dB)						Total gain (dB)	
				BUF1		BUF2		BUF3			
MUTE1	MUTE1A	MUTE2	MUTE3	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch
Input signal is applied to BUF 1.											
OFF	OFF	ON	ON	0	0	—	—	—	—	0	0
OFF	OFF	OFF	ON	−6	−6	—	—	—	—	−6	−6
OFF	OFF	ON	OFF	−6	−6	—	—	—	—	−6	−6
OFF	OFF	OFF	OFF	−9.5	−9.5	—	—	—	—	−9.5	−9.5
OFF	ON	ON	ON	—	0	—	—	—	—	—	0
OFF	ON	OFF	ON	—	−6	—	—	—	—	—	−6
OFF	ON	ON	OFF	—	−6	—	—	—	—	—	−6
OFF	ON	OFF	OFF	—	−9.5	—	—	—	—	—	−9.5
Input signal is applied to BUF 2											
ON	ON/OFF	OFF	ON	—	—	0	0	—	—	0	0
ON	ON/OFF	OFF	OFF	—	—	−6	−6	—	—	−6	−6
OFF	OFF	OFF	ON	—	—	−6	−6	—	—	−6	−6
OFF	ON	OFF	ON	—	—	0	−6	—	—	0	−6
OFF	OFF	OFF	OFF	—	—	−9.5	−9.5	—	—	−9.5	−9.5
OFF	ON	OFF	OFF	—	—	−6	−9.5	—	—	−6	−9.5
Input signal is applied to BUF 3.											
ON	ON/OFF	ON	OFF	—	—	—	—	0	0	0	0
ON	ON/OFF	OFF	OFF	—	—	—	—	−6	−6	−6	−6
OFF	OFF	ON	OFF	—	—	—	—	−6	−6	−6	−6
OFF	ON	ON	OFF	—	—	—	—	0	−6	0	−6
OFF	OFF	OFF	OFF	—	—	—	—	−9.5	−9.5	−9.5	−9.5
OFF	ON	OFF	OFF	—	—	—	—	−6	−9.5	−6	−9.5

(2) 2-input mode

MUTE SW				Attenuation to an input signal (dB)						Total gain (dB)	
				BUF1		BUF2		BUF3			
MUTE1	MUTE1A	MUTE2	MUTE3	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch
Input signal is applied to BUF 1 and BUF 2.											
OFF	OFF	OFF	ON	−6	−6	−6	−6	—	—	0	0
OFF	OFF	OFF	OFF	−9.5	−9.5	−9.5	−9.5	—	—	−3.5	−3.5
OFF	ON	OFF	ON	—	—	—	—	—	—	—	—
OFF	ON	OFF	OFF	—	−6	−9.5	−6	—	—	−3.5	0
Input signal is applied to BUF 1 and BUF 3.											
OFF	OFF	ON	OFF	−6	−6	—	—	−6	−6	0	0
OFF	OFF	OFF	OFF	−9.5	−9.5	—	—	−9.5	−9.5	−3.5	−3.5
OFF	ON	ON	OFF	—	−6	—	—	−6	−6	−6	0
OFF	ON	OFF	OFF	—	−9.5	—	—	−9.5	−9.5	−9.5	−3.5
Input signal is applied to BUF 2 and BUF 3.											
ON	ON/OFF	OFF	OFF	—	—	−6	−6	−6	−6	0	0
OFF	ON	OFF	OFF	—	—	−6	−9.5	−6	−9.5	0	−3.5
OFF	OFF	OFF	OFF	—	—	−9.5	−9.5	−9.5	−9.5	−3.5	−3.5

(3) 3-input mode

MUTE SW				Attenuation to an input signal (dB)						Total gain (dB)	
				BUF1		BUF2		BUF3			
MUTE1	MUTE1A	MUTE2	MUTE3	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch
OFF	OFF	OFF	OFF	−9.5	−9.5	−9.5	−9.5	−9.5	−9.5	0	0
OFF	ON	OFF	OFF	—	−9.5	−9.5	−9.5	−9.5	−9.5	−3.5	0

2. Low-cut compensation

The low-frequency range can be decreased using an output-coupling capacitor and a load (f_c = 50 Hz at C = 100 μF, R = 32 Ω). However, since the capacitor is connected between the IC's output pin (pin 2/4) and EQ pin (pin 1/5), the low-frequency gain of the power amplifier increases, enabling low-cut compensation to be performed. For the response of capacitors of different values, refer to Figure 1.

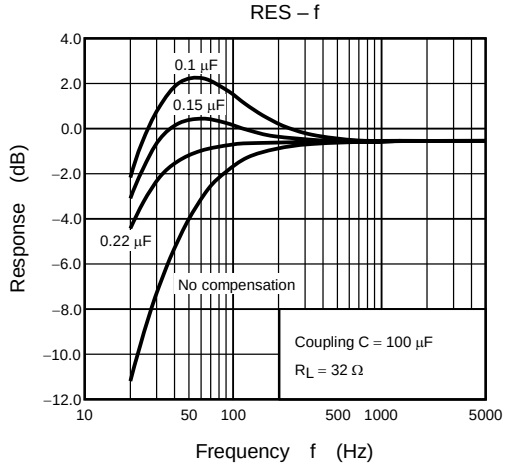


Figure 1. Capacitor Response

3. Adjustment of DC output voltage

Perform the following with the OUT ADJ pin (pin 13) using the power supply of V_{CC1} and V_{CC2}:

- If a boost voltage is applied to V_{CC1}, V_{CC2} is connected to a battery and the difference between V_{CC1} and V_{CC2} is greater than or equal to 0.7 V, short pins 13 and 14 together. In this case the DC output voltage will be as follows:

  $$\frac{V_{CC2}}{2}.$$

- If the difference between V_{CC1} and V_{CC2} is less than 0.7 V, or if V_{CC1} and V_{CC2} are connected to the same power supply, leave pin 13 open.

  In these cases, the DC output voltage will be $\frac{V_{CC2} - 0.7\,V}{2}$.

4. Switch

(1) Timing chart
Refer to Figure 2 for the IC timing chart.

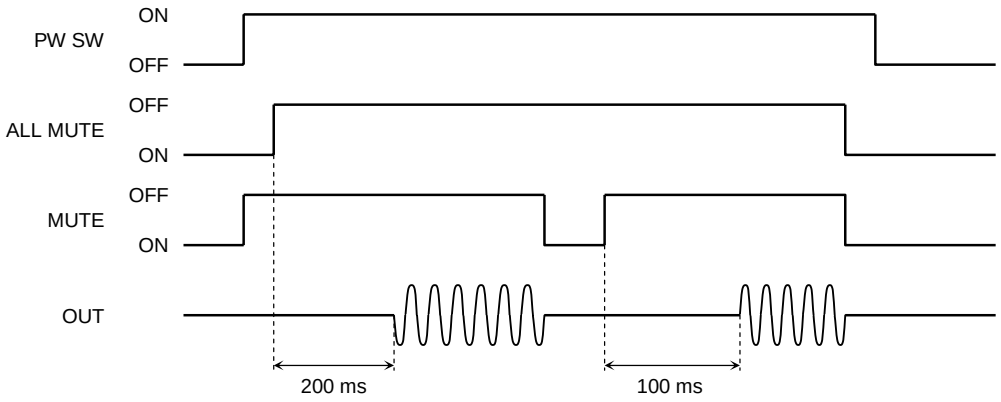
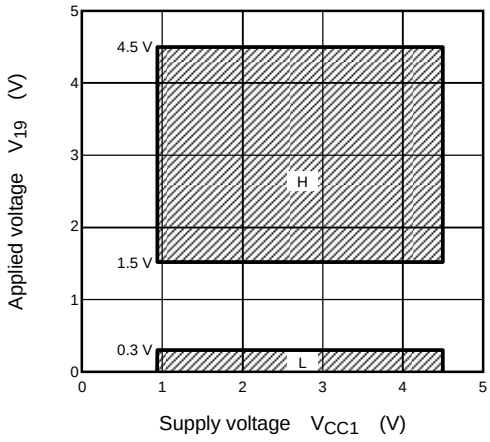


Figure 2. Timing Chart

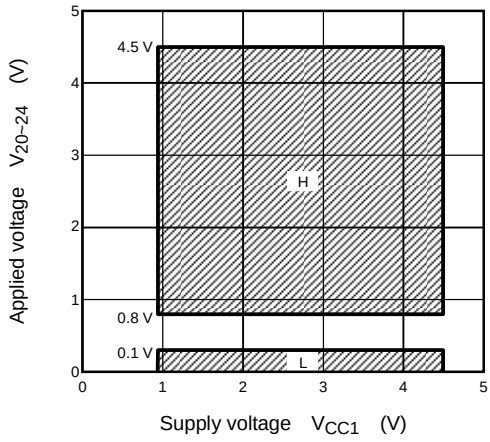
(2) PW SW
The device is ON when this pin is set to High. To prevent the IC being turned ON by external noise, it is necessary to connect an external pull-down resistor to the PW SW pin. The pin is highly sensitive.

(3) Mute smoothing
Ensure that the smoothing resistor used for the mute pin is 100 kΩ or less. The switch circuit will not operate normally if the value is greater than this.

(4) Switch sensitivity (Ta = 25°C)



	PW SW
H level	IC ON
L level	IC OFF



	MUTE
H level	Mute OFF
L level	Mute ON

Figure 3: Switch Sensitivity

5. Capacitor

The following capacitors must have excellent temperature and frequency characteristics.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage 1	V_{CC1}	4.5	V
Supply voltage 2	V_{CC2}	4.5	
Output current	$I_{o\ (peak)}$	100	mA
Power dissipation	P_D (Note)	350	mW
Operating temperature	T_{opr}	−25~75	°C
Storage temperature	T_{stg}	−55~150	°C

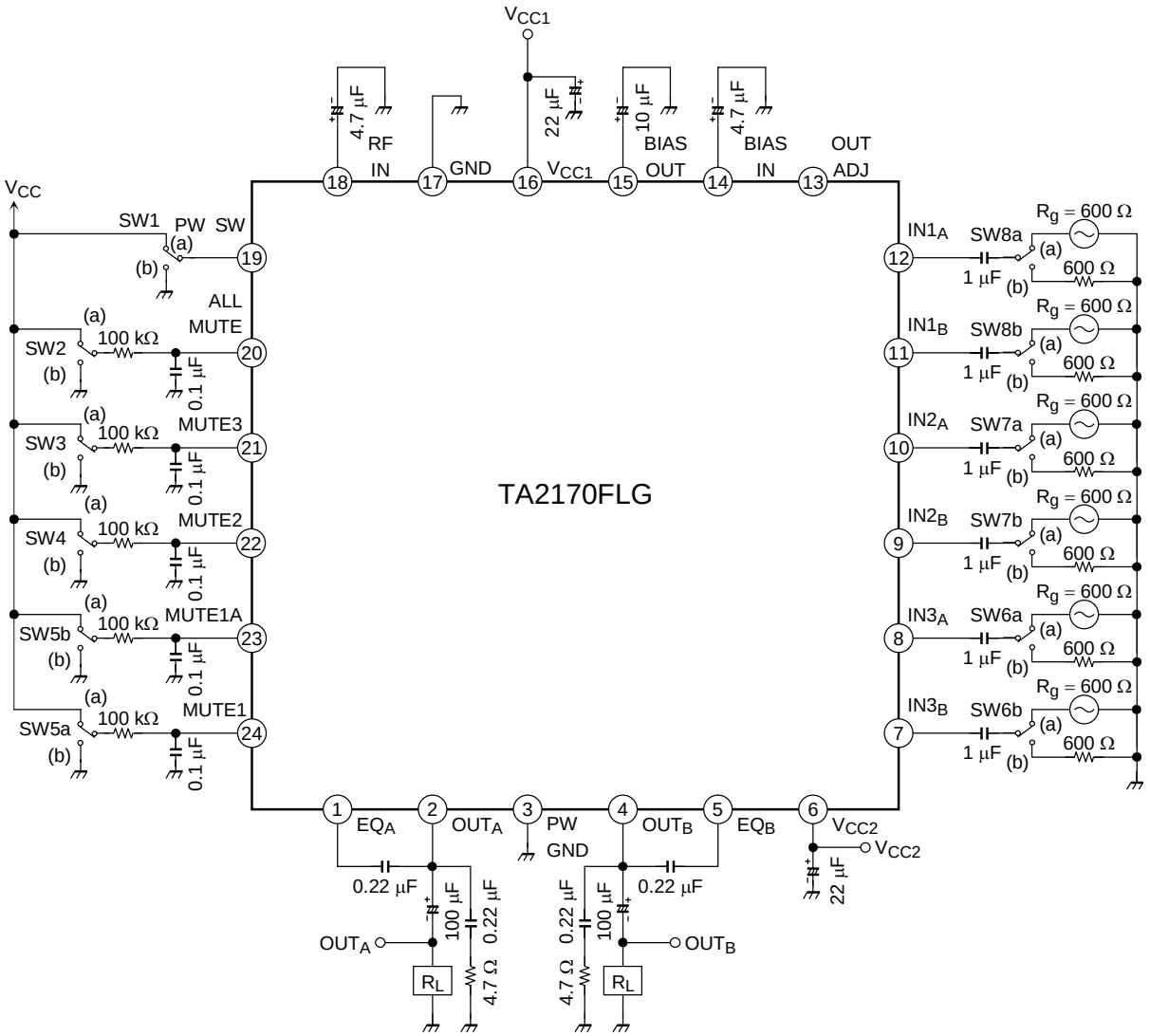
Note: Derated by 2.8 mW/°C above Ta = 25°C

Electrical Characteristics

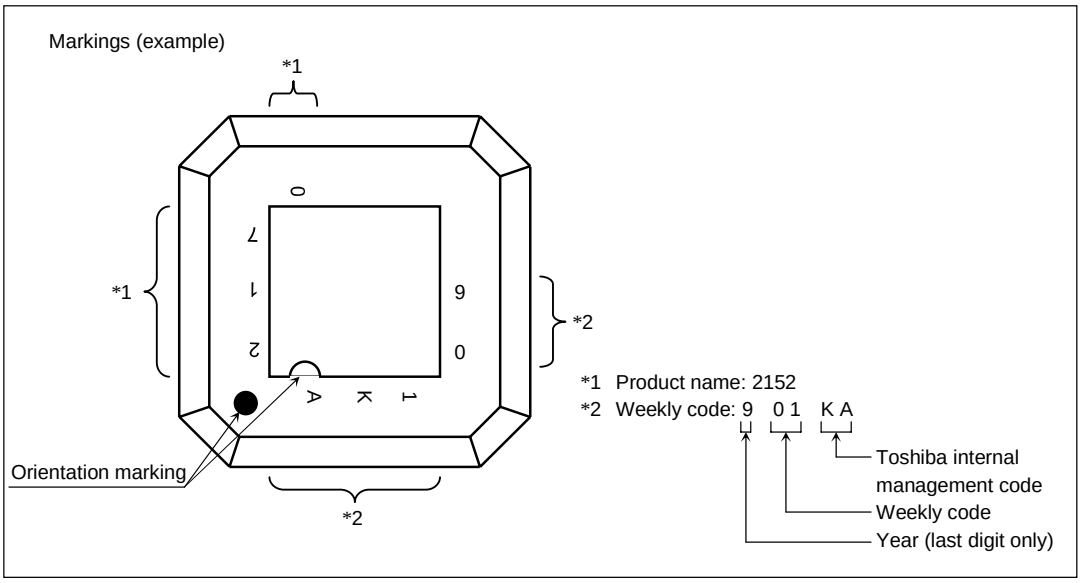
(Unless otherwise specified, $V_{CC1} = V_{CC2} = 3$ V, Rg = 600 Ω, $R_L = 32$ Ω, f = 1 kHz, Ta = 25°C, SW1~SW5: a, SW6~SW8: a)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Quiescent supply current	I_{CCQ1}	IC OFF mode SW1~5: b	—	—	5	μA
	I_{CCQ2}	1 input on mode BUF1: ON (SW5: a, SW3/4: b) BUF2: ON (SW4: a, SW3/5: b) BUF3: ON (SW3: a, SW4/5: b)	—	0.9	1.6	mA
	I_{CCQ3}	2 input on mode BUF1/2: ON (SW4/5: a, SW3: b) BUF1/3: ON (SW3/5: a, SW4: b) BUF2/3: ON (SW3/4: a, SW5: b)	—	1.0	1.8	
	I_{CCQ4}	3 input on mode	—	1.1	2.0	
	I_{CCQ5}	1 input on mode V_{CC1} = 2.4 V, V_{CC2} = 1.2 V BUF1: ON (SW5: a, SW3/4: b) BUF2: ON (SW4: a, SW3/5: b) BUF3: ON (SW3: a, SW4/5: b)	—	0.9	1.6	
Power supply current during drive	I_{CC1}	1 input on mode 0.1 mW/32 Ω × 2 ch BUF1: ON (SW5: a, SW3/4: b) BUF2: ON (SW4: a, SW3/5: b) BUF3: ON (SW3: a, SW4/5: b)	—	2.2	—	mA
	I_{CC2}	2 input on mode 0.1 mW/32 Ω × 2 ch BUF1/2: ON (SW4/5: a, SW3: b) BUF1/3: ON (SW3/5: a, SW4: b) BUF2/3: ON (SW3/4: a, SW5: b)	—	2.3	—	
	I_{CC3}	3 input on mode 0.1 mW/32 Ω × 2 ch	—	2.4	—	
Voltage gain	G_{V1}	1 input on mode V_o = −20 dBV BUF1: ON (SW5: a, SW3/4: b) BUF2: ON (SW4: a, SW3/5: b) BUF3: ON (SW3: a, SW4/5: b)	−1.8	−0.3	1.2	dB
	G_{V2}	2 input on mode V_o = −20 dBV BUF1/2: ON (SW4/5: a, SW3: b) BUF1/3: ON (SW3/5: a, SW4: b) BUF2/3: ON (SW3/4: a, SW5: b)	−1.0	0.5	2.0	
	G_{V3}	3 input on mode V_o = −20 dBV	−0.8	0.7	2.2	
Channel balance	CB	V_o = −20 dBV	−1.5	0	1.5	dB
Output power	P_{o1}	THD = 10%	15	20	—	mW
	P_{o2}	V_{CC1} = 2.4 V, V_{CC2} = 1.2 V THD = 10%	3	6	—	
Total harmonic distortion	THD	P_o = 1 mW	—	0.1	0.3	%
Output noise voltage	V_{no}	R_g = 600 Ω, Filter: IHF-A, SW6~8: b	—	−100	−96	dBV
Cross talk	CT	V_o = −20 dBV	−53	−60	—	dB
Ripple rejection ratio	RR	f_r = 100 Hz, V_r = −20 dBV	−70	−80	—	dB
Muting attenuation	ATT1	ALL MUTE SW: ON, V_o = −20 dBV	−75	−90	—	dB
	ATT2	MUTE SW: ON, V_o = −20 dBV	−47	−62	—	
PW SW ON current	I19	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	5	—	—	μA
PW SW OFF voltage	V19	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	0	—	0.3	V
MUTE SW OFF current	$I_{20\text{-}24}$	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	5	—	—	μA
MUTE SW ON voltage	$V_{20\text{-}24}$	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	0	—	0.1	V

Test Circuit

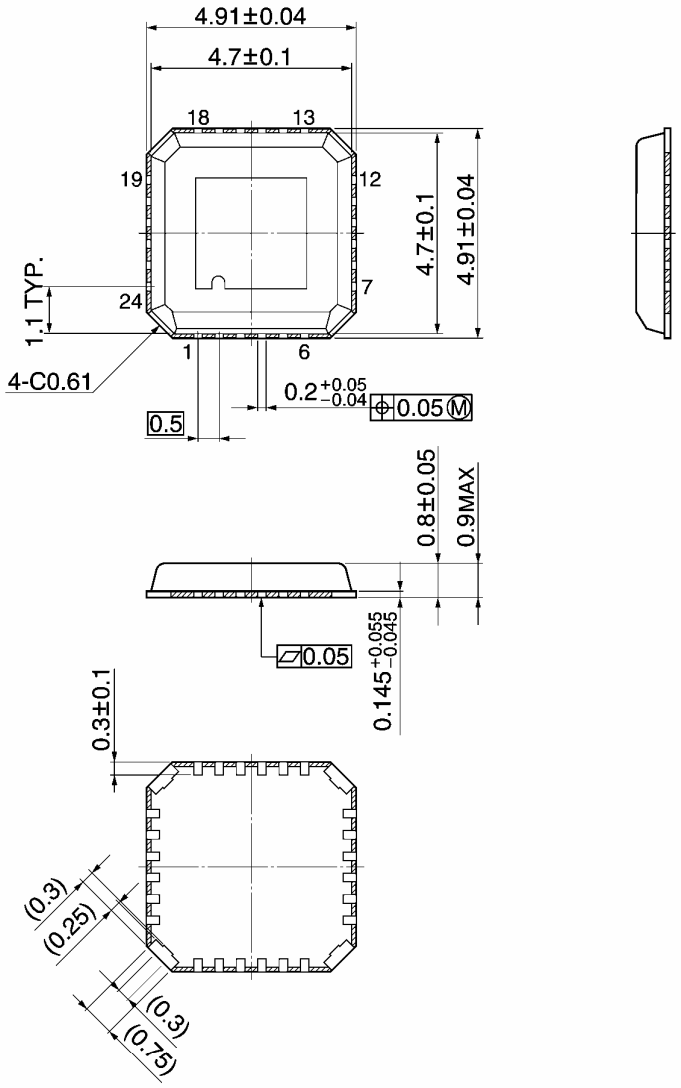


Markings


Markings (example)
*1
*1
*2
*2
0
7
1
2
9
0
A K 1
Orientation marking
*1 Product name: 2152
*2 Weekly code: 9 0 1 K A
Toshiba internal management code
Weekly code
Year (last digit only)

Package Dimensions

QON24-P-0505-0.50 Unit: mm



Note 1) The solder plating portion in four corners of tne package shall not be treated as an external terminal.

Note 2) Don`t carry out soldering to four corners of the package.

Note 3) area : Resin surface

Weight: 0.05 g (typ.)

RESTRICTIONS ON PRODUCT USE

060116EBA

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About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux