

20A, 55V, 0.036 Ohm, N-Channel UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75321.

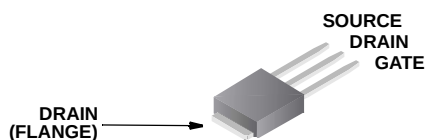
Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75321D3	TO-251AA	75321D
HUF75321D3S	TO-252AA	75321D

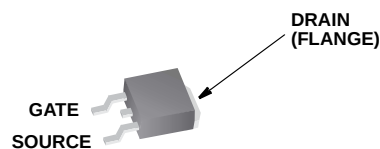
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-251AA variant in tape and reel, e.g., HUF75321D3ST.

Packaging

JEDEC TO-251AA



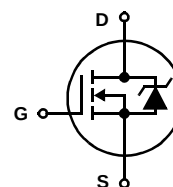
JEDEC TO-252AA



Features

- 20A, 55V
- Simulation Models
 - Temperature Compensating PSPICE® and SABER™ Models
 - Thermal Impedance SPICE and SABER Models Available on the web at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF75321D3, HUF75321D3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DS}	55 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55 V
Gate to Source Voltage	V_{GS}	± 20 V
Drain Current		
Continuous (Figure 2)	I_D	20 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15
Power Dissipation	P_D	93 W
Derate Above 25°C		0.625 $\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 45V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 20A, V _{GS} = 10V (Figure 9)	-	0.030	0.036	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	1.6	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-251, TO-252	-	-	100	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≅ 20A, R _L = 1.5Ω, V _{GS} = 10V, R _{GS} = 25Ω	-	-	100	ns	
Turn-On Delay Time	t _{d(ON)}		-	11	-	ns	
Rise Time	t _r		-	55	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	47	-	ns	
Fall Time	t _f		-	66	-	ns	
Turn-Off Time	t _{OFF}		-	-	170	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 30V, I _D ≅ 20A, R _L = 1.5Ω I _{g(REF)} = 1.0mA (Figure 13)	-	36	44	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	21	26	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	1.3	1.6	nC
Gate to Source Gate Charge	Q _{gs}			-	3	-	nC
Reverse Transfer Capacitance	Q _{gd}			-	9	-	nC

HUF75321D3, HUF75321D3S

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	680	-	pF
Output Capacitance	C_{OSS}		-	270	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	60	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 20\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	59	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	82	nC

Typical Performance Curves

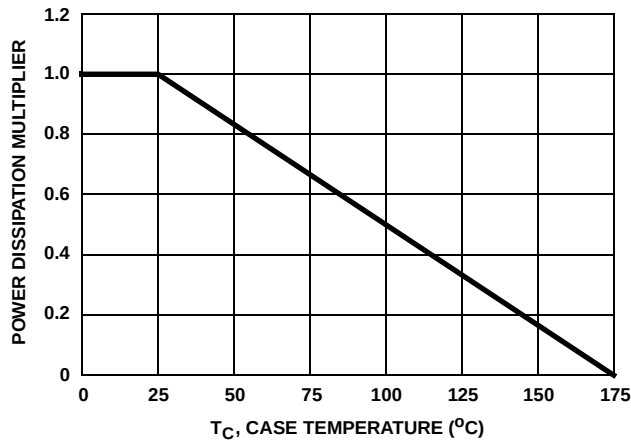


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

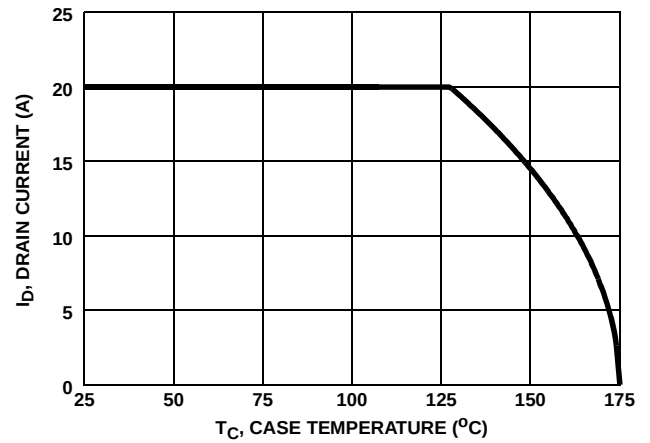


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

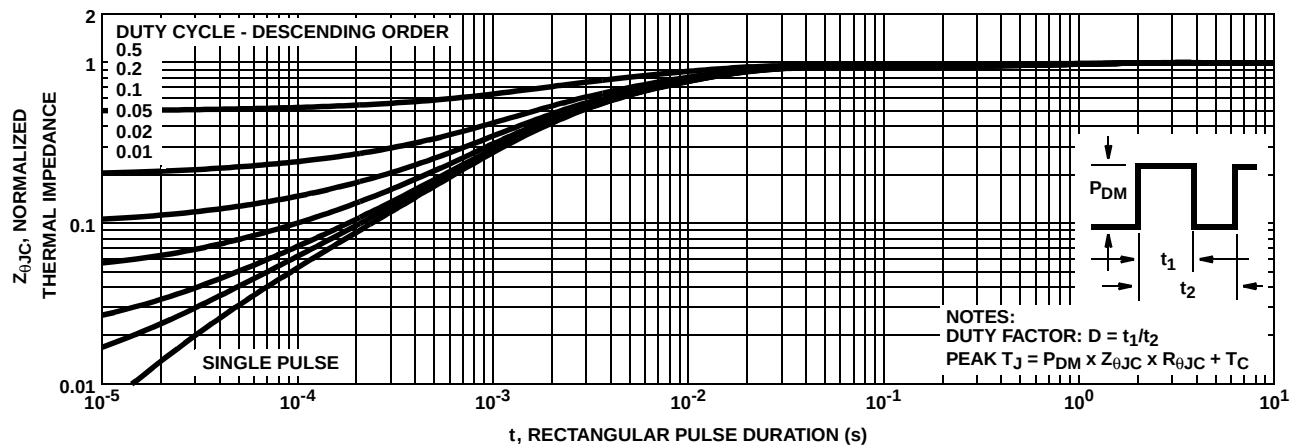


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

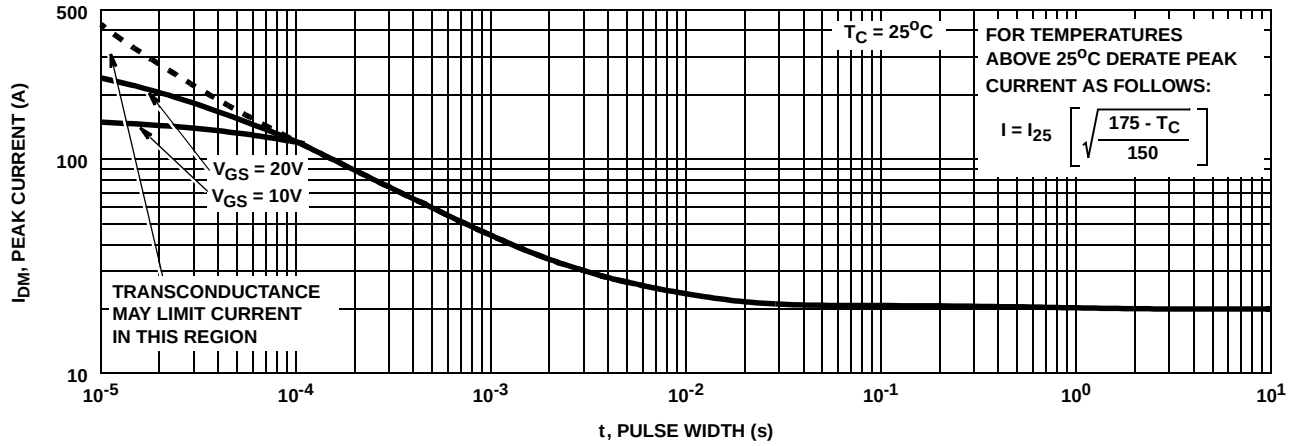


FIGURE 4. PEAK CURRENT CAPABILITY

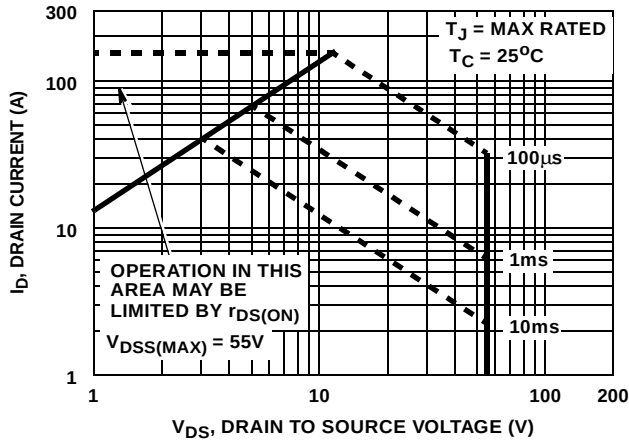


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

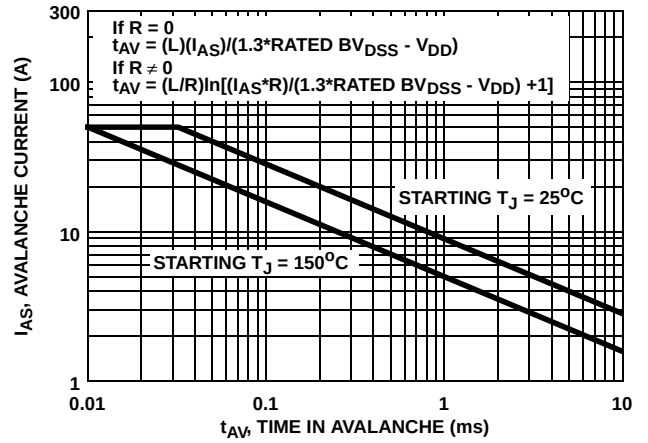


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

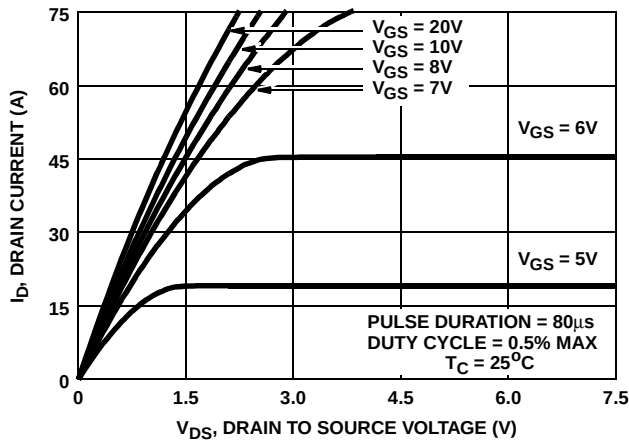


FIGURE 7. SATURATION CHARACTERISTICS

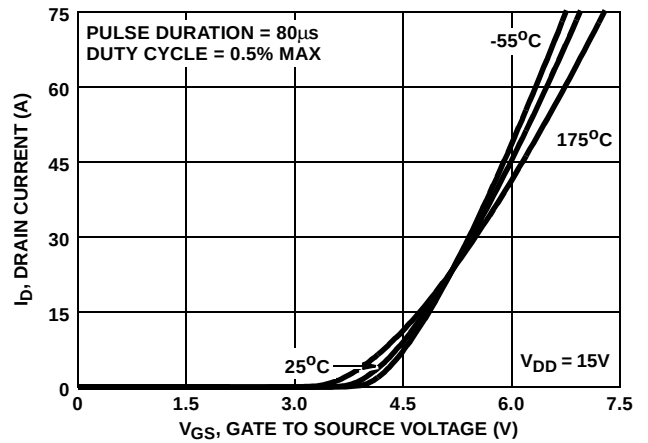


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

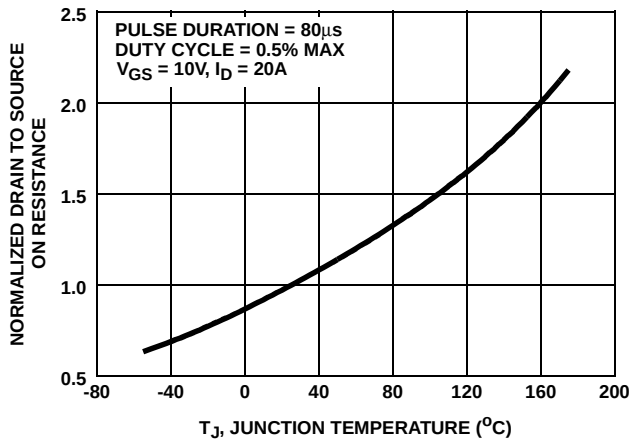


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

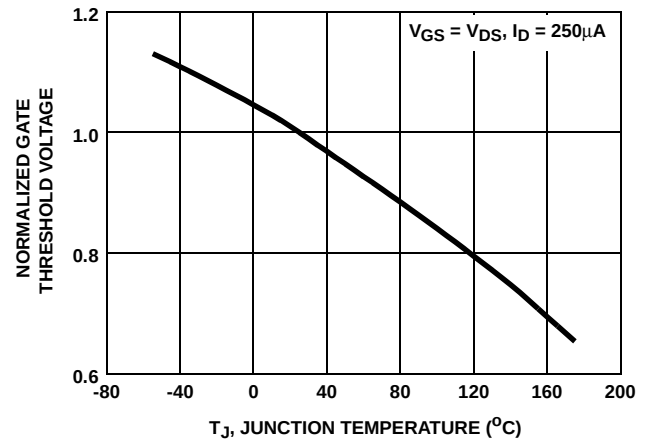


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

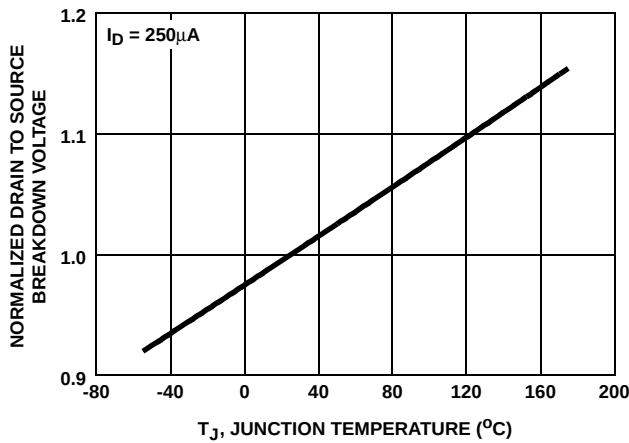


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

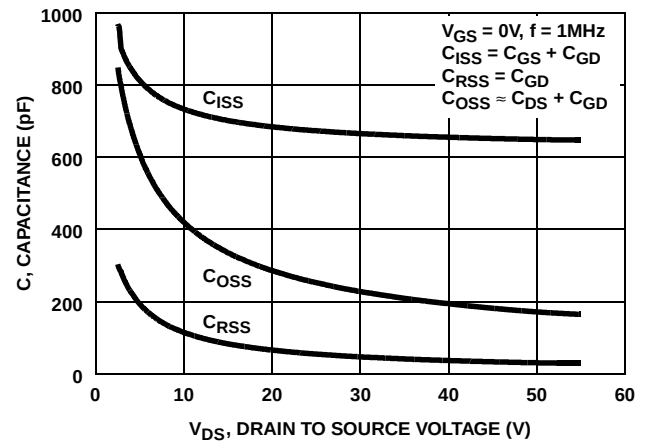
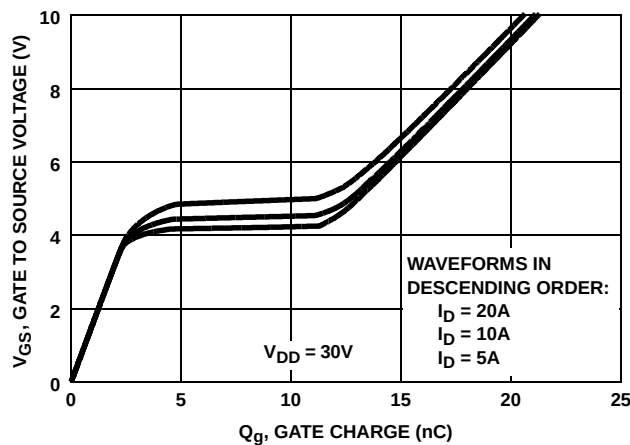


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

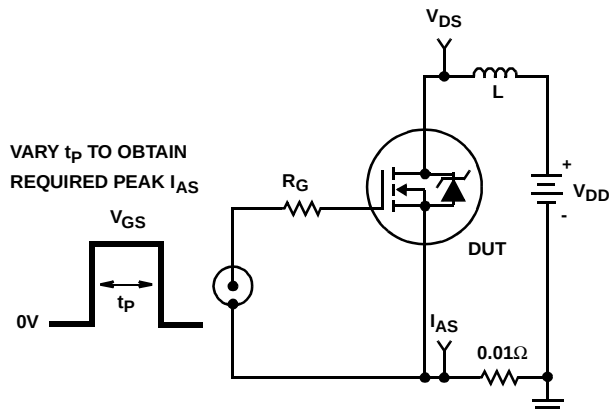


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

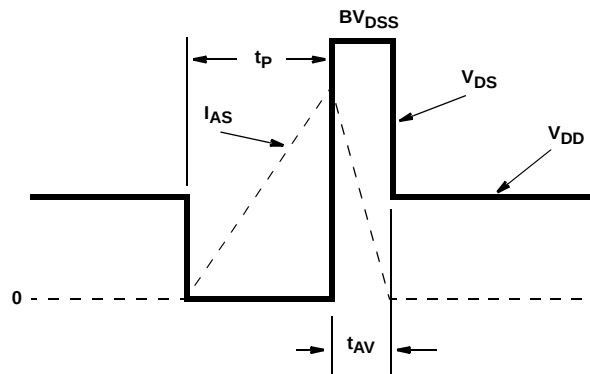


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

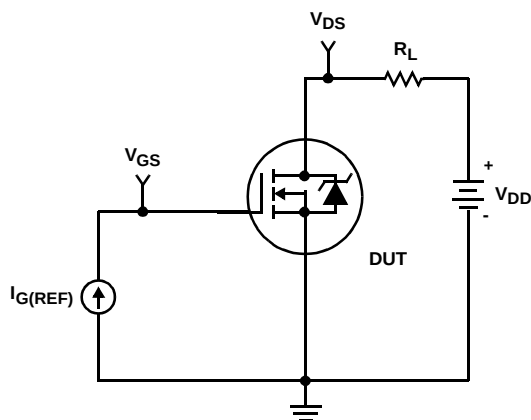


FIGURE 16. GATE CHARGE TEST CIRCUIT

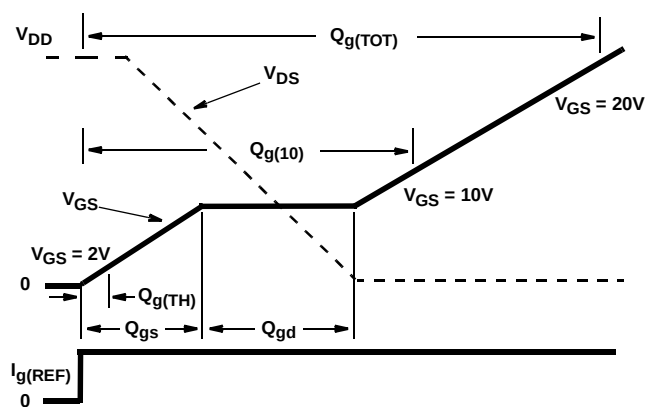


FIGURE 17. GATE CHARGE WAVEFORM

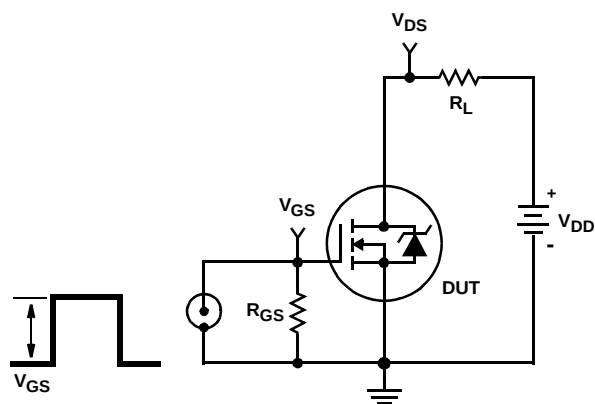


FIGURE 18. SWITCHING TIME TEST CIRCUIT

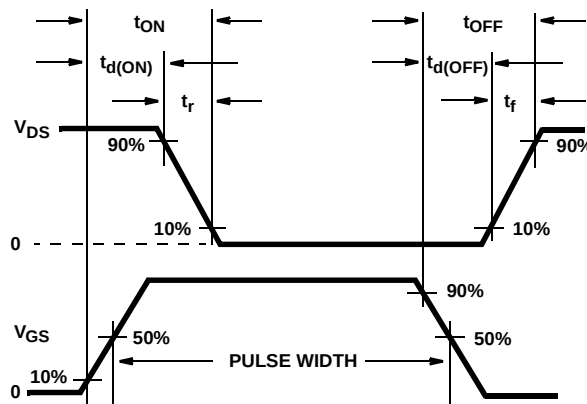


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

.SUBCKT HUF75321D 2 1 3 ; rev 4/29/98

CA 12 8 9.96e-10
CB 15 14 9.83e-10
CIN 6 8 6.18e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 59.54
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.57e-9
LSOURCE 3 7 4.25e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 5.50e-3
RGATE 9 20 2.25
RLDRAIN 2 5 10
RLGATE 1 9 35.7
RLSOURCE 3 7 42.5
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 16.30e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

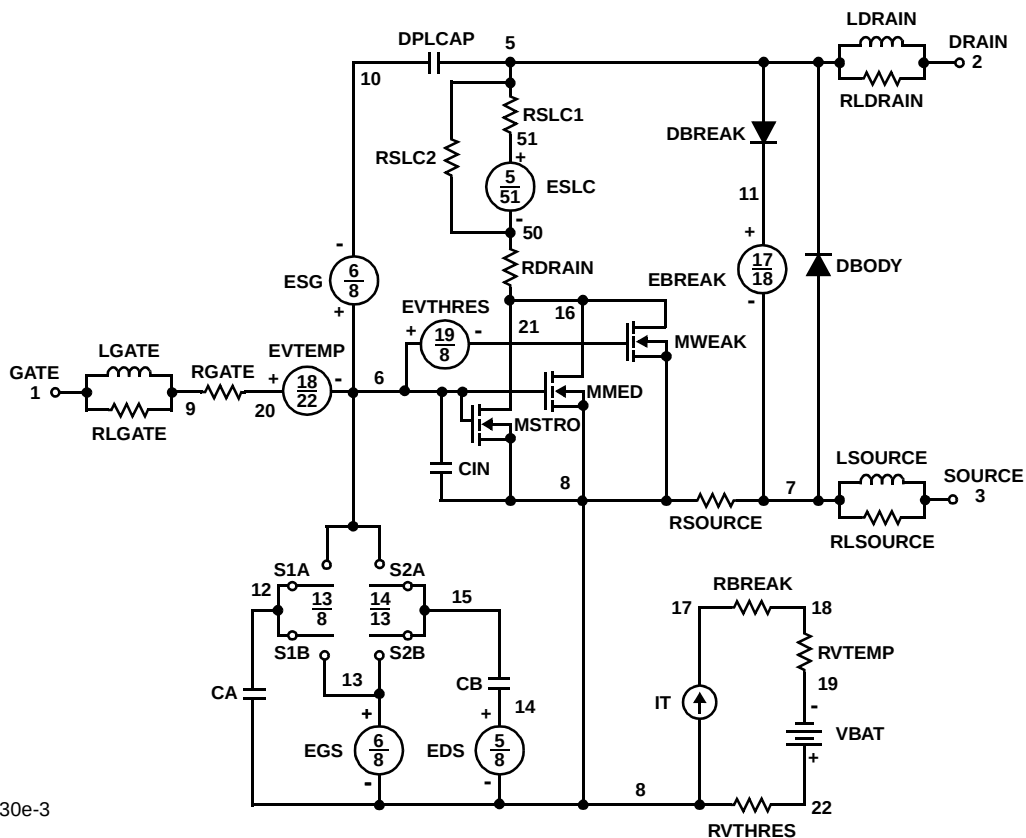
ESLC 51 50 VALUE=((V(5,51)/ABS(V(5,51))))*(PWR(V(5,51)/(1e-6*101),2.5))

.MODEL DBODYMOD D (IS = 7.47e-13 RS = 6.45e-3 TRS1 = 2.01e-3 TRS2 = 1.21e-6 CJO = 1.02e-9 TT = 3.21e-8 M = 0.50)
.MODEL DBREAKMOD D (RS = 2.01e-1 TRS1 = 3.62e-3 TRS2 = 6.01e-7)
.MODEL DPLCAPMOD D (CJO = 9.0e-10 IS = 1e-30 ON = 10 M = 0.85)
.MODEL MMEDMOD NMOS (VTO = 3.25 KP = 1.75 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.25)
.MODEL MSTROMOD NMOS (VTO = 3.65 KP = 32.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.91 KP = 0.07 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 22.5 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = 1.21e-7)
.MODEL RDRAINMOD RES (TC1 = 2.40e-2 TC2 = 1.02e-6)
.MODEL RSLCMOD RES (TC1 = 2.07e-4 TC2 = 4.67e-5)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -3.01e-3 TC2 = -8.85e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.96e-3 TC2 = 1.39e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.85 VOFF = -4.85)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.85 VOFF = -7.85)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF = 3.00)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.00 VOFF = 0.00)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 24 February 1999

HUF75321D

CTHERM1 th 6 2.7e-3
 CHERM2 6 5 3.7e-3
 CHERM3 5 4 1.2e-2
 CHERM4 4 3 3.8e-3
 CHERM5 3 2 1.4e-2
 CHERM6 2 tl 10.55

RHERM1 th 6 1.10e-2
 RHERM2 6 5 2.72e-2
 RHERM3 5 4 7.67e-2
 RHERM4 4 3 4.30e-1
 RHERM5 3 2 6.49e-1
 RHERM6 2 tl 8.61e-2

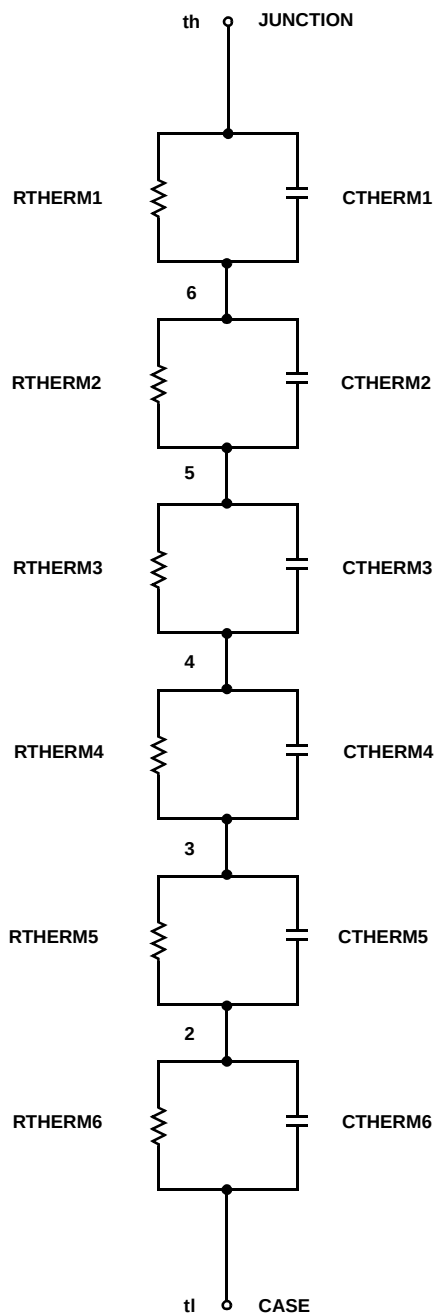
SABER Thermal Model

SABER thermal model HUF75321D

template thermal_model th tl
 thermal_c th, tl

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{
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    ctherm.therm2 6 5 = 3.7e-3
    ctherm.therm3 5 4 = 1.2e-2
    ctherm.therm4 4 3 = 3.8e-3
    ctherm.therm5 3 2 = 1.4e-2
    ctherm.therm6 2 tl = 10.55
```

```
rtherm.rtherm1 th 6 = 1.10e-3
rtherm.rtherm2 6 5 = 2.72e-2
rtherm.rtherm3 5 4 = 7.67e-2
rtherm.rtherm4 4 3 = 4.30e-1
rtherm.rtherm5 3 2 = 6.49e-1
rtherm.rtherm6 2 tl = 8.61e-2
}
```



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CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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