



STGD6NC60H

N-channel 600V - 7A - DPAK
Very fast PowerMESH™ IGBT

General features

Type	V _{CES}	V _{CE(sat)} Max @25°C	I _C @100°C
STGD6NC60H	600V	<2.5V	7A

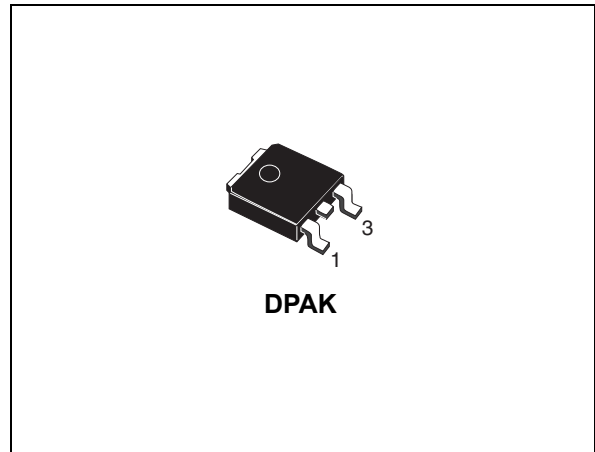
- Low on voltage drop (V_{cesat})
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- High frequency operation

Description

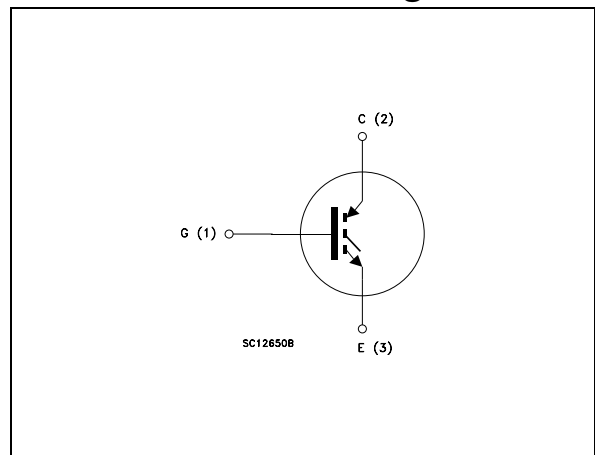
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “H” identifies a family optimized for high frequency application in order to achieve very high switching performances (reduced t_{fall}) maintaining a low voltage drop.

Applications

- High frequency inverters
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STGD6NC60HT4	GD6NC60H	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	15	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	7	A
$I_{CM}^{(2)}$	Collector current (pulsed)	21	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	56	W
T_{stg}	Storage temperature	– 55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		
T_l	Maximum lead temperature for soldering purpose (for 10sec. 1.6 mm from case)	300	$^\circ\text{C}$

1. Calculated according to the iterative formula::

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 3\text{A}$ $V_{GE} = 15\text{V}$, $I_C = 3\text{A}$, $T_C = 125^{\circ}\text{C}$		1.9 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\text{ }\mu\text{A}$	3.75		5.75	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}$, $T_C = 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			10 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 3\text{A}$		3		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		205 32 5.5		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	$V_{CE} = 390\text{V}$, $I_C = 3\text{A}$, $V_{GE} = 15\text{V}$, (see Figure 16)		13.6 3.4 5.1		nC nC nC
I_{CL}	Turn-off SOA minimum current	$V_{clamp} = 390\text{V}$, $T_J = 150^{\circ}\text{C}$, $R_G = 10\Omega$, $V_{GE} = 15\text{V}$		19		A

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 3A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_J = 25^\circ C$ (see Figure 17)		12 5 612		ns ns A/ μs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V$, $I_C = 3A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_J = 125^\circ C$ (see Figure 17)		13 4.3 560		ns ns A/ μs
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 3A$, $R_{GE} = 10\Omega$, $V_{GE} = 15V$, $T_J = 25^\circ C$ (see Figure 17)		40 76 100		ns ns ns
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V$, $I_C = 3A$, $R_{GE} = 10\Omega$, $V_{GE} = 15V$, $T_J = 125^\circ C$ (see Figure 17)		60 98 124		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V$, $I_C = 3A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_J = 25^\circ C$ (see Figure 17)		20 68 88		μJ μJ μJ
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V$, $I_C = 3A$ $R_G = 10\Omega$, $V_{GE} = 15V$, $T_J = 125^\circ C$ (see Figure 17)		37 93 130		μJ μJ μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in Figure 17. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature ($25^\circ C$ and $125^\circ C$)
2. Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

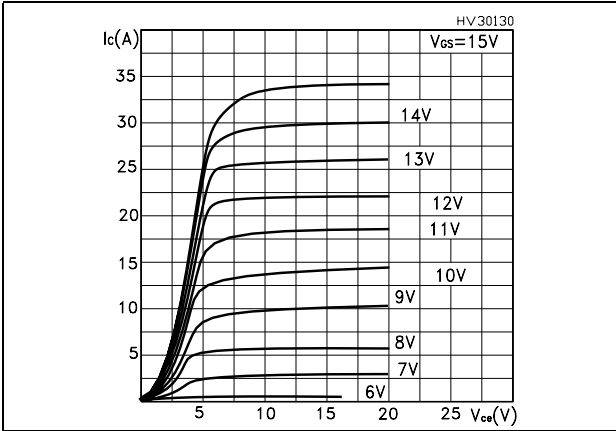


Figure 2. Transfer characteristics

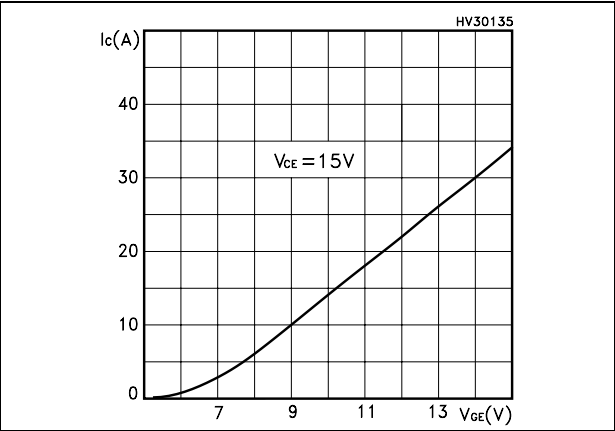


Figure 3. Transconductance

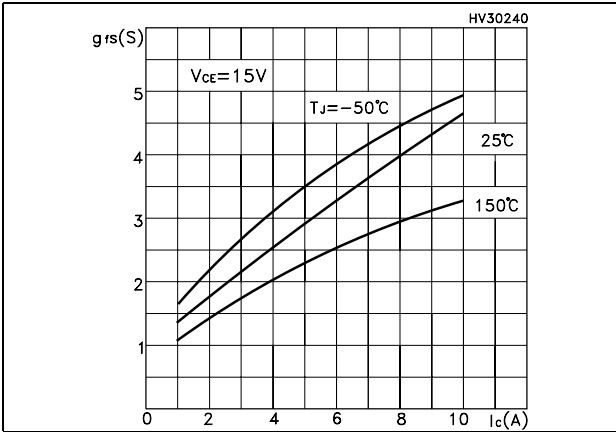


Figure 4. Collector-emitter on voltage vs temperature

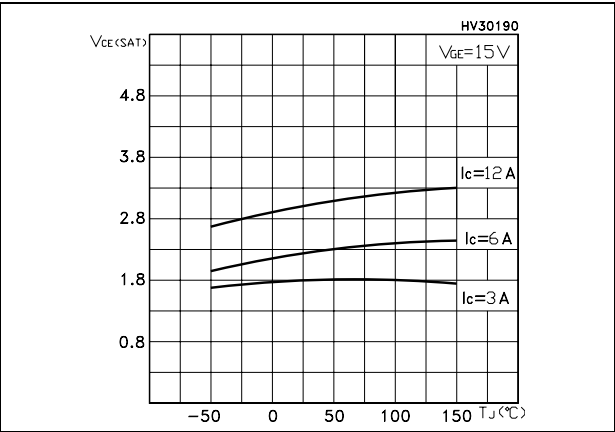


Figure 5. Gate charge vs gate-source voltage

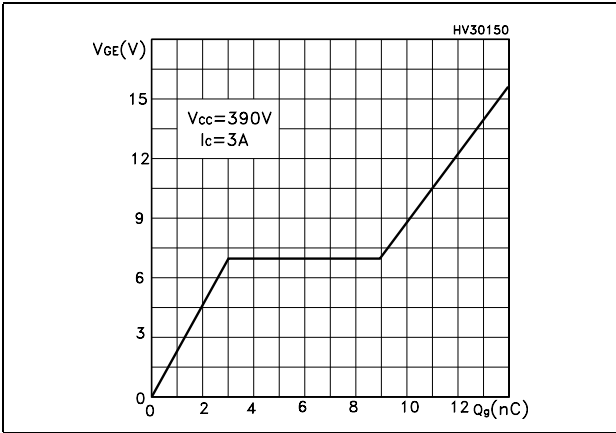


Figure 6. Capacitance variations

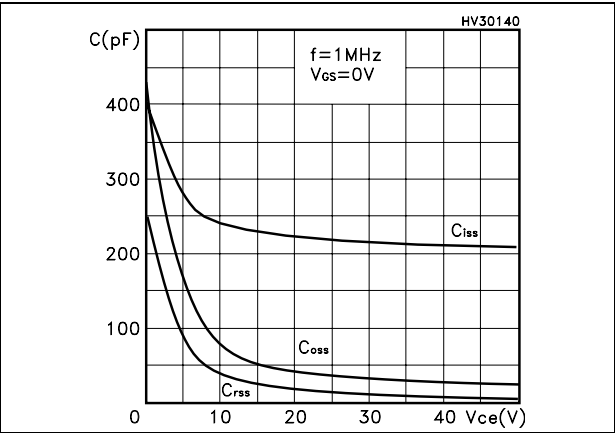


Figure 7. Normalized gate threshold voltage vs temperature

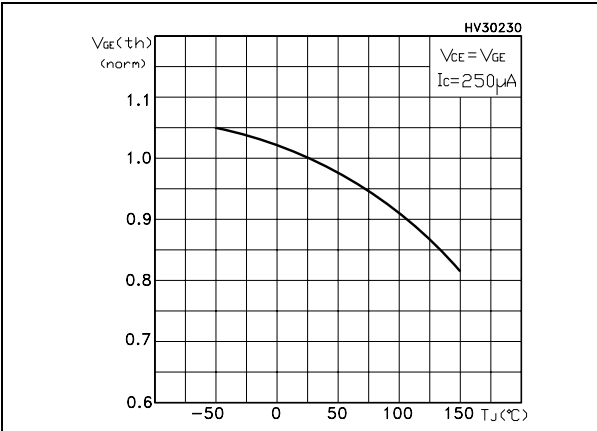


Figure 8. Collector-emitter on voltage vs collector current

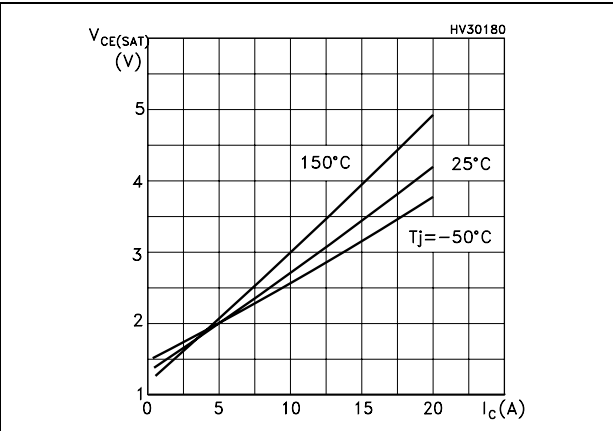


Figure 9. Normalized breakdown voltage vs temperature

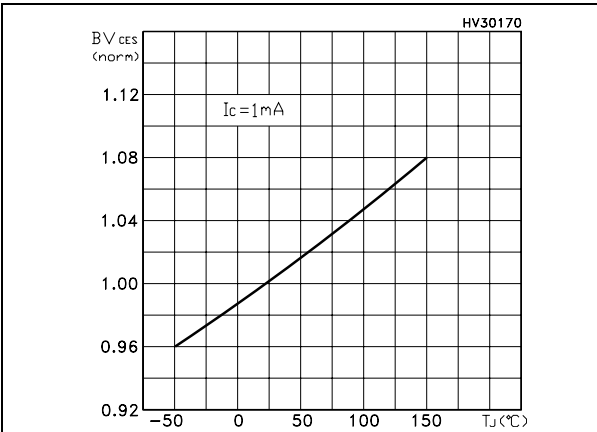


Figure 10. Switching losses vs temperature

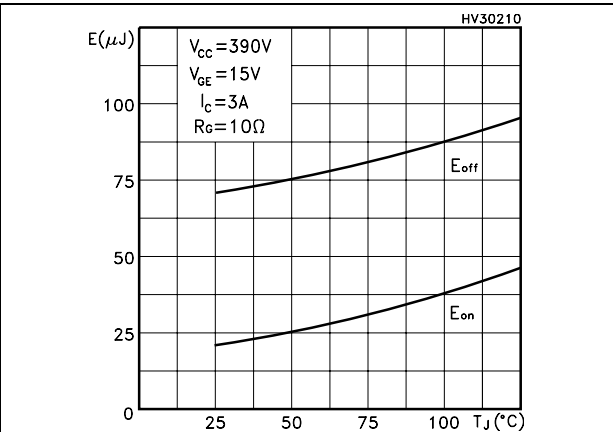


Figure 11. Switching losses vs gate resistance

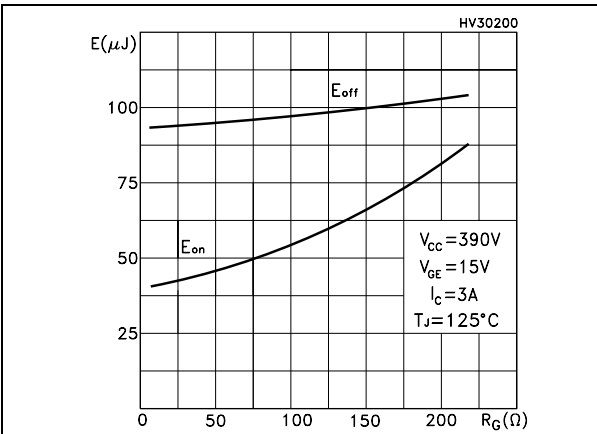


Figure 12. Switching losses vs collector current

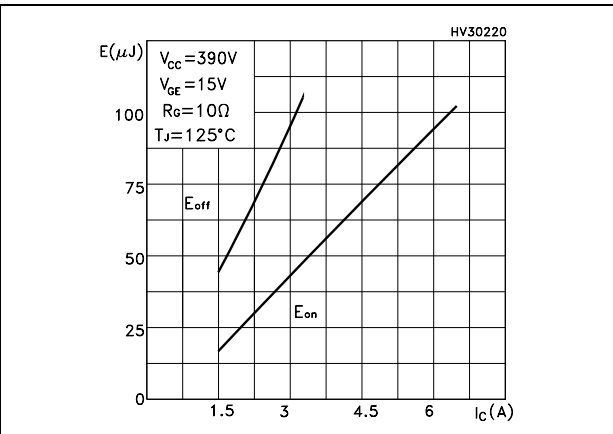


Figure 13. Thermal impedance

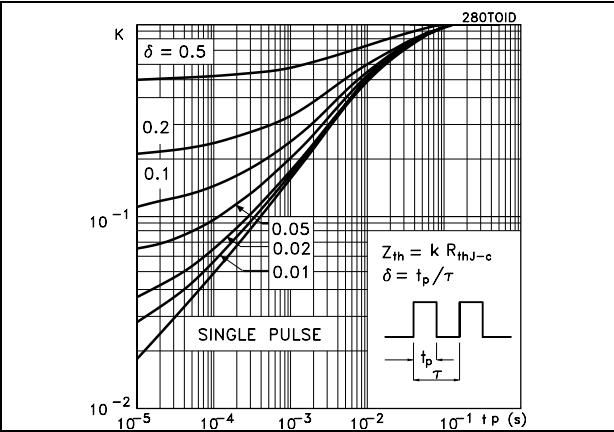
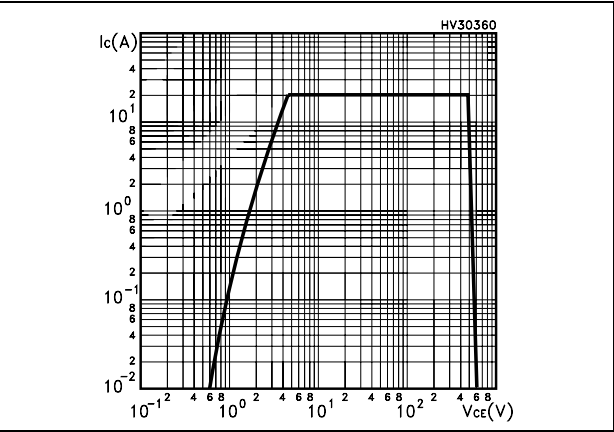


Figure 14. Turn-off SOA



3 Test circuit

Figure 15. Test circuit for inductive load switching

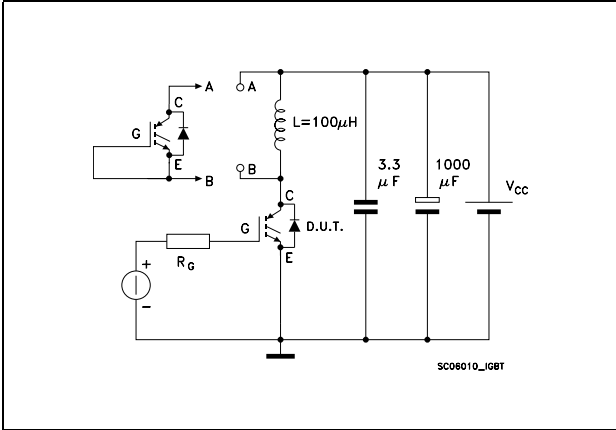


Figure 16. Gate charge test circuit

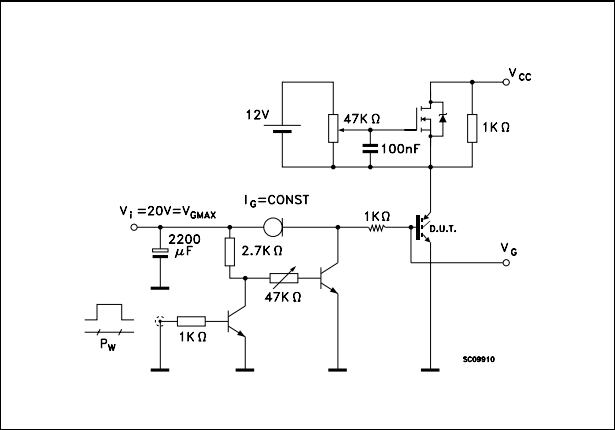


Figure 17. Switching waveform

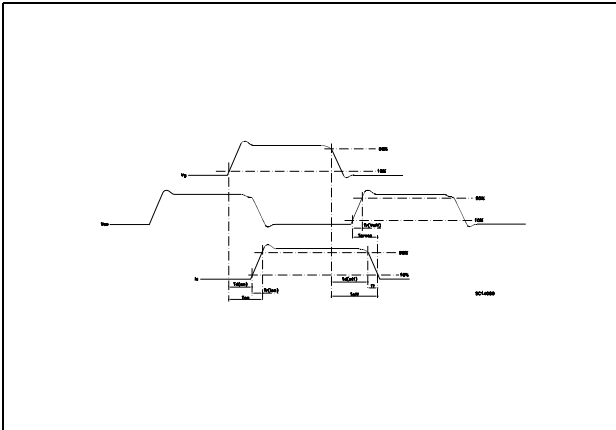
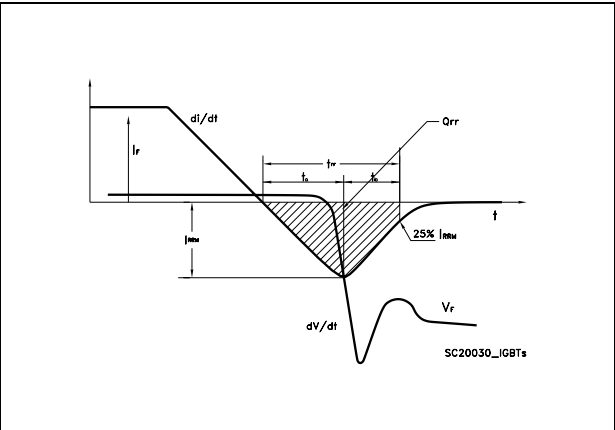


Figure 18. Diode recovery time waveform

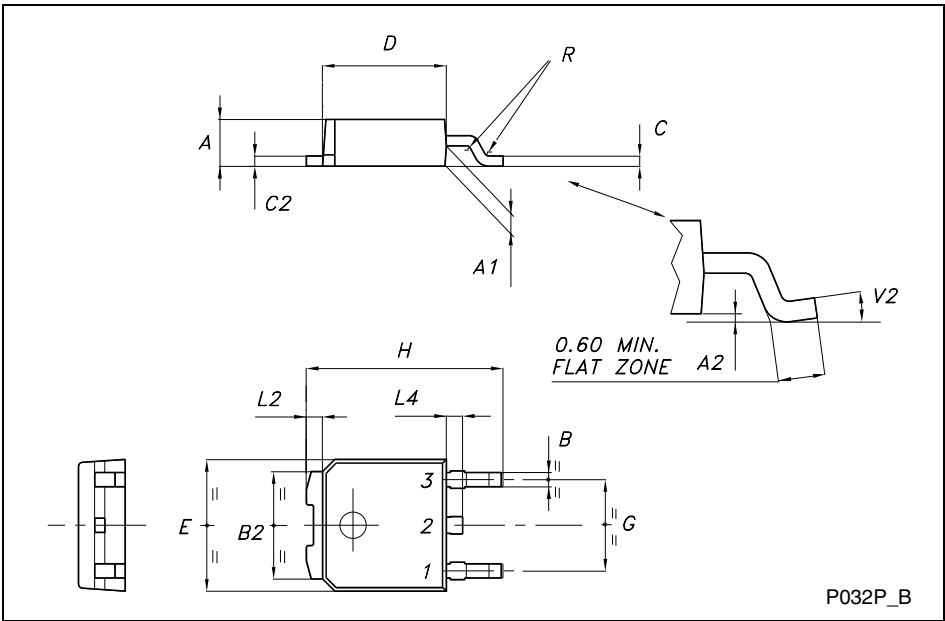


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-252 (DPAK) MECHANICAL DATA

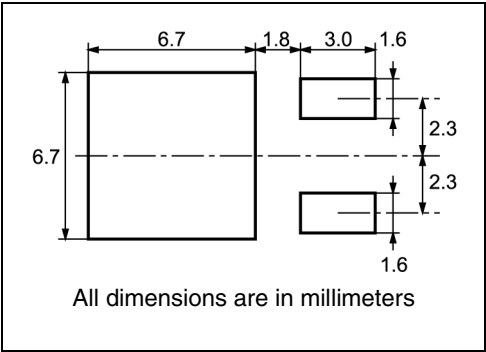
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



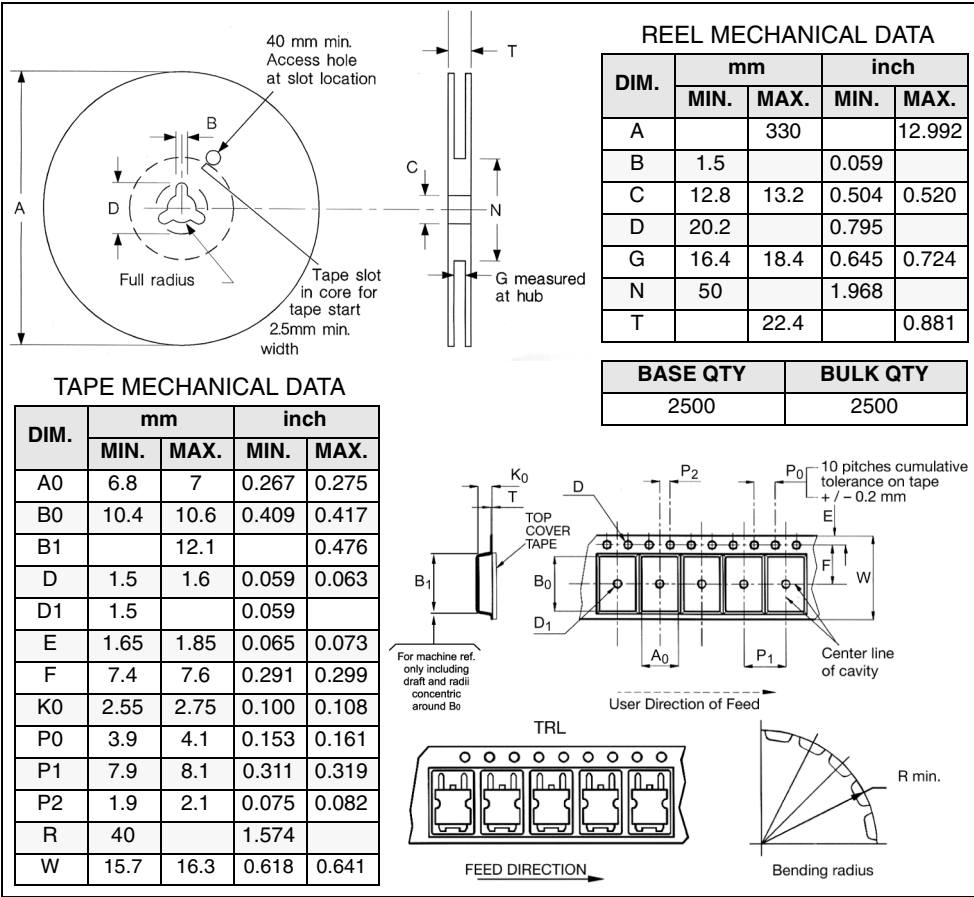
P032P_B

5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
14-Jun-2005	1	First Release
07-Mar-2006	2	Complete version
08-Feb-2007	3	The document has been reformatted

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