National Semiconductor

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LMV841
CMOS Input, RRIO, Wide Supply Range Operational Amplifier

General Description

The LMV841 is a low-voltage and low-power operational amplifier that operates from supply voltages from 2.7V to 12V and has rail-to-rail input and output capability.

The LMV841 is a low offset voltage and low supply current amplifier with MOS inputs, characteristics that make the LMV841 ideal for sensor interface and battery powered applications.

The LMV841 is offered in the space saving 5-Pin SC70 package. This small package is an ideal solution for area constrained PC boards and portable electronics.

Features

Unless otherwise noted, typical values at T_A = 25°C, V^+ = 5V

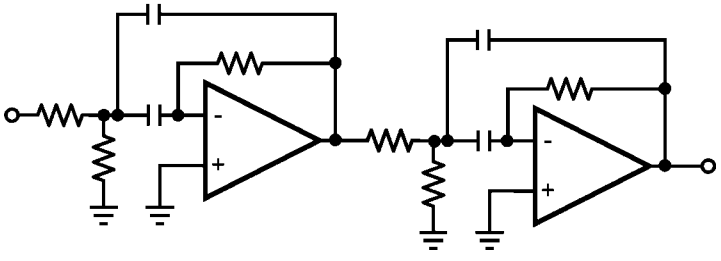
- Space saving 5-Pin SC70 package
- Supply voltage range 2.7V to 12V
- Guaranteed at 3.3V, 5V and ±5V
- Low supply current 1 mA
- Unity gain bandwidth 4.5 MHz
- Open loop gain 100 dB
- Input offset voltage 500 µV max
- Input bias current 0.3 pA
- CMRR 100 dB
- Input voltage noise 20 nV/$\sqrt{\text{Hz}}$
- Temperature range –40°C to 125°C
- Rail-to-rail input
- Rail-to-rail output

Applications

- High impedance sensor interface
- Battery powered instrumentation
- High gain amplifiers
- DAC buffer
- Instrumentation amplifiers
- Active Filters

Typical Application

Active Band-pass Filter



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2 kV
Machine Model	200V
V_{IN} Differential	±300 mV
Supply Voltage ($V^+ - V^-$)	13.2V
Voltage at Input/Output Pins	V^++0.3V, V^- −0.3V
Input Current	10 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to +125°C
Supply Voltage ($V^+ - V^-$)	2.7V to 12V
Package Thermal Resistance (θ_{JA} (Note 3))	
5-Pin SC70	334 °C/W

3.3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for at T_A = 25°C, V^+ = 3.3V, V^- = 0V, $V_{CM} = V^+/2$, and R_L > 10 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			8	±500 **±800**	µV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.5	**±5**	µV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.3V	84 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, $V_O = V^+/2$	86 **82**	100		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**−0.1**		**3.4**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = 0.3V to 3.0V	100 **96**	118		dB
		R_L = 10 kΩ V_O = 0.2V to 3.1V	100 **96**	129		
V_O	Output Swing High, measured from V^+	R_L = 2 kΩ to $V^+/2$		50	80 **120**	mV
		R_L = 10 kΩ to $V^+/2$		25	40 **60**	
	Output Swing Low, measured from V^-	R_L = 2 kΩ to $V^+/2$		50	70 **90**	mV
		R_L = 10 kΩ to $V^+/2$		23	45 **55**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing $V_O = V^+/2$ V_{IN} = 100 mV	25 **20**	30		mA
		Sinking $V_O = V^+/2$ V_{IN} = −100 mV	25 **20**	30		
I_S	Supply Current			0.98	1.2 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 2.3 V_{PP} 10% to 90%		2.5		V/µs
GBW	Gain Bandwidth Product			4.5		MHz
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for at T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L > 10 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			–5	±500 **±800**	µV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.35	**±5**	µV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	86 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = V^+/2	86 **82**	100		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**–0.2**		**5.2**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = 0.3V to 4.7V	100 **96**	118		dB
		R_L = 10 kΩ V_O = 0.2V to 4.8V	100 **96**	129		
V_O	Output Swing High, measured from V^+	R_L = 2 kΩ to V^+/2		60	100 **120**	mV
		R_L = 10 kΩ to V^+/2		30	50 **70**	
	Output Swing Low, measured from V^-	R_L = 2 kΩ to V^+/2		60	90 **100**	mV
		R_L = 10 kΩ to V^+/2		27	40 **50**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = V^+/2 V_{IN} = 100 mV	25 **20**	30		mA
		Sinking V_O = V^+/2 V_{IN} = –100 mV	25 **20**	30		
I_S	Supply Current			1.02	1.5 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 4 V_{PP} 10% to 90%		2.5		V/µs
GBW	Gain Bandwidth Product			4.5		MHz
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω

±5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for at T_A = 25°C, V^+ = 5V, V^- = –5V, V_{CM} = 0V, and R_L > 10 MΩ to V_{CM}. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			–17	±500 **±800**	µV
TCV_{OS}	Input Offset Voltage Drift (Note 7)			0.25	**±5**	µV/°C
I_B	Input Bias Current (Notes 7, 8)			0.3	10 **300**	pA
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	–5V ≤ V_{CM} ≤ 5V	86 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = 0V	86 **82**	100		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	**–5.2**		**5.2**	V
A_{VOL}	Large Signal Voltage Gain	R_L = 2 kΩ V_O = –4.7V to 4.7V	100 **96**	118		dB
		R_L = 10 kΩ V_O = –4.8V to 4.8V	100 **96**	129		
V_O	Output Swing High, measured from V^+	R_L = 2 kΩ to 0V		88	120 **155**	mV
		R_L = 10 kΩ to 0V		40	75 **95**	
	Output Swing Low, measured from V^-	R_L = 2 kΩ to 0V		85	125 **140**	mV
		R_L = 10 kΩ to 0V		36	50 **70**	
I_O	Output Short Circuit Current (Notes 3, 9)	Sourcing V_O = 0V V_{IN} = 100 mV	25 **20**	30		mA
		Sourcing V_O = 0V V_{IN} = –100 mV	25 **20**	30		
I_S	Supply Current			1.11	1.7 **2**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 9 V_{PP} 10% to 90%		2.5		V/µs
GBW	Gain Bandwidth Product			4.5		MHz
Φ_m	Phase Margin			67		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz		20		$nV/\sqrt{Hz}$
R_{OUT}	Open Loop Output Impedance	f = 3 MHz		70		Ω

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

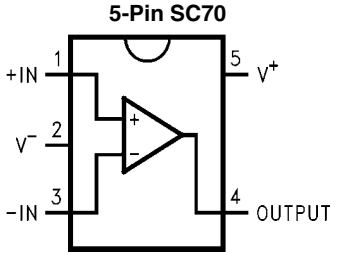
Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 8: Positive current corresponds to current flowing into the device.

Note 9: Short circuit test is a momentary test.

Note 10: Number specified is the slower of positive and negative slew rates.

Connection Diagram



Top View

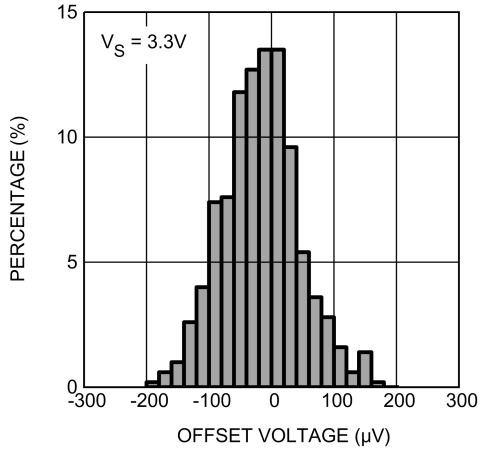
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70	LMV841MG	A97	1k Units Tape and Reel	MAA05A
	LMV841MGX		3k Units Tape and Reel	

Typical Performance Characteristics

At T_A = 25°C, R_L = 10 kΩ, V_S = 5V. Unless otherwise specified.

Offset Voltage Distribution



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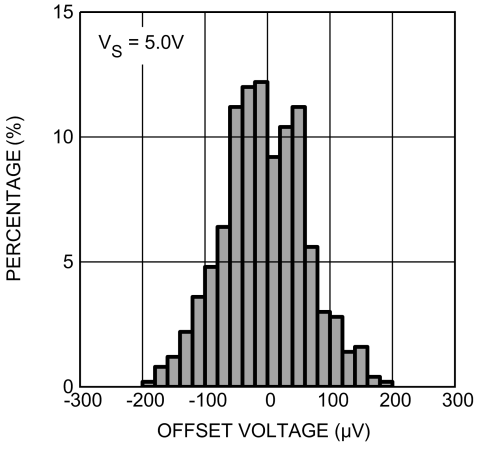
Offset Voltage Distribution



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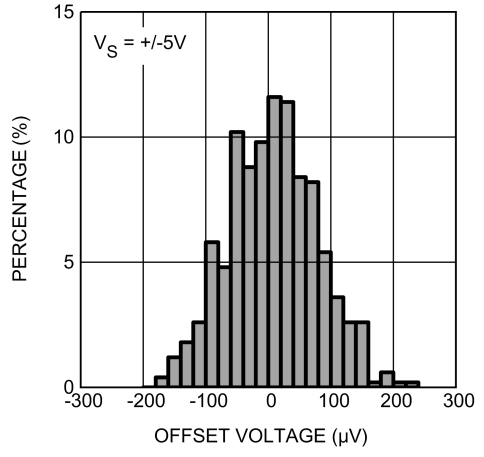
Offset Voltage Distribution



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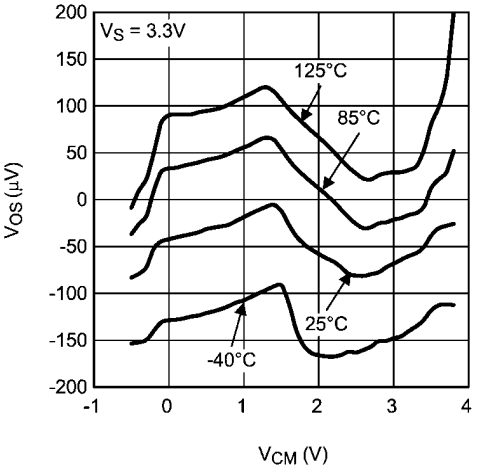
V_{OS} vs. V_{CM} Over Temperature @ 3.3V



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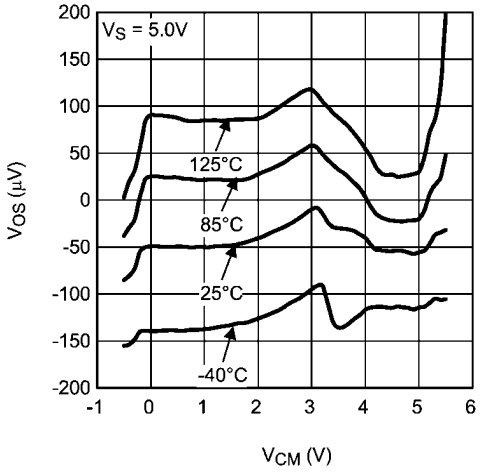
V_{OS} vs. V_{CM} Over Temperature @ 5.0V



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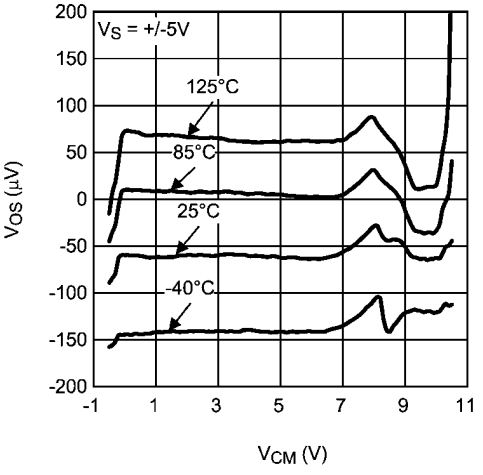
V_{OS} vs. V_{CM} Over Temperature @ ±5.0V



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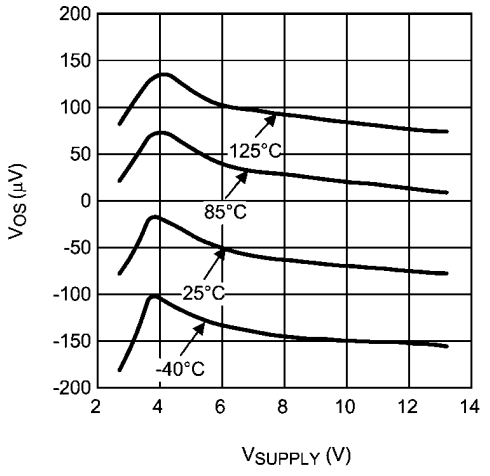
V_{OS} vs. Supply Voltage



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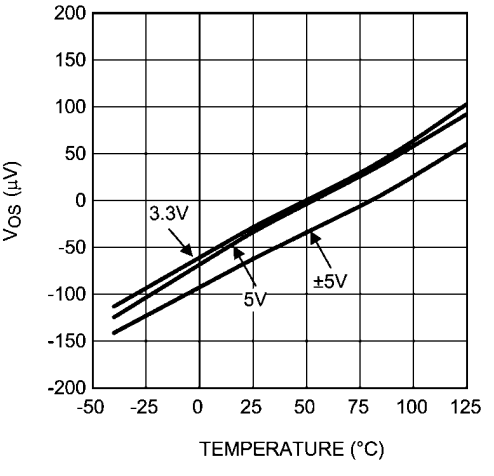
V_{OS} vs. Temperature



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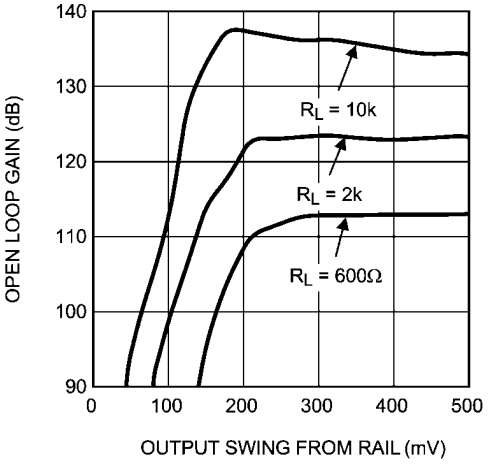
DC Gain vs. V_{OUT}



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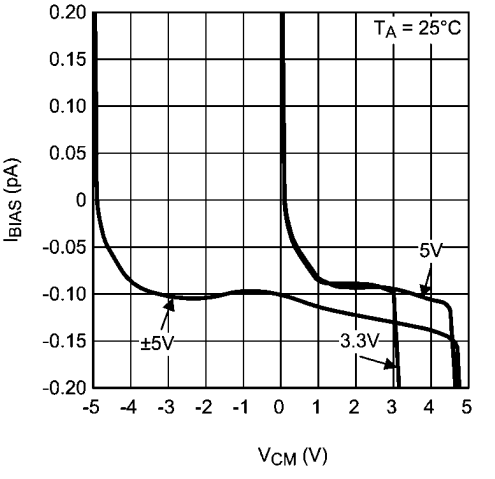
Input Bias Current vs. V_{CM}



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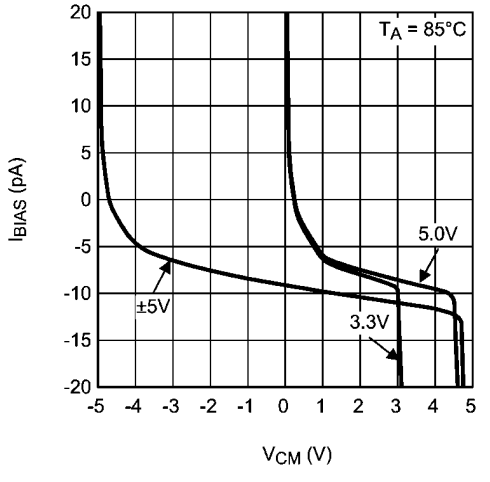
Input Bias Current vs. V_{CM}



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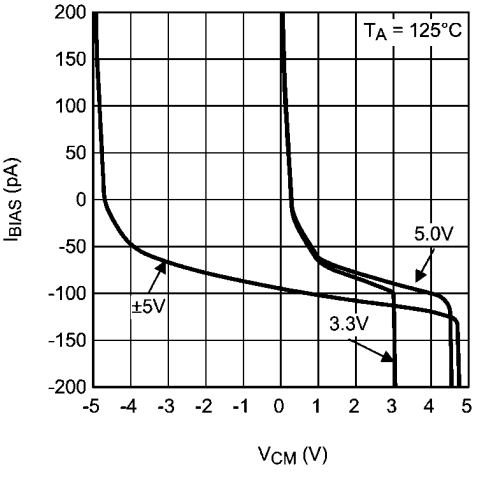
Input Bias Current vs. V_{CM}



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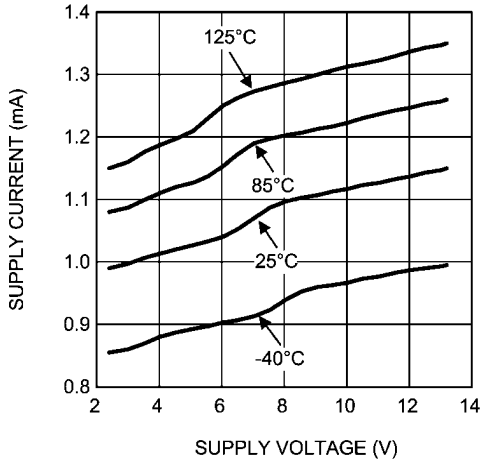
Supply Current vs. Supply Voltage



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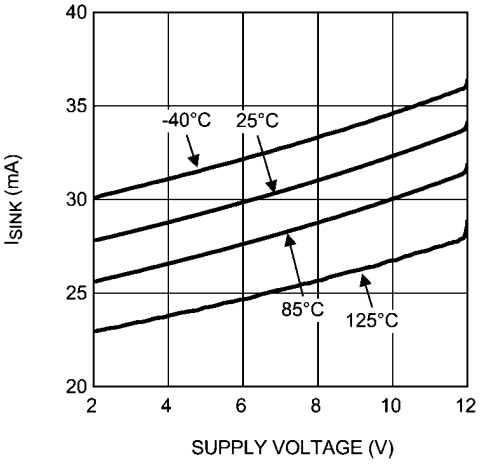
Sinking Current vs. Supply Voltage



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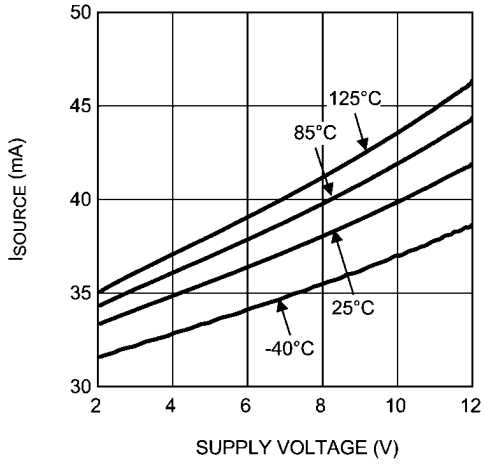
Sourcing Current vs. Supply Voltage



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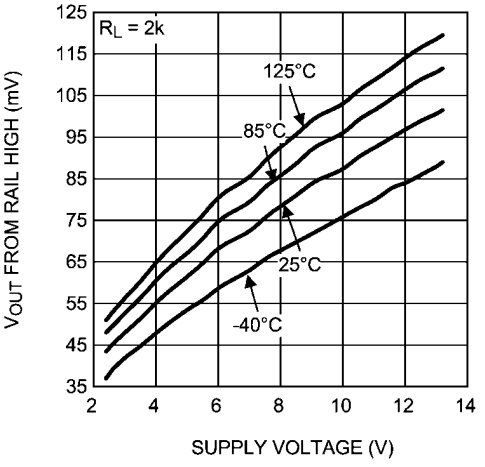
Output Swing High vs. Supply Voltage R_L = 2k



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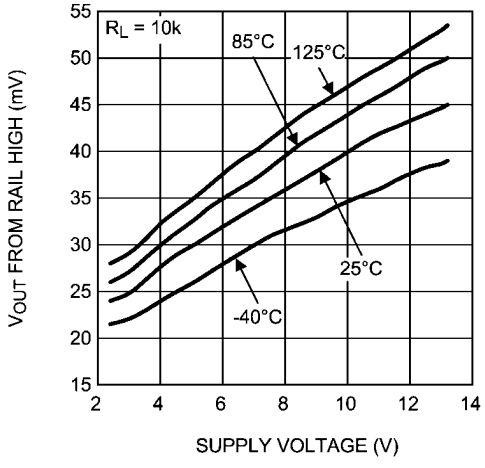
Output Swing High vs. Supply Voltage R_L = 10k



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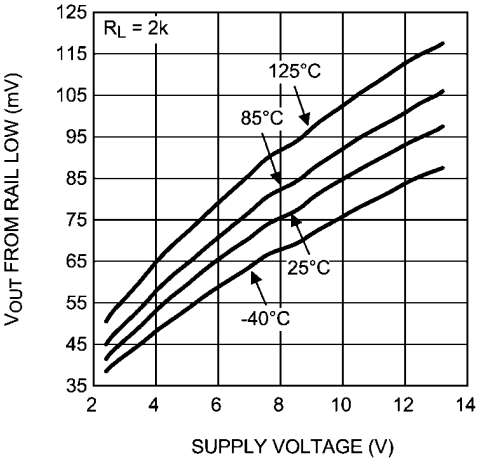
Output Swing Low vs. Supply Voltage R_L = 2k



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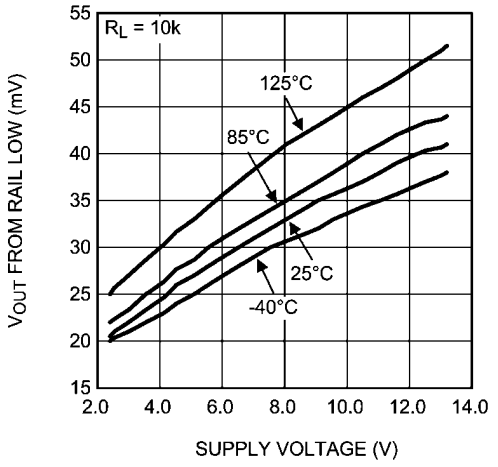
Output Swing Low vs. Supply Voltage R_L = 10k



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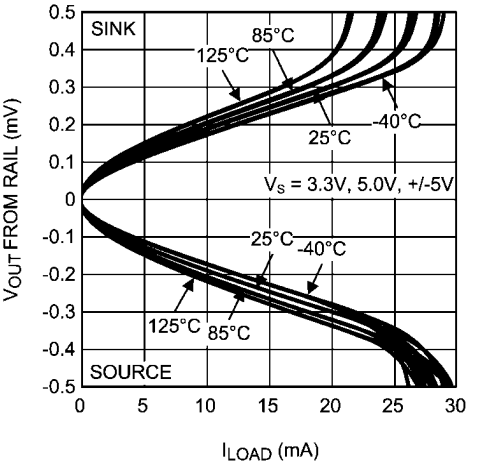
Output Voltage Swing vs. Load Current



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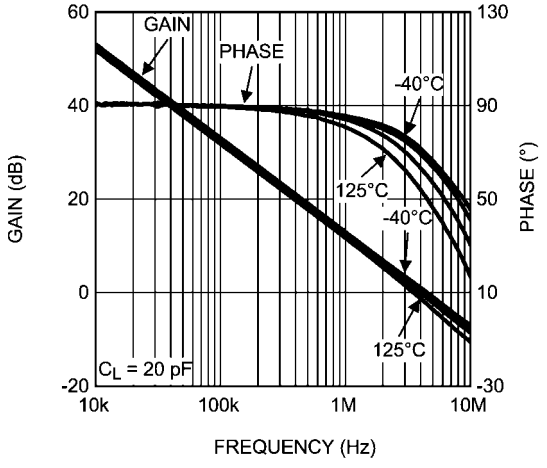
Open Loop Frequency Response Over Temperature



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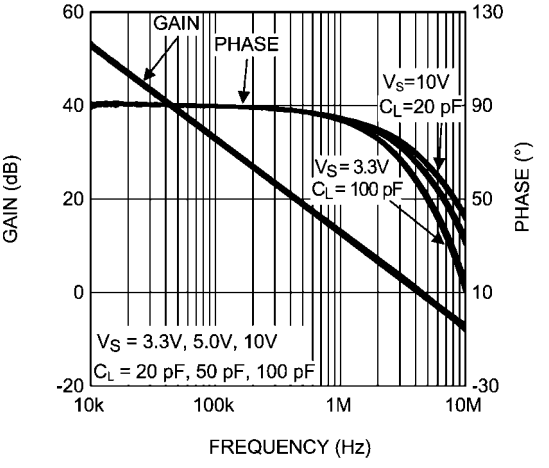
Open Loop Frequency Response Over Load Conditions



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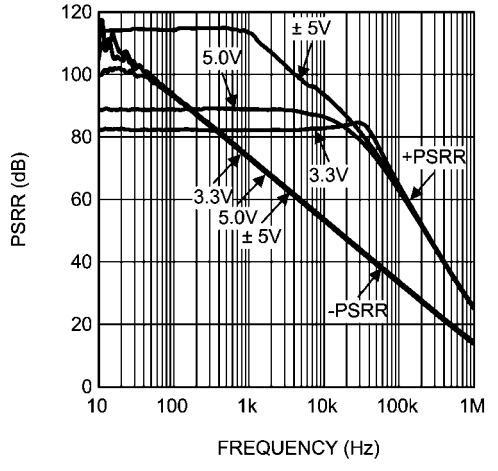
PSRR vs. Frequency



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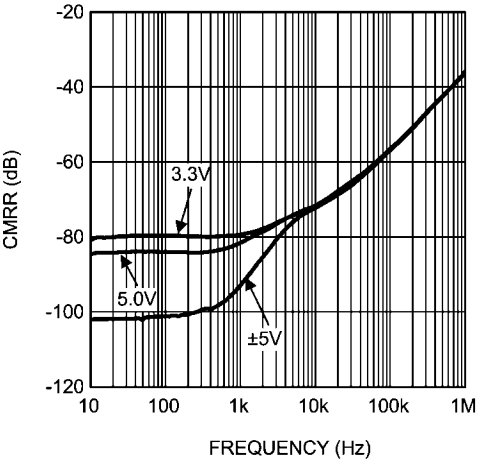
CMRR vs. Frequency



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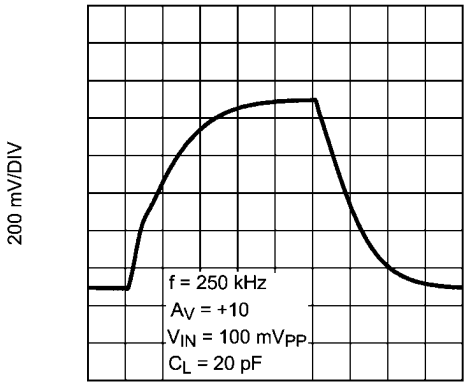
Large Signal Step Response @ GAIN = 10



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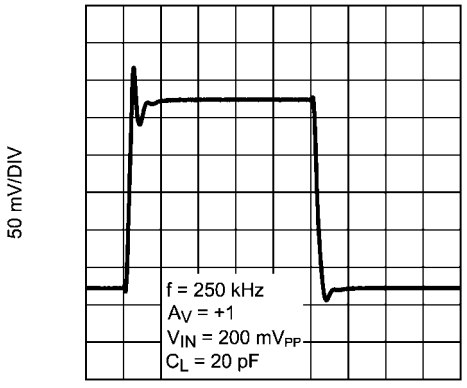
Small Signal Step Response @ GAIN = 1



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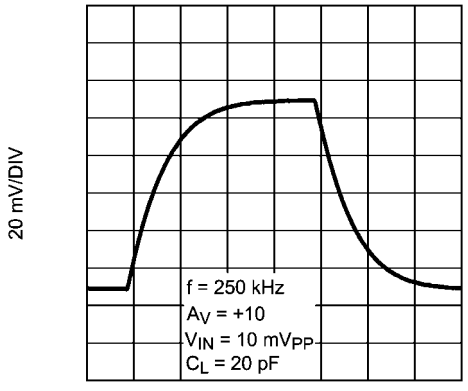
Small Signal Step Response @ GAIN = 10



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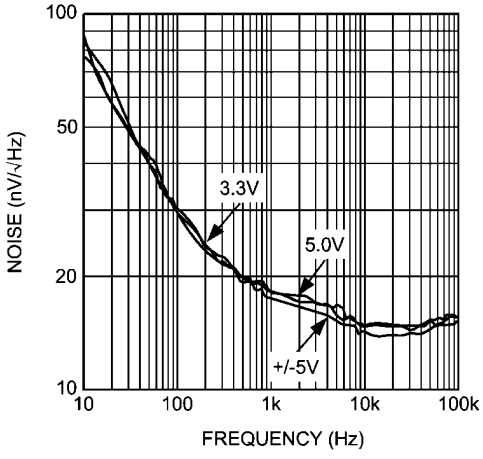
Input Voltage Noise vs. Frequency



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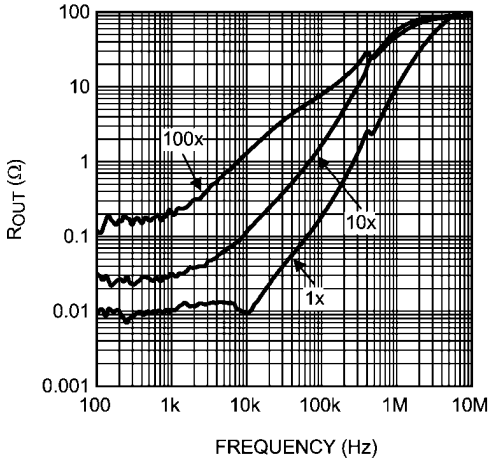
Closed Loop Output Impedance vs Frequency



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Application Information

INTRODUCTION

The LMV841 is an operational amplifier with near-precision specifications: low noise, low temperature drift, low offset and rail-to-rail input and output.

The low supply current, a temperature range of −40°C to 125° C, the 12V supply with CMOS input and the small SC70 package make this a unique op amp.

Possible applications include instrumentation, medical, test equipment, audio and automotive applications.

The small SC70 package and the low supply current, 1 mA, makes the LMV841 a perfect choice for portable electronics.

INPUT PROTECTION

The LMV841 has a set of anti-parallel diodes D_1 and D_2 between the input pins, as shown in *Figure 1*. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins.

A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

Note that when the op amp is slewing, a differential input voltage exists that forward biases the protection diodes. This may result in current being drawn from the signal source. While this current is already limited by the internal resistors R_1 and R_2 (both 130Ω), a resistor of 1 kΩ can be placed in the feedback path, or a 500Ω resistor can be placed in series with the input signal.

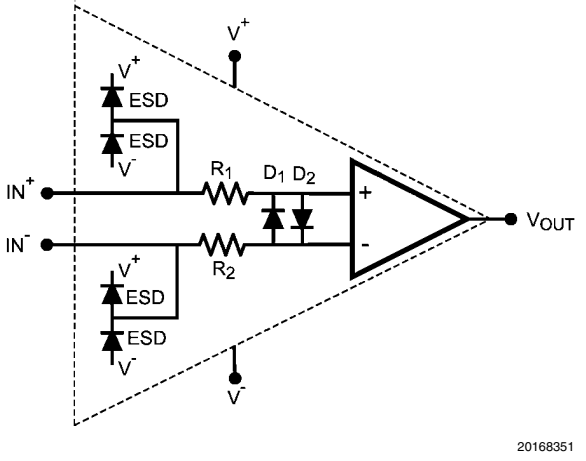


FIGURE 1. Protection diodes between the input pins

INPUT STAGE

The input stage of this Amplifier exists of a PMOS and an NMOS input pair to achieve a more than rail-to-rail input range.

For input voltages close to the negative rail, only the PMOS pair is active. Close to the positive rail, only the NMOS pair is active.

For intermediate signals, the transition from PMOS pair to NMOS pair will result in a very small offset shift, which appears at approximately 1 volt from the positive rail.

To reduce this small offset shift, the amplifier is trimmed during production, resulting in an input offset voltage of less then 1mV at room temperature over the total input range.

CAPACITIVE LOAD

The LMV841 can be connected as a non-inverting unity-gain amplifier. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be underdamped which causes peaking in the transfer and when there is too much peaking the op amp might start oscillating.

In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in *Figure 2*. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

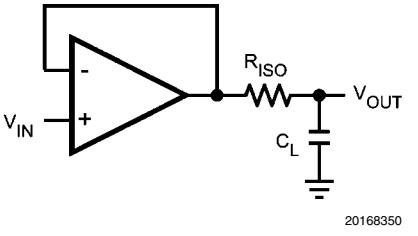


FIGURE 2. Isolating Capacitive Load

REDUCING OVERSHOOT

When the output of the op amp is at its lower swing limit (i.e. saturated near V^-), rapidly rising signals can cause some overshoot.

This overshoot can be reduced by adding a resistor from the output to V^+. Even in extreme situations at high temperatures, a 10k resistor is sufficient to reduce the overshoot to negligible levels.

The resistor at the output will however reduce the maximum output swing, as would any resistive load at the output.

DECOUPLING AND LAYOUT

Care must be taken when creating the board layout for the op amp.

For decoupling of the supply lines 10 nF capacitors are suggested to be placed as close as possible to the op amp.

For single supply, place a capacitor between V^+ and V^-. For dual supplies, place one capacitor between V^+ and the board ground, and the second capacitor between ground and V^-.

NOISE DUE TO RESISTORS

The LMV841 has good noise specifications, and will frequently be used in low noise applications. Therefore it is important to take in account the influence of the resistors to the total noise contribution.

For applications with a voltage input configuration it is, in general, beneficial to keep the resistor values low. In these configurations high resistor values mean high noise levels.

However, using low resistor values will increase the power consumption of the application. This is not always acceptable for portable applications.

To determine if the noise is acceptable for the application, use the following formula for resistor noise :

$$e_{th} = \sqrt{4kTRB}$$

where:

e_{th} = Thermal noise voltage (Vrms)

k = Boltzmann constant (1.38 x 10–23 J/K)

T = Absolute temperature (K)

R = Resistance (Ω)

B = Noise bandwidth (Hz), fmax - fmin

Given in an example with a resistor of 1MOhm at 25°C (298 K) over a frequency range of 100 kHz:

$$e_{th} = \sqrt{4kTRB}$$
$$= \sqrt{4 \times 1.38 \times 10^{-23} J/K \times 298K \times 1\ M\Omega \times 100\ kHz}$$
$$= 40\ \mu V = -88\ dBV$$

To keep the noise of the application low it might be necessary to decrease the resistors to 100k, which will decrease the noise to –97.8 dBV (12.8 uV).

The op amp's input-referred noise of 20 nV/$\sqrt{Hz}$ at 1 kHz is equivalent to the noise of a 24 kΩ resistor.

ACTIVE FILTER

The rail-to-rail input and output of the LMV841, and its wide supply voltage range makes this amplifier ideal to use in numerous applications. One of the typical applications is an active filter as shown in *Figure 3*. This example is a band-pass filter, for which the pass band is widened. This is achieved by cascading two band-pass filters, with slightly different centre frequencies.

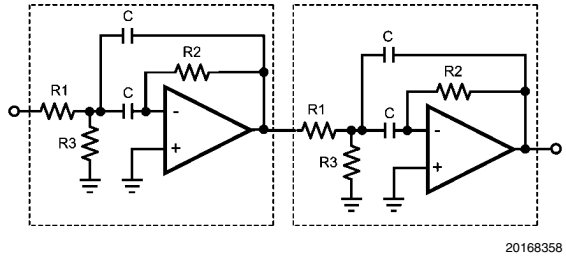


FIGURE 3. Active Filter

The centre frequency of the separate band-pass filters can be calculated by:

$$f_{mid} = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1\ R_2\ R_3}}$$

In this example a filter was designed with its pass band at 10 kHz. The two separate band-pass filters are designed to have a centre frequency of approximately 10% from the frequency of the total filter:

C = 33 nF

R1 = 2 kΩ

R2 = 6.2 kΩ

R3 = 45 Ω

This will give for Filter A

$$f_{mid} = \frac{1}{\pi \times 33\ nF}\sqrt{\frac{2\ k\Omega + 6.2\ k\Omega}{2\ k\Omega \times 6.2\ k\Omega \times 45\Omega}} = 9.2\ kHz$$

And for filter B with C = 27 nF:

$$f_{mid} = \frac{1}{\pi \times 27\ nF}\sqrt{\frac{2\ k\Omega + 6.2\ k\Omega}{2\ k\Omega \times 6.2\ k\Omega \times 45\Omega}} = 11.2\ kHz$$

Bandwidth can be calculated by:

$$B = \frac{1}{\pi R_2 C}$$

For filter A this will give

$$B = \frac{1}{\pi \times 6.2\ k\Omega \times 33\ nF} = 1.6\ kHz$$

and for filter B:

$$B = \frac{1}{\pi \times 6.2\ k\Omega \times 27\ nF} = 1.9\ kHz$$

The response of the two filters and the combined filter is shown in *Figure 4*.

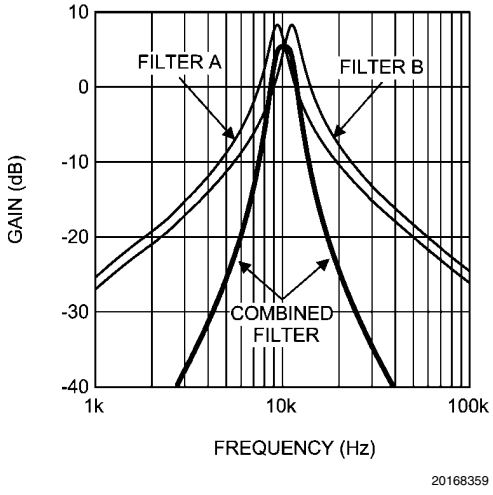


FIGURE 4. Active Filter Curve

The filter responses of filter A and filter B are shown as the thin lines in *Figure 4*, the response of the combined filter is shown as the thick line. By shifting the centre frequencies of the separate filters further apart, the result will be a wider band, however positioning the centre frequencies too far apart will result in a less flat gain within the band. For wider bands more band-pass filters can be cascaded.

Tip: use the WEBENCH internet tools at www.national.com for your filter application

HIGH IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10 MOhm. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier.

The input bias current of this amplifier can load the sensor's output and cause a voltage drop across the source resistance as shown in *Figure 5*, where $V_{IN}+ = V_S - I_B * R_S$. The last term, $I_B * R_S$, is the voltage drop across R_S.

The LMV841 can be used to prevent errors introduced to the system due to this voltage drop. The very low input bias current of the LMV841 is a must for the use with high impedance sensors. This is to keep the error contribution by $I_B * R_S$ negligibly small.

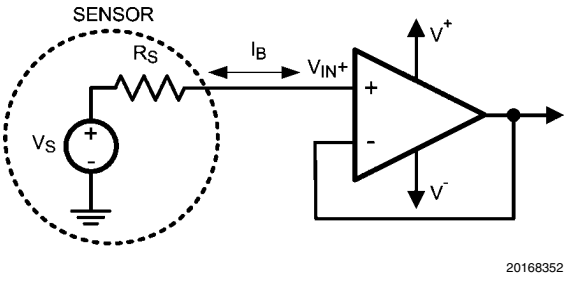


FIGURE 5. High Impedance Sensor Interface

THERMOCOUPLE AMPLIFIER

The LMV841 is also a very good choice to be used in a thermocouple amplifier application as shown in the example below. The low source impedance of the thermocouple makes it possible to use a single differential amplifier. A differential amplifier is used to remove common-mode noise, picked up by the wires.

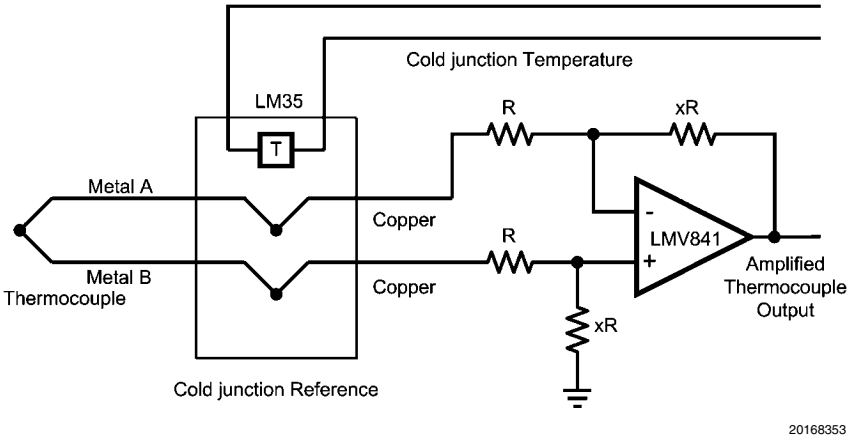
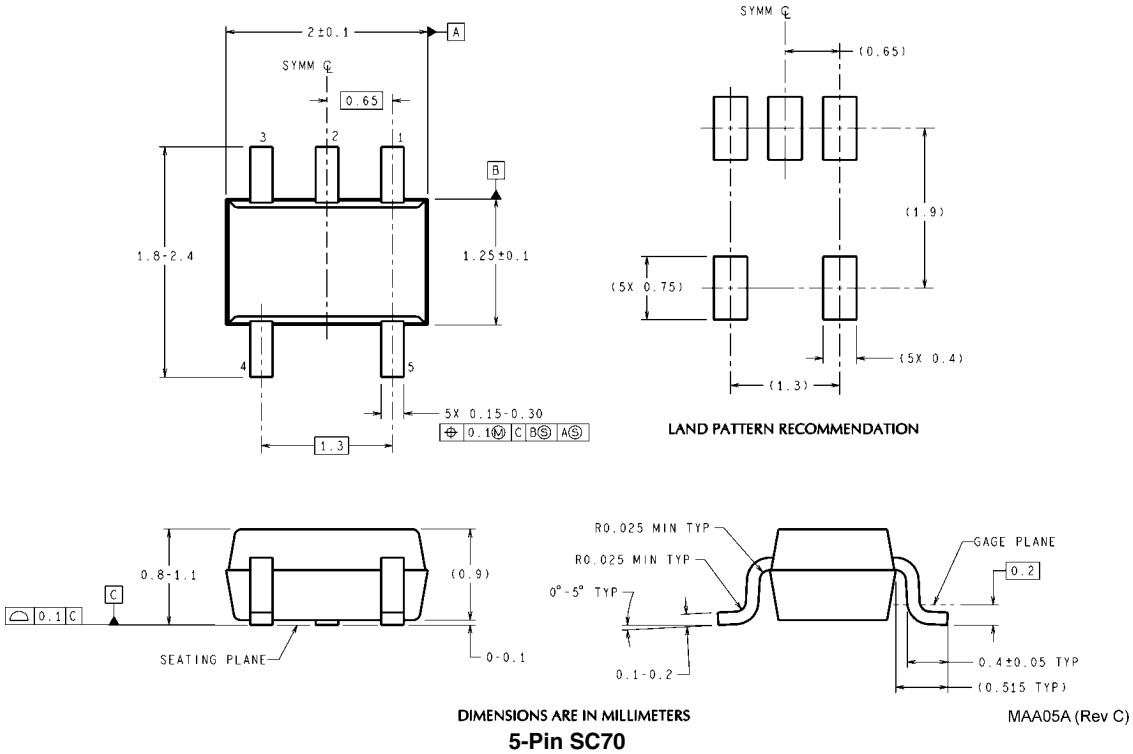


FIGURE 6. Thermocoupler Amplifier

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

MAA05A (Rev C)

5-Pin SC70
NS Package Number MAA05A

Notes

Notes

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