PCI EXPRESS™ CLOCK GENERATOR

ICS841S01

General Description

The ICS841S01 is a PLL-based clock generator specifically designed for PCI_Express™Clock Generation applications. This device generates a 100MHz HCSL clock. The device offers a HCSL (Host Clock Signal Level) clock output from a clock input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating.

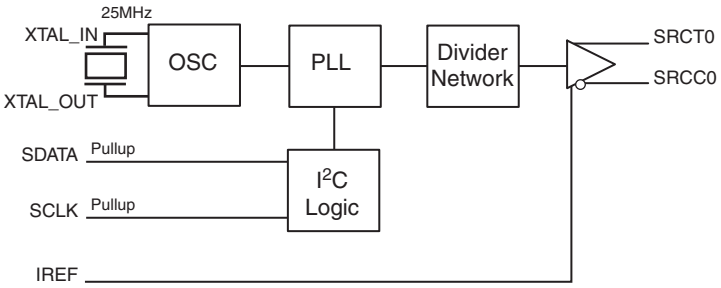
The device offers spread spectrum clock output for reduced EMI applications. An I²C bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -0.5%.

The ICS841S01 is available in both standard and lead-free 16-Lead TSSOP packages.

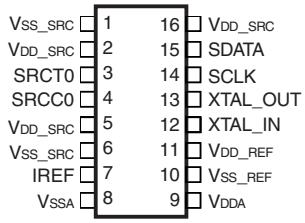
Features

- One 0.7V current mode differential HCSL output pair
- Crystal oscillator interface, 25MHz
- Output frequency: 100MHz
- RMS period jitter: 3ps (maximum)
- Cycle-to-cyle jitter: 35ps (maximum)
- I²C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS841S01
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6	V_{SS_SRC}	Power		Ground for core and SRC outputs.
2, 5, 16	V_{DD_SRC}	Power		Power supply for core and SRC outputs.
3, 4	SRCT0, SRCC0	Output		Differential output pair. HCSL interface levels.
7	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode SRCC0, SRCT0 clock outputs.
8	V_{SSA}	Power		Analog ground pin.
9	V_{DDA}	Power		Power supply for PLL.
10	V_{SS_REF}	Power		Ground for crystal interface
11	V_{DD_REF}	Power		Power supply for crystal interface.
12, 13	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
14	SCLK	Input	Pullup	SMBus compatible SCLK. This pin has an internal pullup resistor, but is in high impedance in powerdown mode. LVCMOS/LVTTL interface levels.
15	SDATA	Input/ Output	Pullup	SMBus compatible SDATA. This pin has an internal pullup resistor, but is in high impedance in powerdown mode. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{OUT}	Output Pin Capacitance			4		pF

SERIAL DATA INTERFACE

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

DATA PROTOCOL

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3A.*

The block write and block read protocol is outlined in *Table 3B*, while *Table 3C* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

TABLE 3A. COMMAND CODE DEFINITION

BIT	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
6:5	Chip select address, set to "00" to access device.
4:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be "00000".

TABLE 3B. BLOCK READ AND BLOCK WRITE PROTOCOL

BIT	Description = Block Write	BIT	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 1 - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 - 8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte/Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave / Acknowledges
			Data Byte N from slave - 8 bits
			Not Acknowledge

TABLE 3C. BYTE READ AND BYTE WRITE PROTOCOL

BIT	Description = Byte Write	BIT	Description = Byte Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data from slave - 8 bits
		38	Not Acknowledge
		39	Stop

CONTROL REGISTERS

TABLE 4A. BYTE 0:CONTROL REGISTER 0

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z) 1 = Enable
1	0	Reserved	Reserved
0	0	Reserved	Reserved

TABLE 4B. BYTE 1:CONTROL REGISTER 1

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

TABLE 4C. BYTE 2:CONTROL REGISTER 2

BIT	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection 0 = -0.35%, 1 = -0.50%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	1	Reserved	Reserved

TABLE 4D. BYTE 3:CONTROL REGISTER 3

BIT	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

TABLE 4E. BYTE 4:CONTROL REGISTER 4

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

TABLE 4F. BYTE 5:CONTROL REGISTER 5

BIT	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

TABLE 4G. BYTE 6:CONTROL REGISTER 6

BIT	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF/N or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

TABLE 4H. BYTE 7:CONTROL REGISTER 7

BIT	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	1		Vendor ID Bit 0

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD_REF} + 0.5 V
Outputs, V_O	-0.5V to V_{DD_SRC} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5A. Power Supply DC Characteristics, $V_{DD\_REF} = V_{DDA} = V_{DD\_SRC} = 3.3V±5\%$, $T_A = T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_REF}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD_REF} – 0.25	3.3	V_{DD_REF}	V
V_{DD_SRC}	Core/SRC Output Supply Voltage		3.135	3.3	3.465	V
I_{DD_REF}	Crystal Supply Current				8	mA
I_{DDA}	Analog Supply Current				25	mA
I_{DD_SRC}	Core/SRC Supply Current				130	mA

Table 5B. DC Characteristics, $V_{DD\_REF} = V_{DDA} = V_{DD\_SRC} = 3.3V±5\%$, $T_A = T_A = 0°C$ to 70°C

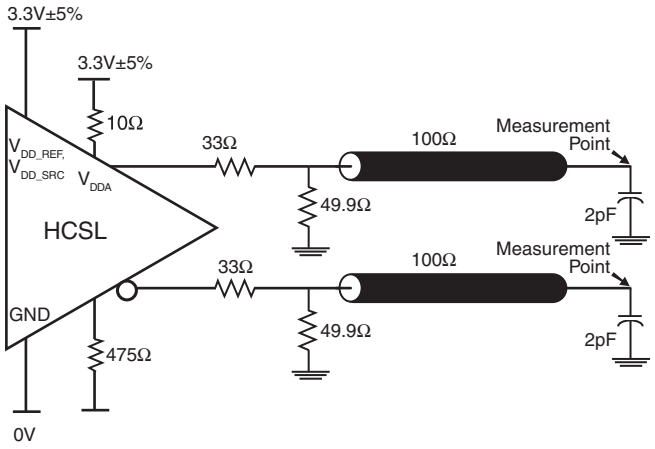
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IHSMBUS}$	Input High Voltage	SDATA, SCLK		2.2			V
$V_{ILSMBUS}$	Input Low Voltage	SDATA, SCLK				1.0	V
I_{IH}	Input High Current	SDATA, SCLK	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	SDATA, SCLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
I_{OH}	Output Current				14		mA
I_{OZ}	High Impedance Leakage Current			-10		10	µA

TABLE 6. AC CHARACTERISTICS, $V_{DD\_REF} = V_{DDA} = V_{DD\_SRC} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

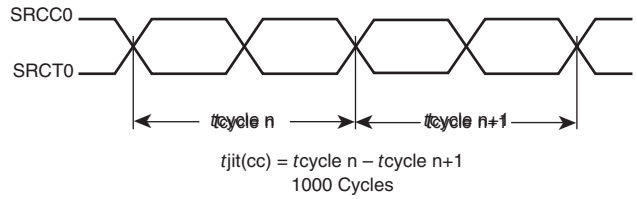
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fref	Frequency				25		MHz
sclk	SCLK Frequency					400	kHz
	Frequency Tolerance; NOTE 1	XTAL				50	ppm
		External Reference				0	ppm
odc	SRCT/SRCC Duty Cycle; NOTE 2, 7			47		53	%
t_{PERIOD}	Average Period; NOTE 3			9.9970		10.0533	ns
*t*jit(cc)	SRCT/C Cycle-to-Cycle Jitter; NOTE 2, 7					35	ps
*t*jit(per)	Period Jitter, RMS; NOTE 2, 7					3	ps
t_R / t_F	SRCT/SRCC Rise/Fall Time; NOTE 4		20% to 80%	175		700	ps
t_{RFM}	Rise/Fall Time Matching; NOTE 5					20	%
t_{DC}	XTAL_IN Duty Cycle; NOTE 6			47.5		52.5	%
Δt_R / t_F	Rise/Fall Time Variation					125	ps
V_{HIGH}	Voltage High			520		800	mv
V_{LOW}	Voltage Low			-150			mv
V_{OX}	Output Crossover Voltage		@ 0.7V Swing	250		550	mV
V_{OVS}	Maximum Overshoot Voltage					V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage			-0.3			V
V_{RB}	Ring Back Voltage					0.2	V

NOTE 1: With recommended crystal.
NOTE 2: Measured at crossing point V_{OX}.
NOTE 3: Measured at crossing point V_{OX} at 100MHz.
NOTE 4: Measured from V_{OL} = 0.175V to V_{OH} = 0.525V.
NOTE 5: Determined as a fraction of $2*(t_R - t_F) / (t_R + t_F)$.
NOTE 6: The device will operate reliably with input duty cycles up to 30/70% but the REF clock duty cycle will not be within specification
NOTE 7: Measured using a 50Ω to GND termination.

PARAMETER MEASUREMENT INFORMATION

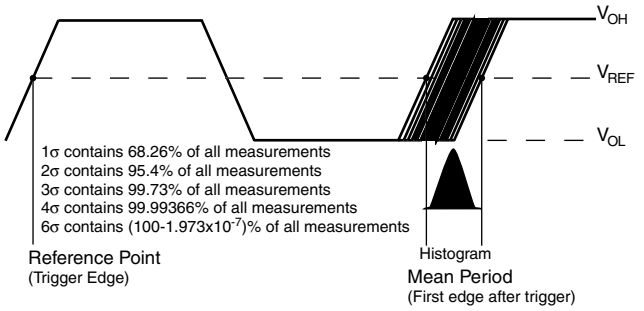


3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT

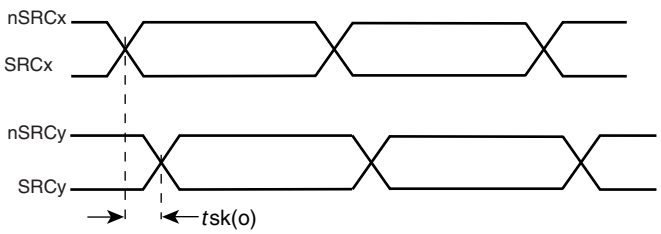


$t$jit(cc) = $t$cycle n – $t$cycle n+1
1000 Cycles

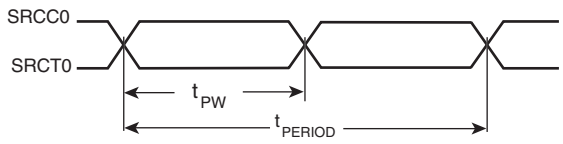
CYCLE-TO-CYCLE JITTER



RMS PERIOD JITTER

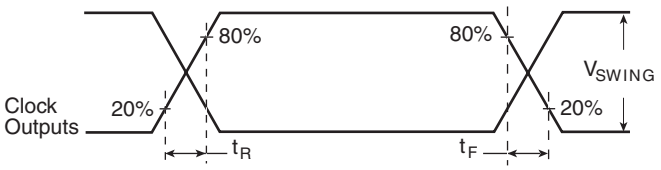


OUTPUT SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS841S01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD_REF}, V_{DDA}, and V_{DD_SRC} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

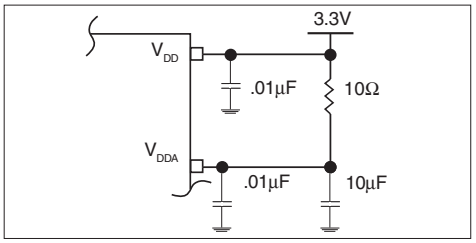


FIGURE 1. POWER SUPPLY FILTERING

USING THE ON-BOARD CRYSTAL OSCILLATOR

The ICS841S01 features a fully integrated Pierce oscillator to minimize system implementation costs. The ICS841S02I may be operated with a 25MHz crystal and without additional components. Recommended operation for the crystal should be of a parallel resonant type and a load specification of C_L = 18pF. See Table 7 for complete crystal specifications.

If more precise frequency control is desired, the addition of capacitors from each of the XTAL_IN and XTAL_OUT pins to ground may be used to trim the frequency as shown in Figure 2.

TABLE 7. RECOMMENDED CRYSTAL SPECIFICATIONS

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Shunt Capacitance (C_L)	5-7pF
Load Capacitance (C_O)	18pF
Equivalent Series Resistance (ESR)	20-50Ω

The crystal and optional trim capacitors should be located as close to the ICS841S01 XTAL_IN and XTAL_OUT pins as possible to avoid any board level parasitic.

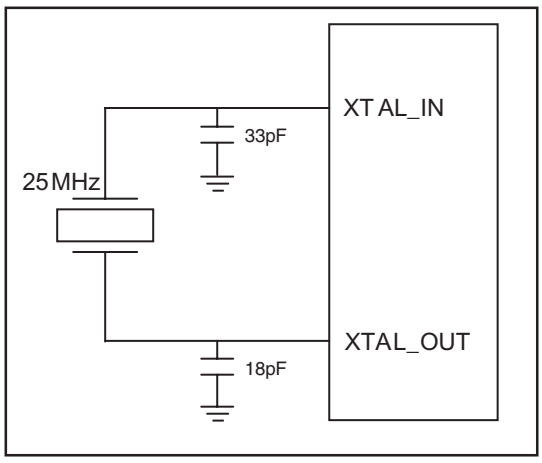


FIGURE 2. CRYSTAL OSCILLATOR WITH TRIM CAPACITOR

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Output Driver Current

The ICS841S01 outputs are HCSL current drive with the current being set with a resistor from I_{REF} to ground. For a 50Ω pc board trace, the drive current would typically be set with a R_{REF} of 475Ω which products an I_{REF} of 2.32mA. The I_{REF} is multiplied by a current mirror to an output drive of 6*2.32mA or 13.92mA. See *Figure 3* for current mirror and output drive details.

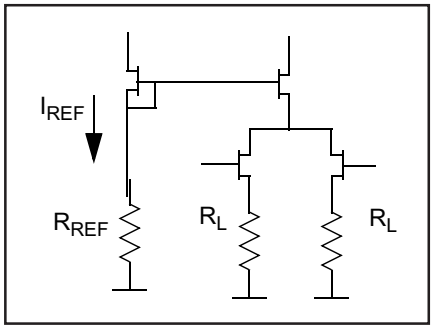


Figure 3. HCSL Current Mirror and Output Drive

RECOMMENDED TERMINATION

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB.

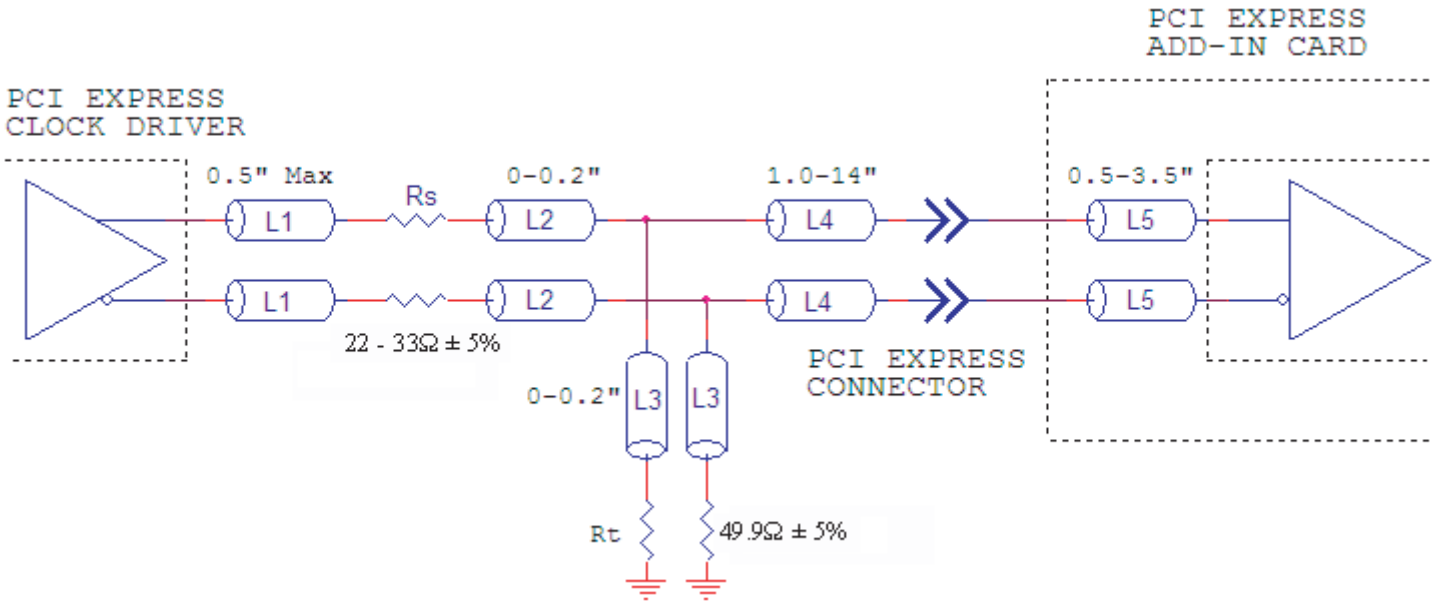


FIGURE 4A. RECOMMENDED TERMINATION

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

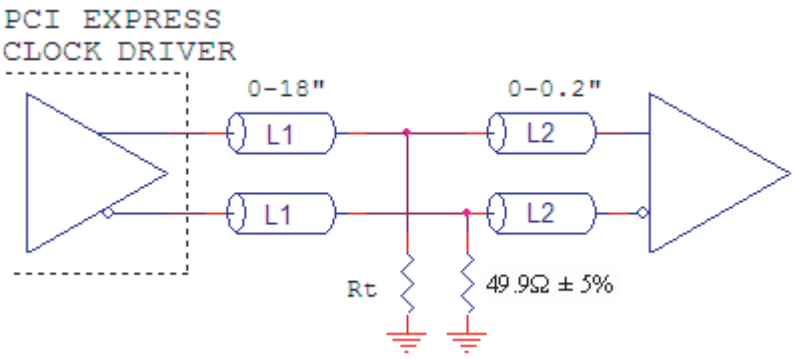


FIGURE 4B. RECOMMENDED TERMINATION

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS841S02 is: 1874

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

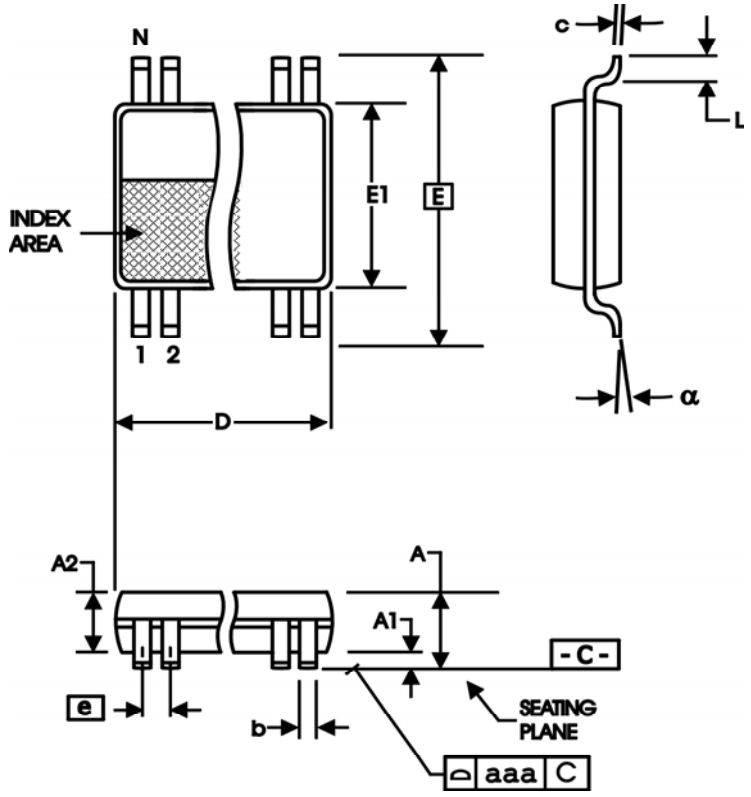


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS841S01BG	841S01BG	16 Lead TSSOP	tube	0°C to 70°C
ICS841S01BGT	841S01BG	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS841S01BGLF	841S01BL	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS841S01BGLFT	841S01BL	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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