



SCCS035 - September 1994 - Revised March 2000

# CY54/74FCT841T

## 10-Bit Latch

### Features

- Function, pinout, and drive compatible with FCT, F, and AM29841 logic
- FCT-C speed at 5.5 ns max. (Com'I)  
FCT-B speed at 6.5 ns max. (Com'I)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'I),  
32 mA (Mil)
- Source current 32 mA (Com'I),  
12 mA (Mil)

### High-speed parallel latches

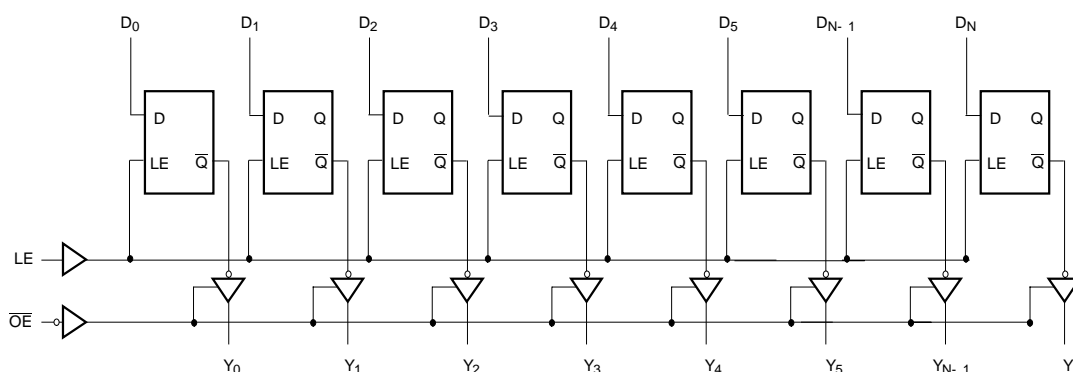
### Buffered common latch enable input

### Functional Description

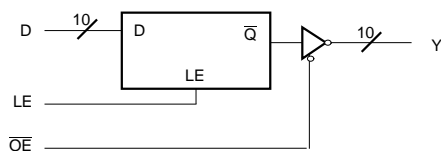
The FCT841T bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The FCT841T is a buffered 10-bit wide version of the FCT373 function.

The FCT841T high-performance interface is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

### Functional Block Diagram

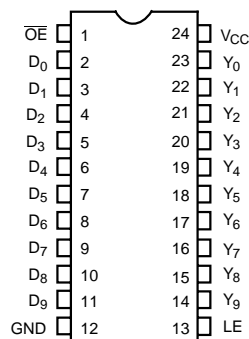


### Logic Block Diagram



### Pin Configurations

#### DIP/QSOP/SOIC Top View



**Pin Description**

Name	I/O	Description
D	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When the $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs $Y_1$ are in the high impedance (off) state.

**Function Table<sup>[1]</sup>**

Inputs			Internal Outputs		Function
$\overline{OE}$	LE	D	O	Y	
H	X	X	X	Z	High Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -65°C to +135°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage ..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... 120 mA

Power Dissipation ..... 0.5W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	All	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

**Notes:**

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, Z = High Impedance.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = –32 mA	Com'I	2.0			V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = –15 mA	Com'I	2.4	3.3		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = –12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 64 mA	Com'I		0.3	0.55	V
		V <sub>CC</sub> = Min., I <sub>OL</sub> = 32 mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = –18 mA			–0.7	–1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.5V				±1	μA
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.7V				10	μA
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V				–10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V		–60	–120	–225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> = 0V, V <sub>OUT</sub> = 4.5V				±1	μA

**Capacitance<sup>[6]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V, V_{IN} \geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V, f_1 = 0, \text{Outputs Open}^{[8]}$	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[9]</sup>	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, One Input Toggling, } \overline{OE} = \text{GND}, LE = V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
$I_C$	Total Power Supply Current <sup>[10]</sup>	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, One Bit Toggling at } f_1 = 10 \text{ MHz, } \overline{OE} = \text{GND}, LE = V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, One Bit Toggling at } f_1 = 10 \text{ MHz, } \overline{OE} = \text{GND}, LE = V_{CC}, V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.0	2.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, Ten Bits Toggling at } f_1 = 2.5 \text{ MHz, } \overline{OE} = \text{GND}, LE = V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	1.0	3.2 <sup>[11]</sup>	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, Ten Bits Toggling at } f_1 = 2.5 \text{ MHz, } \overline{OE} = \text{GND}, LE = V_{CC}, V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	4.1	13.2 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	Test Load	FCT841AT				FCT841BT		FCT841CT		Unit	Fig. No. <sup>[13]</sup>
			Military		Commercial		Commercial		Commercial			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>1</sub> to Y <sub>1</sub> (L =HIGH)	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	10.0	1.5	9.0	1.5	6.5	1.5	5.5	ns	1, 3
	Propagation Delay D <sub>1</sub> to Y <sub>1</sub> (LE=HIGH)	C <sub>L</sub> = 300 pF R <sub>L</sub> = 500Ω	1.5	15.0	1.5	13.0	1.5	13.0	1.5	13.0	ns	1, 3
t <sub>SU</sub>	Data to LE Set-Up Time	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	2.5		2.5		2.5		2.5		ns	9
t <sub>H</sub>	Data to LE Hold Time	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	3.0		2.5		2.5		2.5		ns	9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to Y <sub>1</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	13.0	1.5	12.0	1.5	8.0	1.5	6.4	ns	1, 3
	Propagation Delay LE to Y <sub>1</sub> <sup>[12]</sup>	C <sub>L</sub> = 300 pF R <sub>L</sub> = 500Ω	1.5	20.0	1.5	16.0	1.5	15.5	1.5	15.0	ns	1, 3
t <sub>W</sub>	LE Pulse Width (HIGH)	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	5.0		4.0		4.0		4.0		ns	5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to Y <sub>1</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	13.0	1.5	11.5	1.5	8.0	1.5	6.5	ns	1, 7, 8
	Output Enable Time OE to Y <sub>1</sub> <sup>[12]</sup>	C <sub>L</sub> = 300 pF R <sub>L</sub> = 500Ω	1.5	25.0	1.5	23.0	1.5	14.0	1.5	12.0	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to Y <sub>1</sub> <sup>[12]</sup>	C <sub>L</sub> = 5 pF R <sub>L</sub> = 500Ω	1.5	9.0	1.5	7.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
	Output Disable Time OE to Y <sub>1</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	10.0	1.5	8.0	1.5	7.0	1.5	6.0	ns	1, 7, 8

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT841CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT841CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
6.5	CY74FCT841BTPC	P13/P13A	24-Lead (300-Mil) Molded DIP	Commercial
9.0	CY74FCT841ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	Commercial
10.0	CY54FCT841ATDMB	D14	24-Lead (300-Mil) CerDIP	Military

**Notes:**

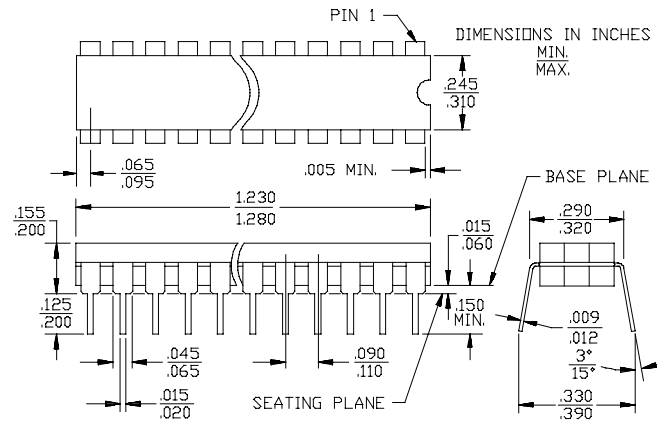
12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

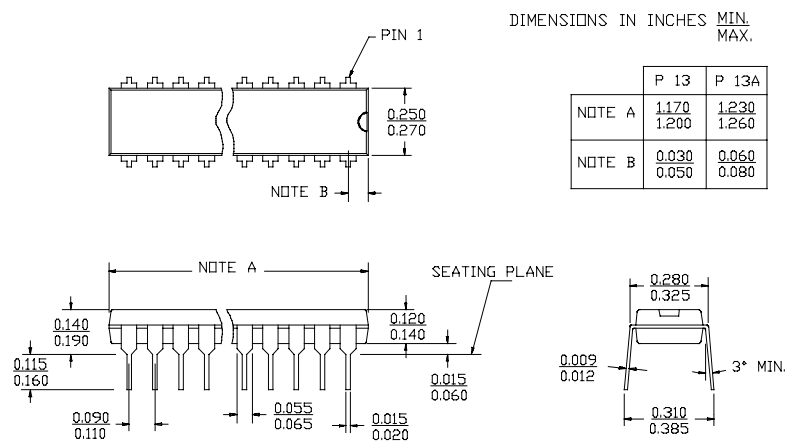
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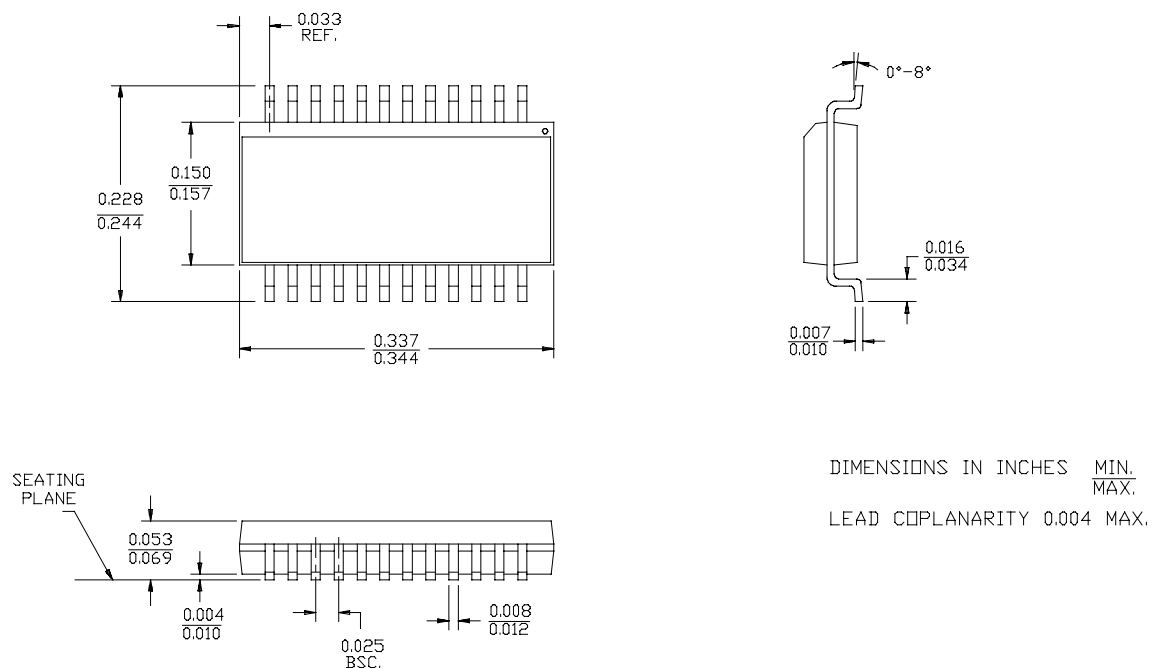
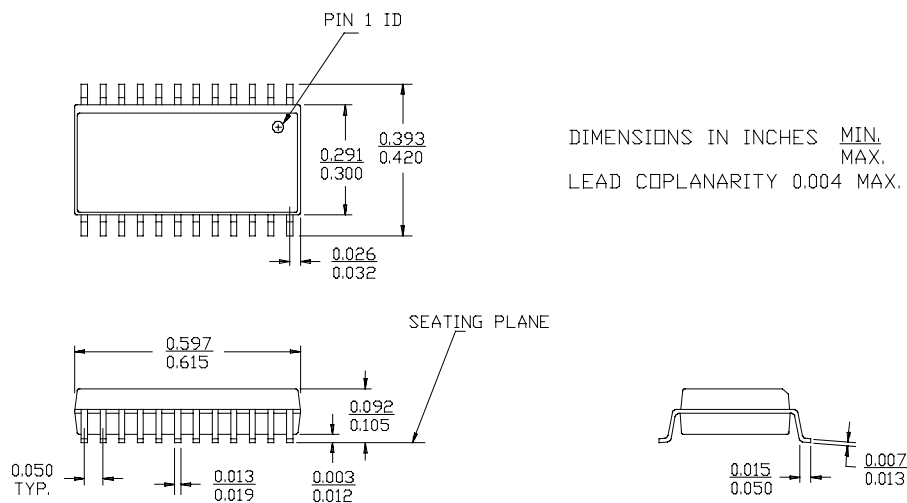
**Package Diagrams**

**24-Lead (300-Mil) CerDIP D14**  
MIL-STD-1835 D-9Config.A



**24-Lead (300-Mil) Molded DIP P13/P13A**



**Package Diagrams (continued)**
**24-Lead Quarter Size Outline Q13**

**24-Lead (300-Mil) Molded SOIC S13**


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