SN54ABT16853, SN74ABT16853
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Parity-Error Flag With Parity Generator/Checker**
- **Latch for Storage of the Parity-Error Flag**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16853 . . . WD PACKAGE
SN74ABT16853 . . . DGG OR DL PACKAGE
(TOP VIEW)

1OEB	1	56	1OEA
1LE	2	55	1CLR
1ERR	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2ERR	26	31	2PARITY
2LE	27	30	2CLR
2OEB	28	29	2OEA

description

The 'ABT16853 dual 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus, with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT16853 provide true data at the outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the ERR flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (LE) and clear (CLR) control inputs. When both OEA and OEB are low, data is transferred from the A bus to the B bus, and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

description (continued)

The SN54ABT16853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16853 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

OEB	OEA	CLR	LE	AI Σ OF H	BI† Σ OF H	A	B	PARITY	ERR‡	FUNCTION
L	H	X	X	Odd / Even	NA	NA	A	L / H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd / Even	B	NA	NA	H / L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H / L / X / X	H / H / L / L	X / X / L Odd / H Even	X	Z	Z	Z	NC / H / H / L	Isolation§ (parity check)
L	L	X	X	Odd / Even	NA	NA	A	H / L	NA	A data to B bus and generate inverted parity

(Table header spans: INPUTS = OEB, OEA, CLR, LE, AI Σ OF H, BI† Σ OF H; OUTPUT AND I/O = A, B, PARITY, ERR‡)

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume ERR was previously high.
§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

logic diagram (each transceiver) (positive logic)

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	$\overline{LE}$	POINT P	$\overline{ERR}_{n-1}$[†]		
L	L	L	X	L	Pass
		H		H	
H	L	L	X	L	Sample
		X	L	L	
		H	H	H	
L	H	X	X	H	Clear
H	H	X	L	L	Store
			H	H	

† State of $\overline{ERR}$ before changes at $\overline{CLR}$, $\overline{LE}$, or point P

error-flag waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16853 . . . . 96 mA
                                                                SN74ABT16853 . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 81°C/W
                                                                      DL package . . . . 74°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
              2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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recommended operating conditions (see Note 3)

			SN54ABT16853		SN74ABT16853		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	$\overline{ERR}$		5.5		5.5	V
I_{OH}	High-level output current	Except $\overline{ERR}$		−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT16853		SN74ABT16853		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	All outputs except $\overline{ERR}$	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5	3		2.5				V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3	3.4		3		3		
		V_{CC} = 4.5 V	I_{OH} = −24 mA				2				
			I_{OH} = −32 mA	2*	2.7				2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 24 mA		0.25	0.55		0.55			V
			I_{OL} = 64 mA		0.3	0.55*				0.55	
V_{hys}					100						mV
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			20		20		20	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \leq$ 4.5 V			±100		±100		±100	µA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V			50		50		50	µA
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports					±100		±100		±100	
I_{IL}	A or B ports	V_{CC} = 0,	V_I = GND			−50		−50		−50	µA
$I_O‡$		V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
$I_{OZH}§$		V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
$I_{OZL}§$		V_{CC} = 5.5 V,	V_O = 0.5 V			−50		−50		−50	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1.5	2		2		2	mA
			Outputs low		32	40		40		40	
			Outputs disabled		1	2		2		2	
$\Delta I_{CC}¶$		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT16853		SN74ABT16853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LE}$ high or low	8.5		8.5		8.5		ns
		$\overline{CLR}$ low	4		4		4		
t_{su}	Setup time	A, B, and PARITY before $\overline{LE}$↓	10		10		10		ns
		$\overline{CLR}$ before $\overline{LE}$↓	0		0		0		
t_h	Hold time	A, B, and PARITY after $\overline{LE}$↓	0		0		0		ns
		$\overline{CLR}$ after $\overline{LE}$↓	0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

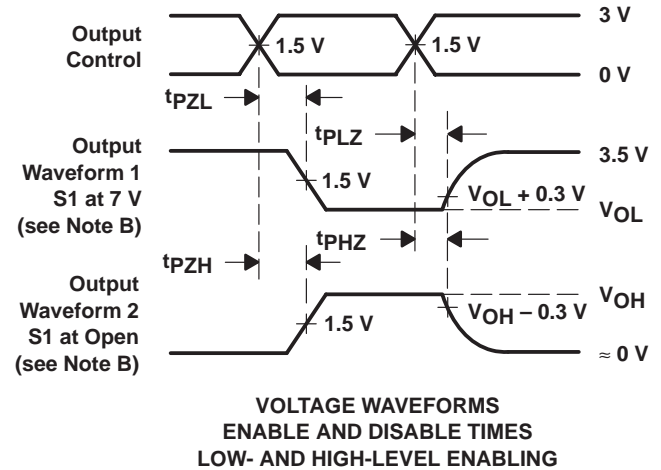| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16853		SN74ABT16853		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PLH}	A or $\overline{OE}$	PARITY	2	4.6	5.9	2	7.3	2	7.1	ns
t_{PHL}			2	4.8	6.2	2	7.6	2	7.2	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	2	3.7	5.1	2	5.9	2	5.7	ns
t_{PZH}	$\overline{OE}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{OE}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PZH}	$\overline{OE}$	PARITY	2	3.6	5	2	5.8	2	5.7	ns
t_{PZL}			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
t_{PHZ}	$\overline{OE}$	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t_{PLZ}			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
t_{PLH}	$\overline{LE}$	$\overline{ERR}$	2	3.5	4.2	2	5	2	4.8	ns
t_{PHL}			2	3.4	4.4	2	5.2	2	4.9	
t_{PLH}	A, B, or PARITY	$\overline{ERR}$	2	4.5	6.3	2	7.5	2	7.2	ns
t_{PHL}			2	4.8	6.3	2	7.7	2	7.4	

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PARAMETER MEASUREMENT INFORMATION
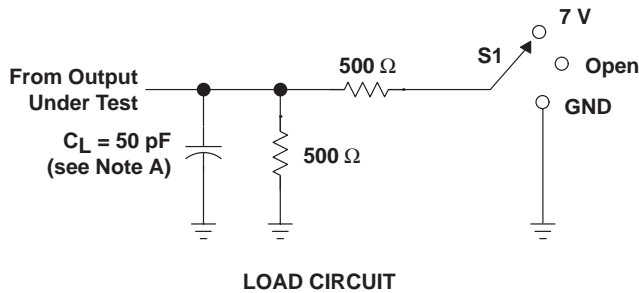
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

$\overline{ERR}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
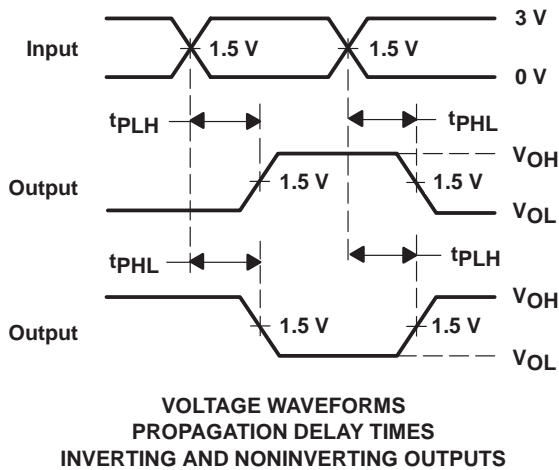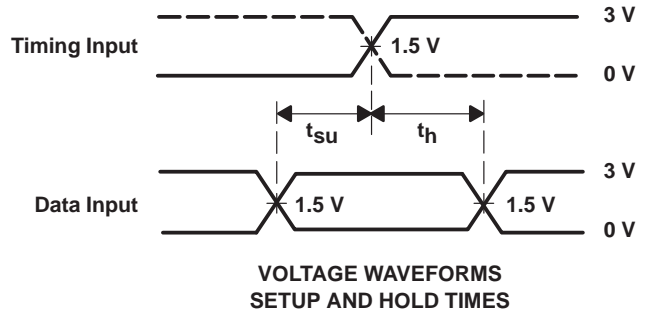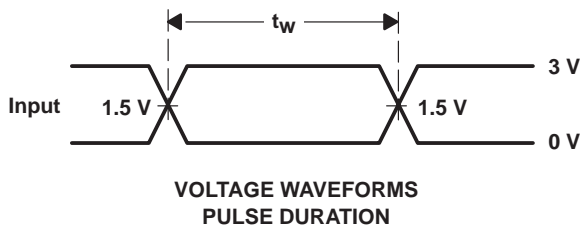
NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
  D. The outputs are measured one at a time with one transition per measurement.
  E. t_{PHL} is measured at 1.5 V.
  F. t_{PLH} is measured at V_{OL} + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ABT16853DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16853DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16853DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16853DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16853DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16853DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
                      Post Office Box 655303 Dallas, Texas 75265

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