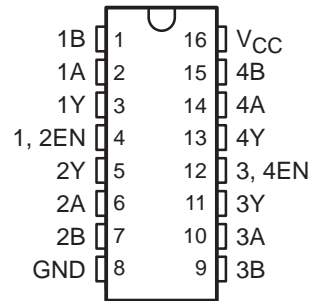


# SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed to Operate Up To 20 Mbaud
- –7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k $\Omega$  Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement  
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

D OR N PACKAGE  
(TOP VIEW)



## description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of  $\pm 300$  mV over a common-mode input voltage range of  $\pm 7$  V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each receiver)

DIFFERENTIAL INPUTS A–B	EN	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	H
$-0.3$ V $< V_{ID} < 0.3$ V	H	?
$V_{ID} \leq -0.3$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,  
? = indeterminate, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

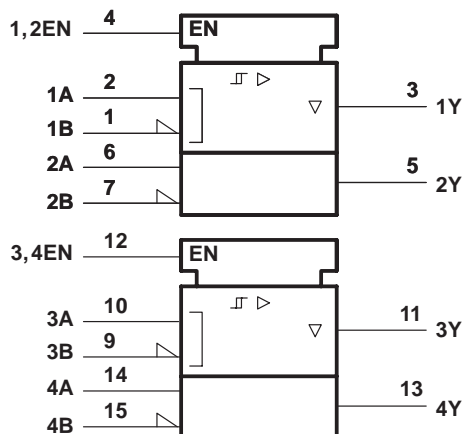
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# SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

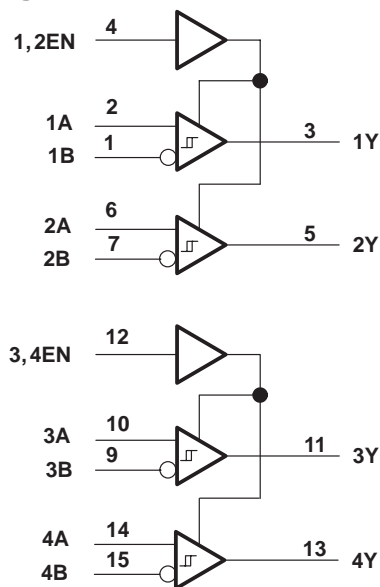
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## logic symbol†

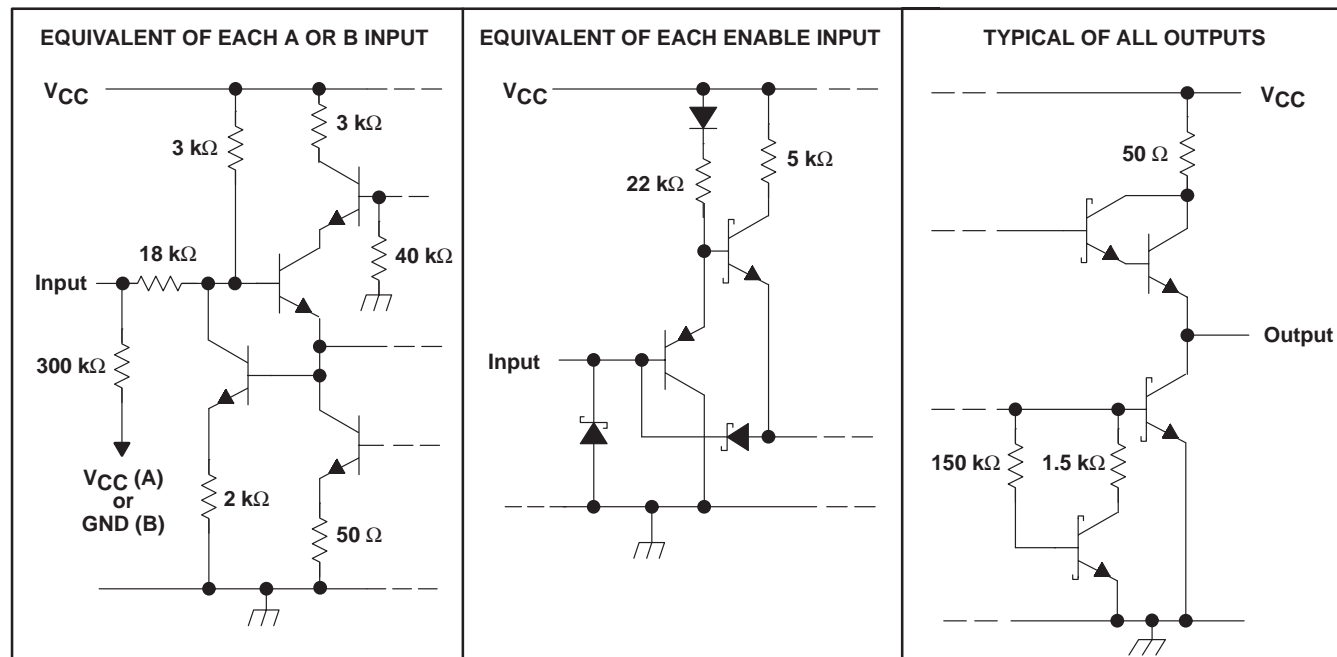


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram



## schematics of inputs and outputs



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$ (A or B inputs)	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 15$ V
Enable input voltage, $V_I$	7 V
Low-level output current, $I_{OL}$	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$			$\pm 7$	V
Differential input voltage, $V_{ID}$			$\pm 12$	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
High-level output current, $I_{OH}$			– 400	$\mu\text{A}$
Low-level output current, $I_{OL}$			16	mA
Operating free-air temperature, $T_A$	0		70	°C

# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$ Positive-going input threshold voltage				300	mV
$V_{IT-}$ Negative-going input threshold voltage		-300‡			mV
$V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			120		mV
$V_{IK}$ Enable-input clamp voltage	$I_I = -18$ mA			-1.5	V
$V_{OH}$ High-level output voltage	$V_{ID} = 300$ mV, $I_{OH} = -400$ $\mu$ A	2.7	3.6		V
$V_{OL}$ Low-level output voltage	$V_{ID} = -300$ mV			0.45	V
				0.5	
$I_{OZ}$ High-impedance-state output current	$V_{IL} = 0.8$ V, $V_{ID} = -3$ V, $V_O = 2.7$ V			20	$\mu$ A
	$V_{IL} = 0.8$ V, $V_{IO} = 3$ V, $V_O = 0.5$ V			-20	
$I_I$ Line input current	Other input at 0 V, See Note 3	$V_I = 15$ V	0.7	1.2	mA
		$V_I = -15$ V	-1	-1.7	
$I_{IH}$ High-level enable-input current		$V_{IH} = 2.7$ V		20	$\mu$ A
		$V_{IH} = 5.25$ V		100	
$I_{IL}$ Low-level enable-input current	$V_{IL} = 0.4$ V			-100	$\mu$ A
Input resistance		12	18		k $\Omega$
$I_{OS}$ Short-circuit output current§	$V_{ID} = 3$ V, $V_O = 0$	-15	-78	-130	mA
$I_{CC}$ Supply current	Outputs disabled		22	35	mA

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

### switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$V_{ID} = 0$ V to 3 V, $C_L = 15$ pF, See Figure 2		15	22	ns
$t_{PHL}$ Propagation delay time, high- to low-level output			15	22	
$t_{PZH}$ Output enable time to high level	$C_L = 15$ pF, See Figure 3		13	25	ns
$t_{PZL}$ Output enable time to low level			11	25	
$t_{PHZ}$ Output disable time from high level	$C_L = 15$ pF, See Figure 3		13	25	ns
$t_{PLZ}$ Output disable time from low level			15	22	

## PARAMETER MEASUREMENT INFORMATION

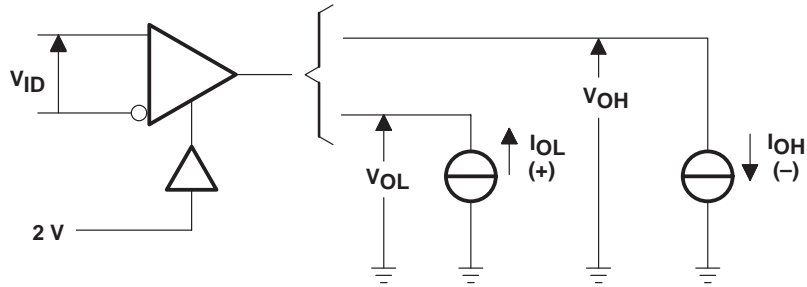
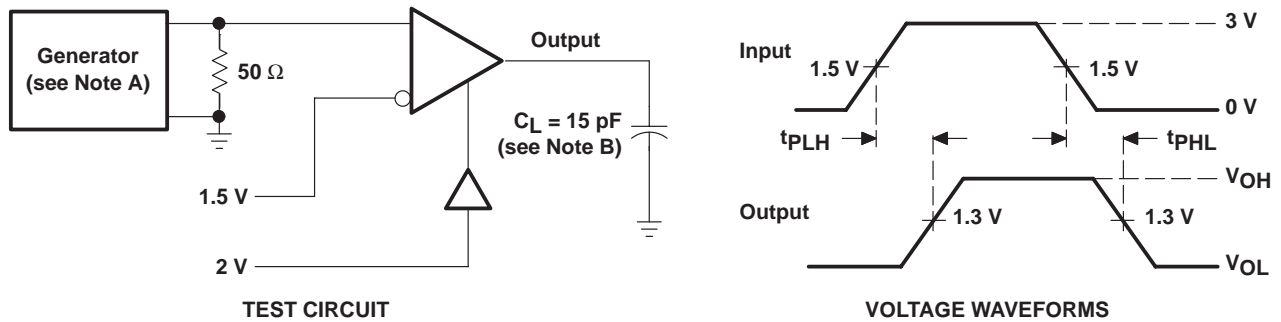


Figure 1.  $V_{OH}$  and  $V_{OL}$  Test Circuit



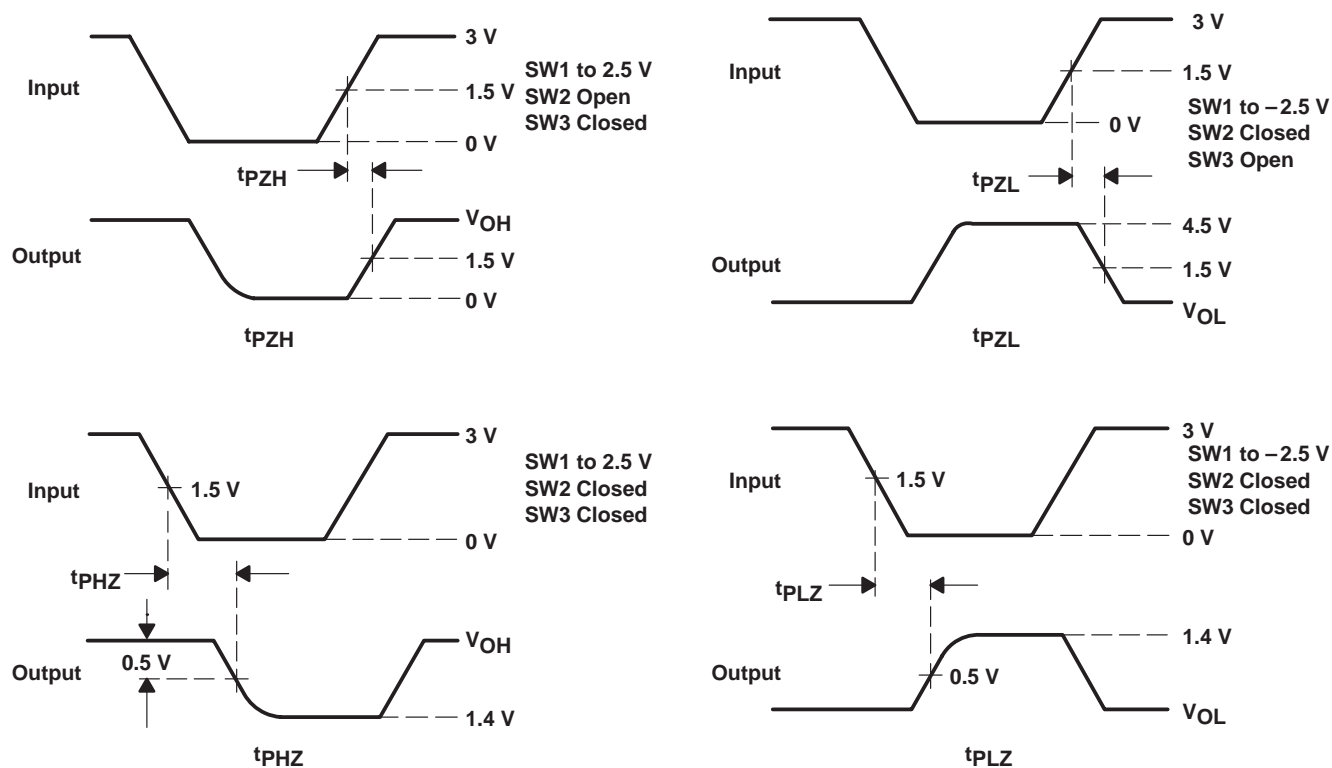
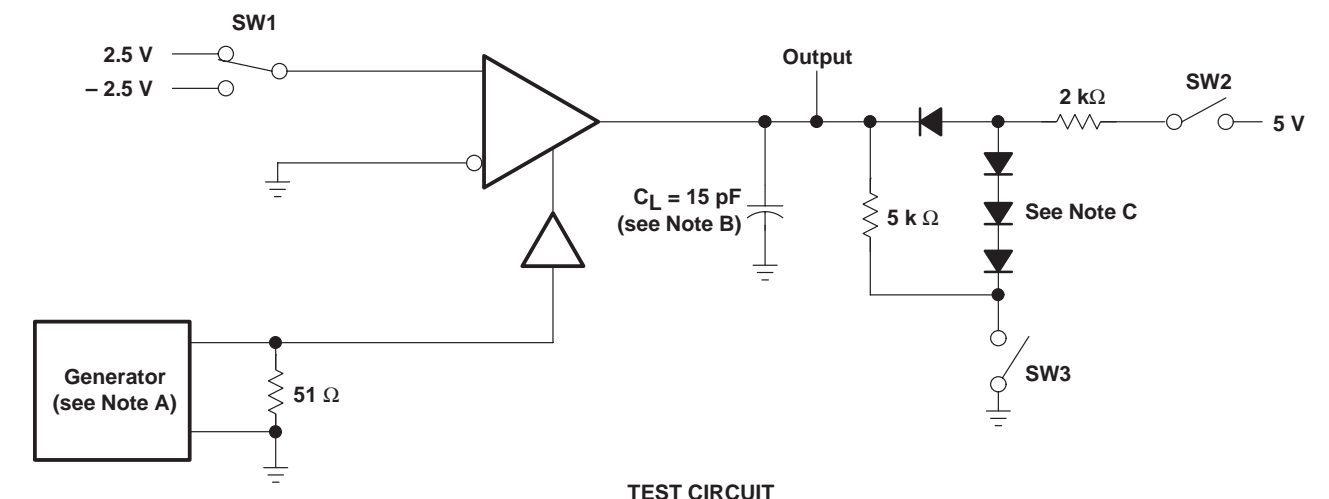
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle  $\leq 50\%$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle  $\leq 50\%$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

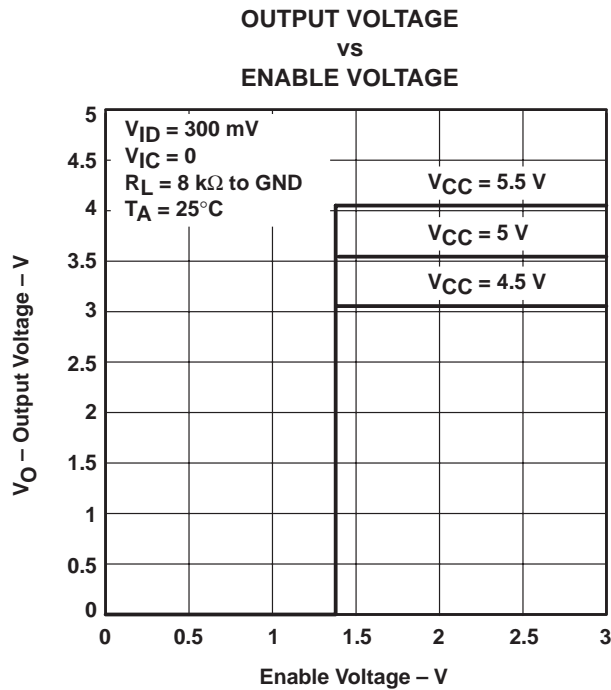


Figure 4

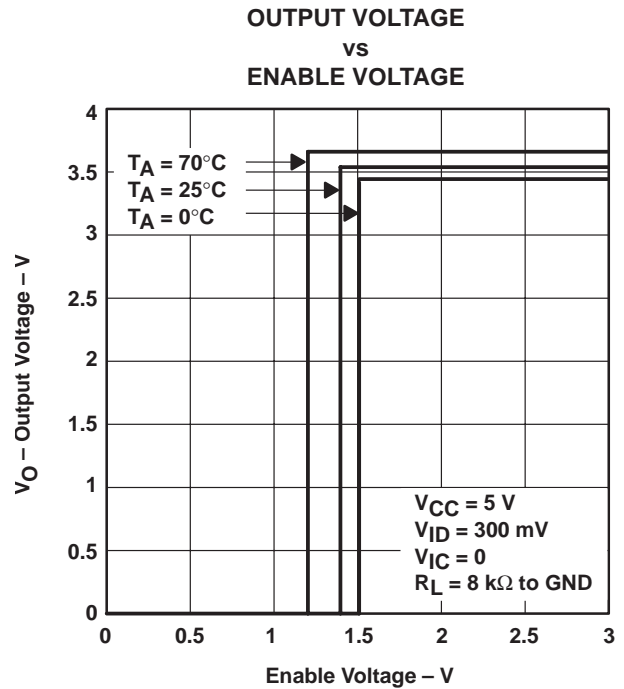


Figure 5

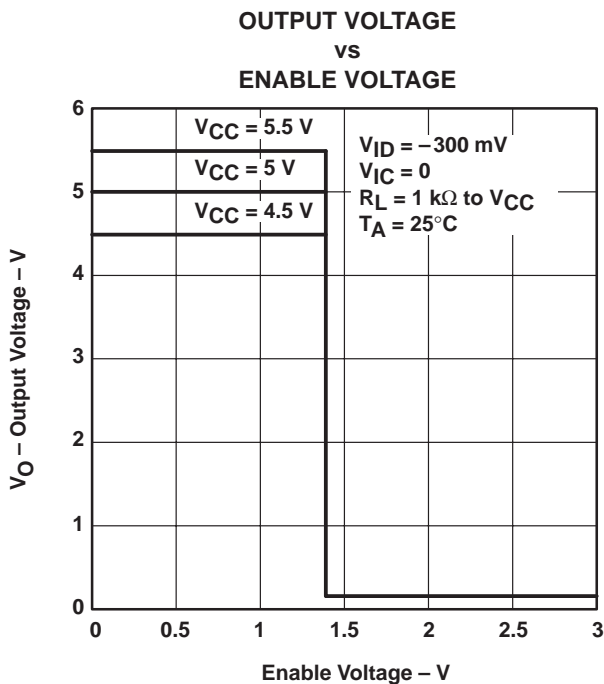


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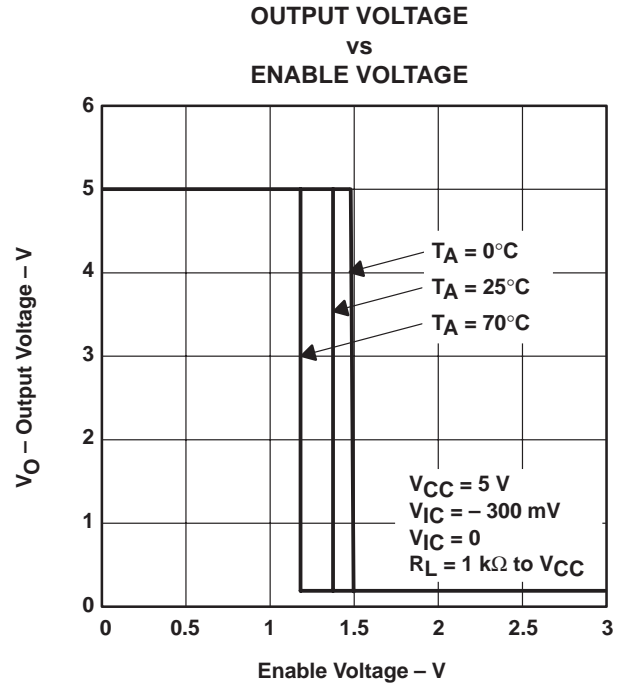


Figure 7

# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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### TYPICAL CHARACTERISTICS

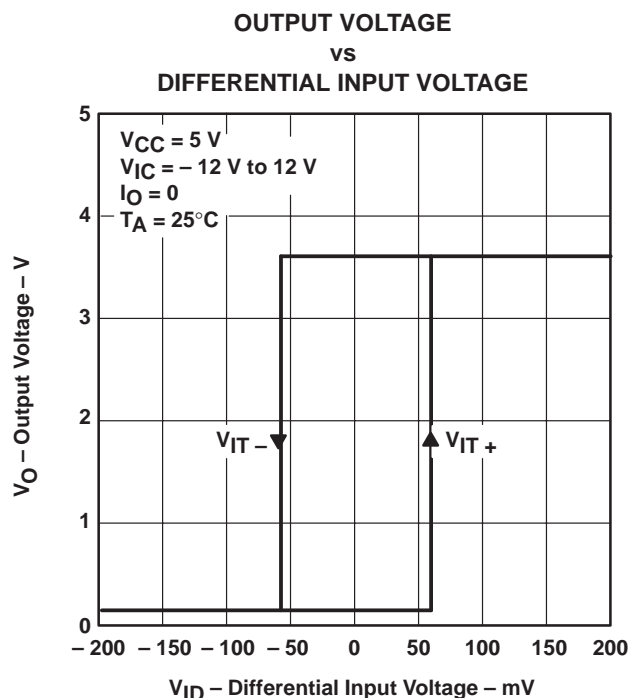


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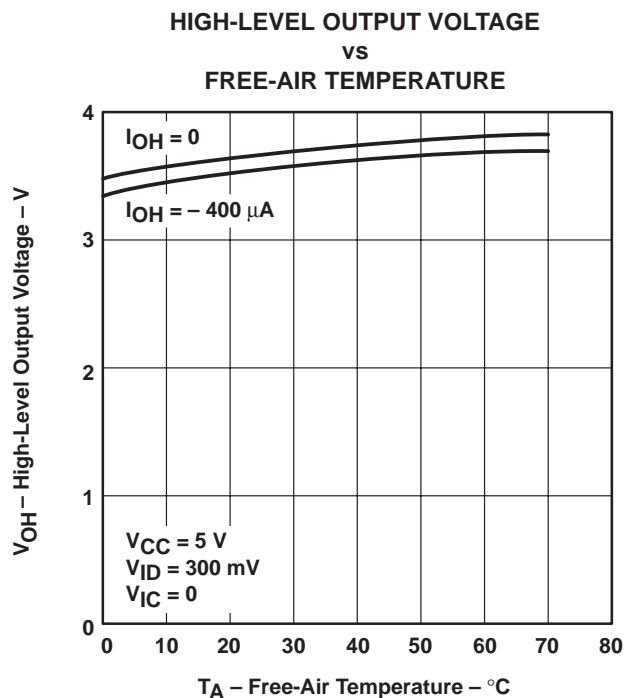


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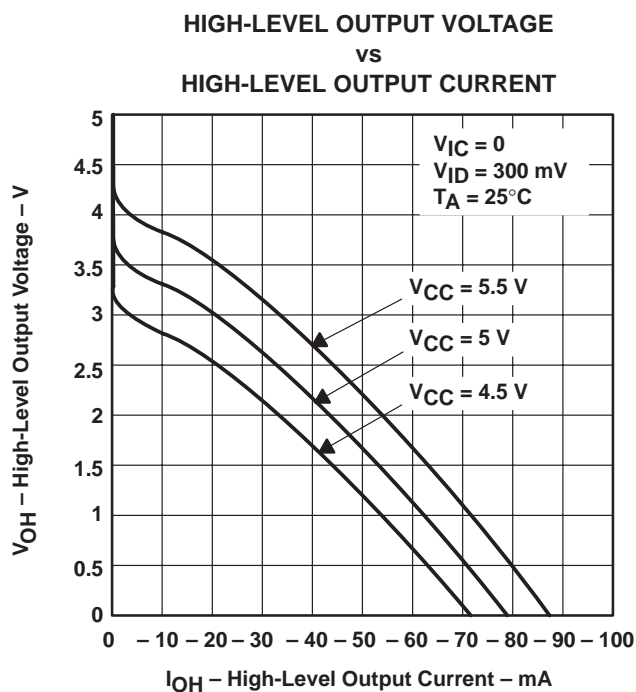


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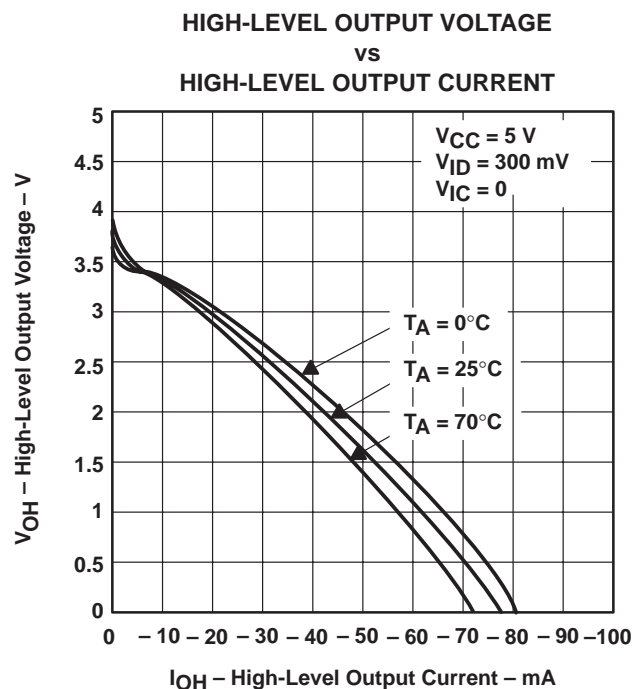


Figure 11



## TYPICAL CHARACTERISTICS

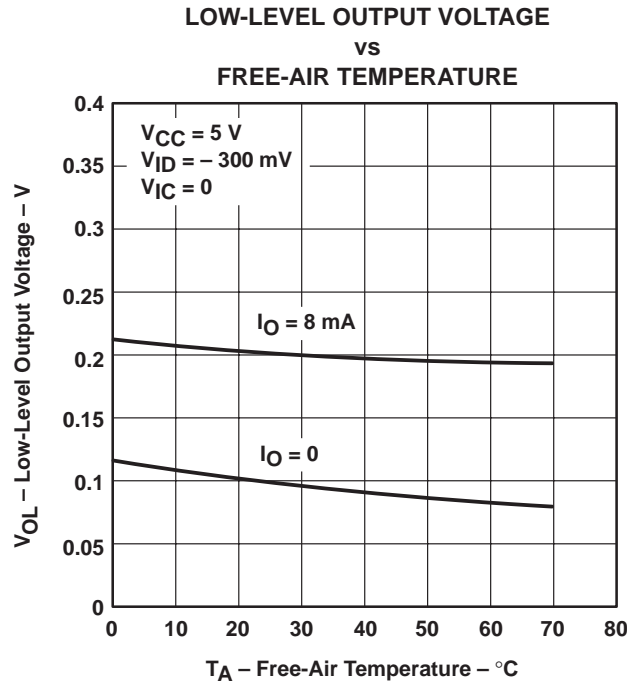


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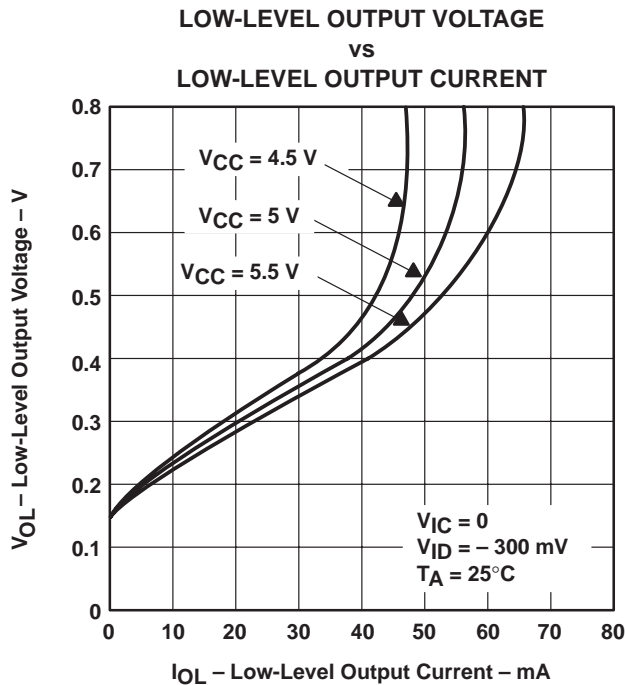


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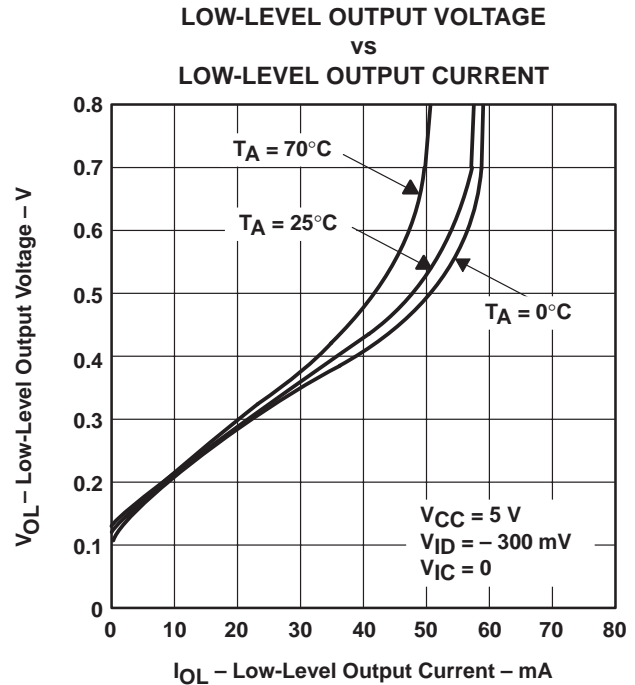


Figure 14

# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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### TYPICAL CHARACTERISTICS

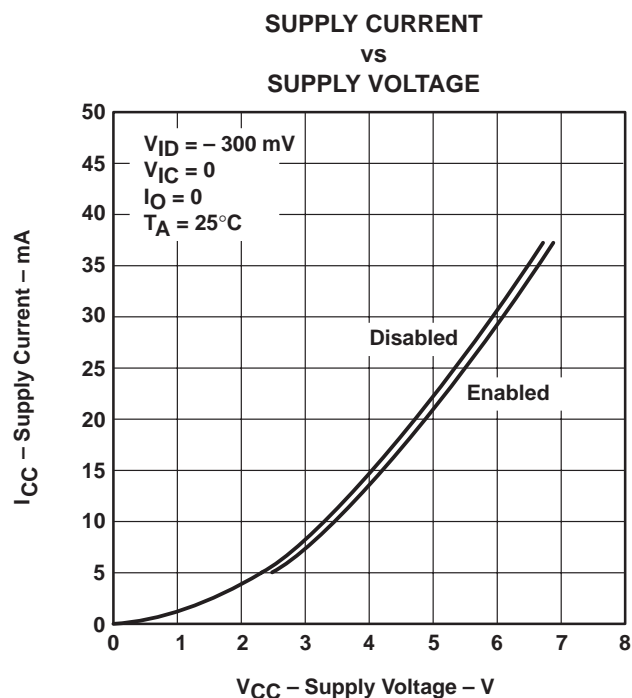


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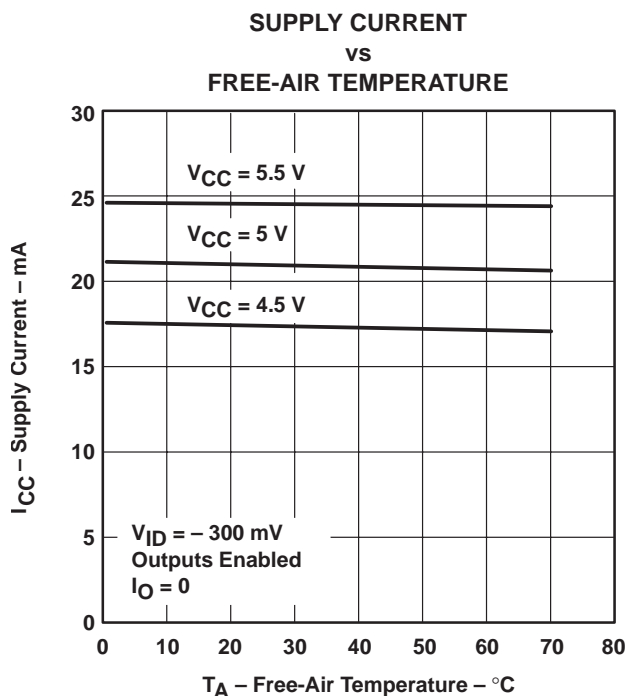


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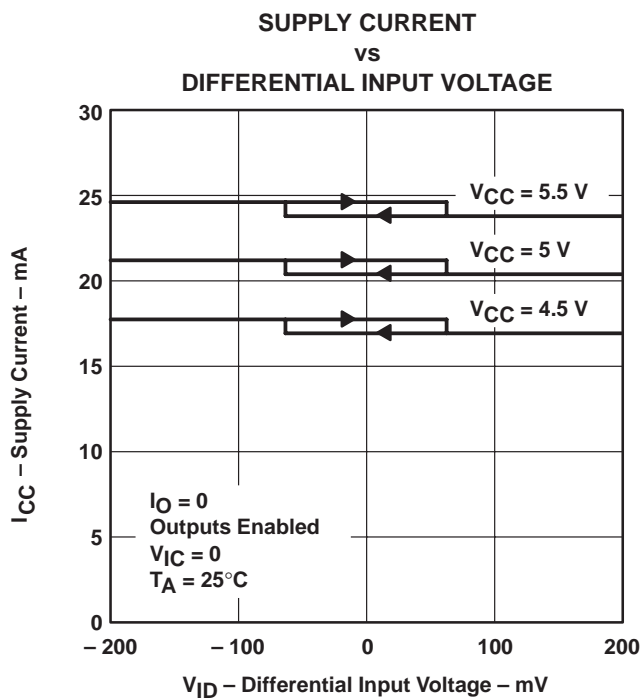


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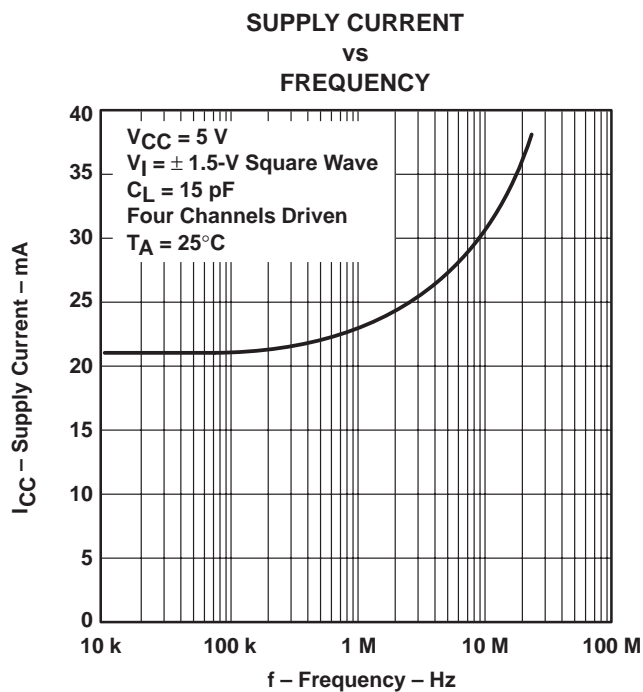


Figure 18

TYPICAL CHARACTERISTICS

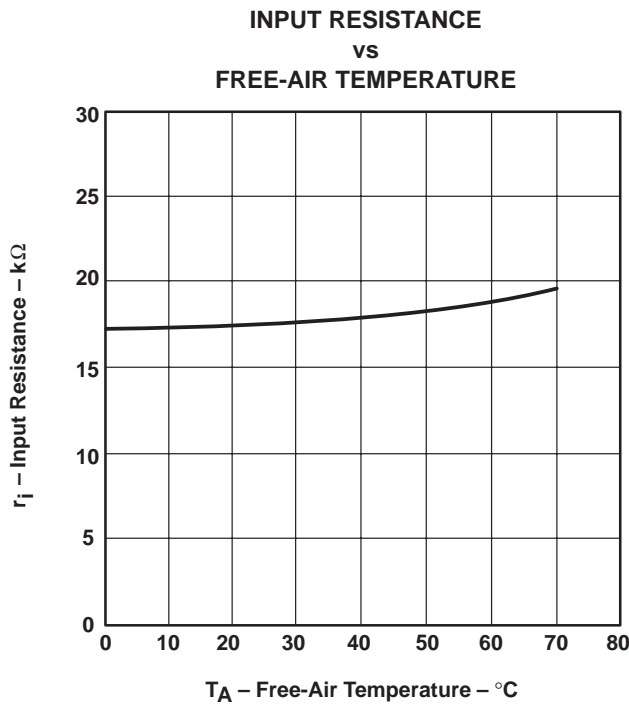


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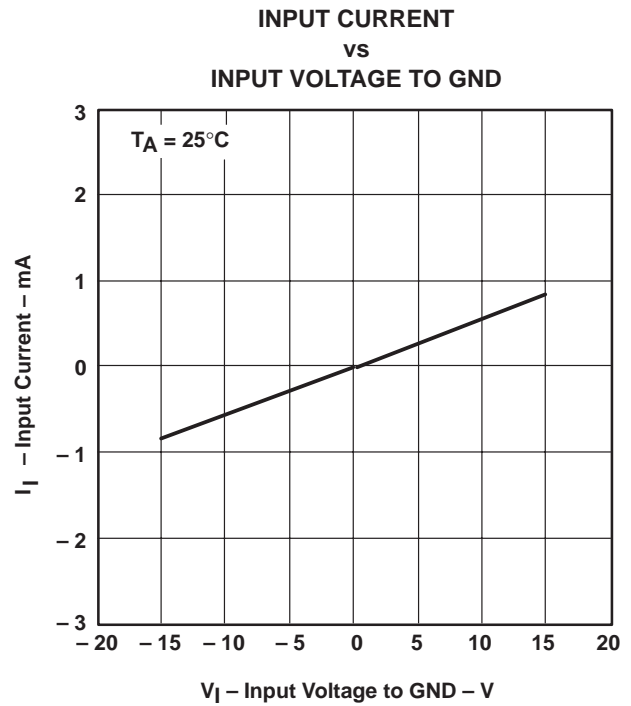


Figure 20

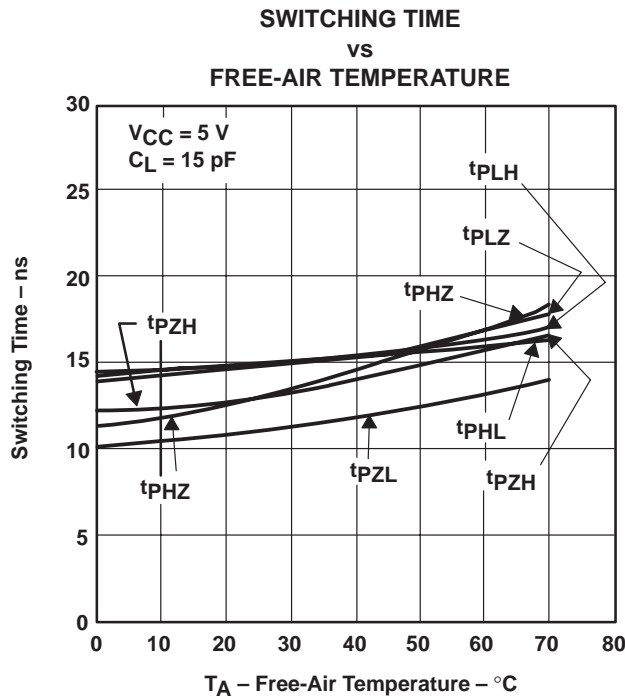


Figure 21

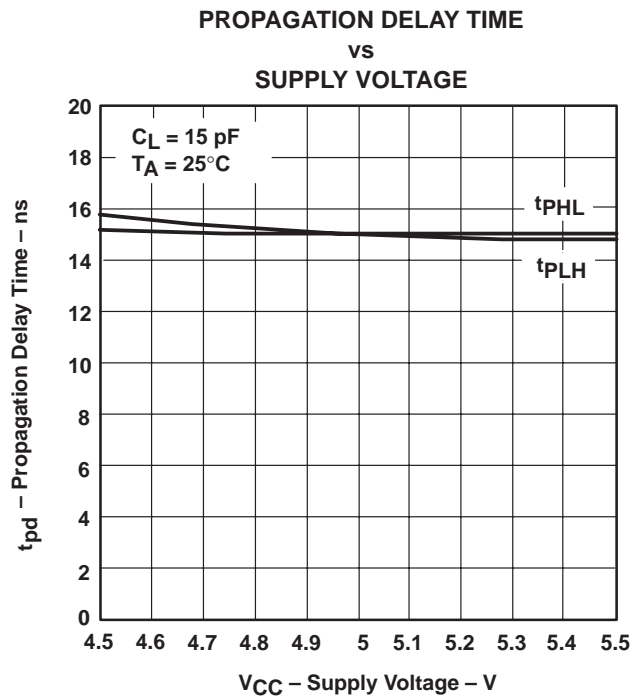


Figure 22

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