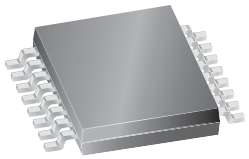
Relay Driver with 5 V Regulator for Automotive Applications

Features and Benefits

- Three independent low-side DMOS output drivers
- Short-circuit protection of drivers
- Eliminates need for flyback diodes on relays
- Thermal shutdown
- Separate precision 5 V regulator (2%)
- Current clamp on 5 V regulator
- 16-pin TSSOP package with exposed thermal pad
- Programmable reset (NPOR) delay time
- Programmable watchdog
- Automotive voltage and temperature ranges
- Active clamps for automotive load dump specifications
- Lead (Pb) free

Package: 16 pin TSSOP (suffix LP) with exposed pad



Approximate Scale 

Description

Large numbers of relay-based applications require the use of a microprocessor which implements complex system control. In these systems, there is the need for microprocessor logic supply voltage, power-on reset circuitry, and watchdog capabilities. The Allegro® A2550 combines the functions of voltage regulator, watchdog, and reset, as well as three low-side DMOS relay driver outputs. Primarily targeted at automotive applications, this IC is designed to provide robust performance over extended voltage and temperature ranges.

Three low-side DMOS drivers can drive inductive loads, such as relay coils. Each driver integrates rugged voltage clamps which survive automotive load dump pulses up to 48 V. The 40 V rating on VBB also ensures adequate survival in harsh automotive environments.

A 5 V linear regulator provides 40 mA of output current, with a tolerance of 2% over the operating temperature range. To enhance the usefulness of the IC in automotive applications, the 5 V regulator output, as well as the three low-side driver outputs are protected against overcurrent conditions.

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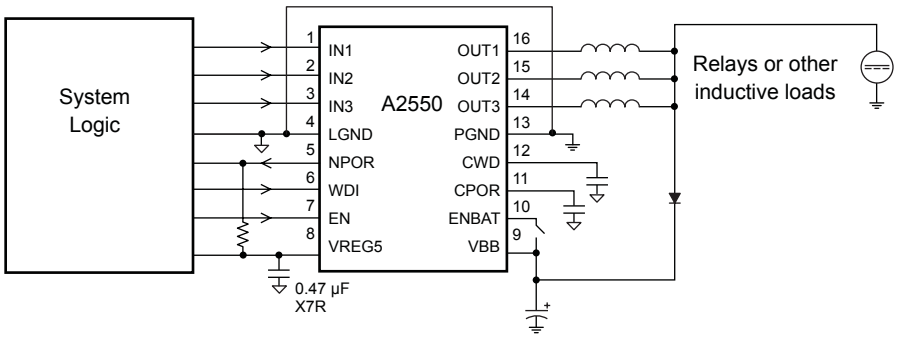
Typical Application



Description (continued)

The A2550 also includes power-on reset circuitry (NPOR) as well as an integrated watchdog circuit. Combined, they service the monitoring and reset requirements of a system microprocessor.

The A2550 is supplied in a 16-pin TSSOP package with exposed thermal pad (package LP). The package is lead (Pb) free, with 100% matte tin leadframe plating.

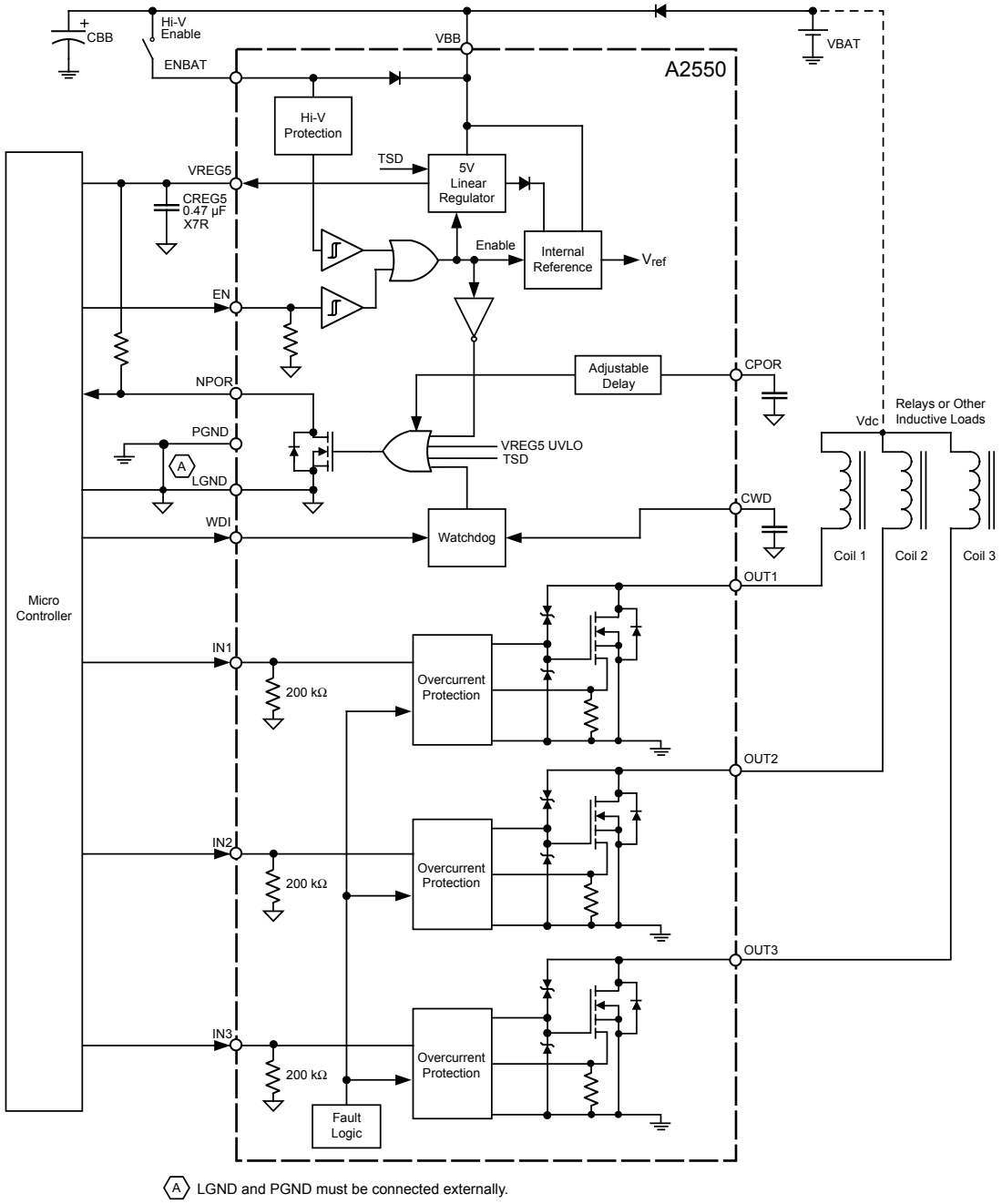
Selection Guide

Part Number	Packing
A2550KLP-T	96 pieces / tube
A2550KLPTR-T	13-in. reel, 4000 pieces / reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{BB}		–0.3 to 60	V
High Voltage Enable	V_{ENBAT}		–0.3 to 60	V
Output Driver	V_{OUT}	Continuous rating; outputs off	–1.4 to 48	V
Output Load Clamp	$V_{OUT(CL)}$	Transient rating	60	V
Maximum Energy at Outputs	E_{OUT}	Single Pulse, T_J(initial) = 125°C	100	mJ
Peak Power Dissipation at Outputs	P_{PK}	Single pulse, T_J(initial) = 125°C, Δt = 1 ms; see figure 2 for different durations and T_J(initial)	1.7	W
All other pins			–0.3 to 7	V
ESD Rating – Human Body Model		AEC-Q100-002; all pins	2.5	kV
ESD Rating – Charged Device Model		AEC-Q100-011; all pins	1050	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	$T_{J\ (max)}$		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Functional Block Diagram



A LGND and PGND must be connected externally.

Component Selection Table

Name	Suitable Characteristics	Representative Device
CBB	33 µF, 63 V electrolytic	United Chemi-Con EGHA630E–560MJC5S
CREG5	0.47 µF, 25 V, X7R ceramic	
CWD, CPOR	0.22 µF, 16 V, X7R ceramic	

ELECTRICAL CHARACTERISTICS, –40°C ≤ T_J ≤ 150°C, V_{BB} within operating limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply						
VBB Operating Voltage[1]	V_{BB}		7	–	40	V
VBB Supply Current	I_{BBQ}	All OUTx Off; EN = 5 V, V_{BB} = ENBAT = 14 V	–	–	4	mA
	I_{BB}	All OUTx On; EN = 5 V, V_{BB} = ENBAT= 14 V	–	–	5	mA
	I_{BBS}	Sleep mode, EN = ENBAT = 0	–	–	10	µA
Logic Inputs						
ENBAT Input Voltage[2]	V_{ENBAT}	HIGH input level	3.5	–	V_{BB}	V
		LOW input level	0	–	1.5	V
EN, WDI, and INx Input Voltage	V_{IH}	HIGH input level	3.5	–	5.5	V
	V_{IL}	LOW input level	0	–	1.5	V
ENBAT, EN, WDI, INx Input Voltage Hysteresis	V_{Ihys}		200	–	–	mV
ENBAT Input Current[2,3]	I_{ENBAT}	HIGH input level, V_{BB} = $V_{BB(max)}$	–	–	400	µA
		HIGH input level, V_{BB} = 14 V	–	–	70	µA
		LOW input level	–50	–	10	µA
EN Input Current[2]	I_{EN}	HIGH input level	–	–	50	µA
		LOW input level	–50	–	10	µA
WDI Input Current[2]	I_{WDI}	HIGH input level	–	–	50	µA
		LOW input level	–10	–	10	µA
INx Input Current[2]	I_{INx}	HIGH input level	–	–	50	µA
		LOW input level	–10	–	10	µA
Drivers						
Propagation Delays	$t_{p(ON)}$	INx change to unloaded output change	–	1	2	µs
	$t_{p(OFF)}$	INx change to unloaded output change	–	0.5	1	µs
Driver On-Resistance	$R_{DS(on)}$	I_{OUTx} = 250 mA, V_{BB} = 14 V	–	–	5	Ω
		I_{OUTx} = 250 mA, V_{BB} = 9 V	–	–	5.5	Ω
		I_{OUTx} = 250 mA, V_{BB} = 7 V	–	–	6	Ω
Driver Leakage Current	I_{DSS}	V_{OUTx} = 40 V	–	–	10	µA
Diode Forward Voltage	V_F	I_{OUTx} = –250 mA	–	–1.3	–1.4	V
Output Clamp Voltage	V_{CL}	I_{OUTx} = 100 µA	50	–	60	V
Low-Side Driver Overcurrent (O.C.) Threshold	$I_{OUT(OC)}$		275	–	500	mA
Blanking Time Before Overcurrent Detect	t_{BLANK}	I_{OUT} = 500 mA	2	–	20	µs
Regulator						
Voltage Regulator Output Voltage	V_{REG5}	C_{REG5} ≥ 0.47 µF (X7R Ceramic, ESR ≤ 0. 5Ω), 1 mA ≤ I_{REG5} ≤ 40 mA	4.9	5.0	5.1	V
Pass Transistor On-Resistance[1]	R_{REG5}	I_{REG5} = 40 mA	–	–	55	Ω
Line Regulation Voltage	V_{LNR}	I_{REG5} = 1 mA	–	–	20	mV
Load Regulation Voltage	V_{LDR}	1 mA ≤ I_{REG5} ≤ 40 mA, V_{BB} = 7 V	–	–	100	mV
		1 mA ≤ I_{REG5} ≤ 40 mA, V_{BB} ≥ 9 V	–	–	40	mV
Current Limit Level[4]	$I_{REG5Lim}$	V_{REG5} = 4.63 V, V_{BB} = 7 V	40	–	150	mA
		V_{REG5} = 4.63 V, V_{BB} ≥ 9 V	65	–	200	mA
		V_{REG5} = 0 V	65	–	200	mA
Under Voltage Lockout Threshold	V_{UVREG5}	V_{REG5} falling	4.25	4.38	4.63	V
		V_{REG5} rising	4.36	4.50	4.75	V
Under Voltage Lockout Hysteresis	$V_{UVREG5hys}$		–	0.12	–	V

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ELECTRICAL CHARACTERISTICS, continued –40°C ≤ T_J ≤ 150°C, V_{BB} within operating limits, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Watchdog and Power-On Reset						
NPOR Active Voltage	V_{NPOR}	I_{NPOR} = 1 mA; V_{REG5} = 1.5 V; 1.5 V ≤ V_{BB} ≤ 40 V	–	–	400	mV
NPOR Inactive Leakage Current	$I_{NPOR(Off)}$	V_{NPOR} = 5 V	–	–	10	µA
CWD and CPOR Trip Voltage	$V_{TRIP(H)}$	$V_{TRIP(H)} = V_{REF}$	–	1.2	–	V
	$V_{TRIP(L)}$		–	0.2	–	V
CPOR Charge Current	I_{POR}		2.5	5	7.5	µA
Power-On Reset Cycle Time[5]	t_{POR}	C_{POR} = 0.22 µF	–	44	–	ms
CWD Charge Current	I_{CWD}	Charging	2.5	5	7.5	µA
		Discharging	–	70	–	µA
Thermal Protection						
Thermal Shut Down Threshold	T_{TSD}		–	175	–	°C
Thermal Shut Down Hysteresis	T_{TSDhys}		–	15	–	°C

[1]See Applications Information section for operation with V_{BB} < 7 V. For V_{BB} > 24 V, thermal constraints limit regulator current.
[2]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[3]When V_{ENBAT} exceeds V_{BB} it is clamped with a diode. (V_{ENBAT} – V_{BB}) ≤ 1.2 V at 40 mA.
[4]Defined as the maximum current level allowed during excessive load condition.
[5]See Applications Information section for calculations. Values guaranteed by design, and depend on capacitor tolerances.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Thermal Resistance, Junction to Pad	$R_{\theta JP}$		2	ºC/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	34	ºC/W
		2-layer PCB with 2 in.^{2} copper both sides, connected by thermal vias	44	ºC/W
Maximum Allowable Power Dissipation	P_D	$R_{\theta JA}$ = 44 ºC/W (estimated), 2-layer PCB with 2.0 in.^{2} of 2 oz. copper, T_A = 125°C	0.57	W
		$R_{\theta JA}$ = 44 ºC/W (estimated), 2-layer PCB with 2.0 in.^{2} of 2 oz. copper, T_A = 85°C	1.48	W

*Additional thermal data available on the Allegro Web site.

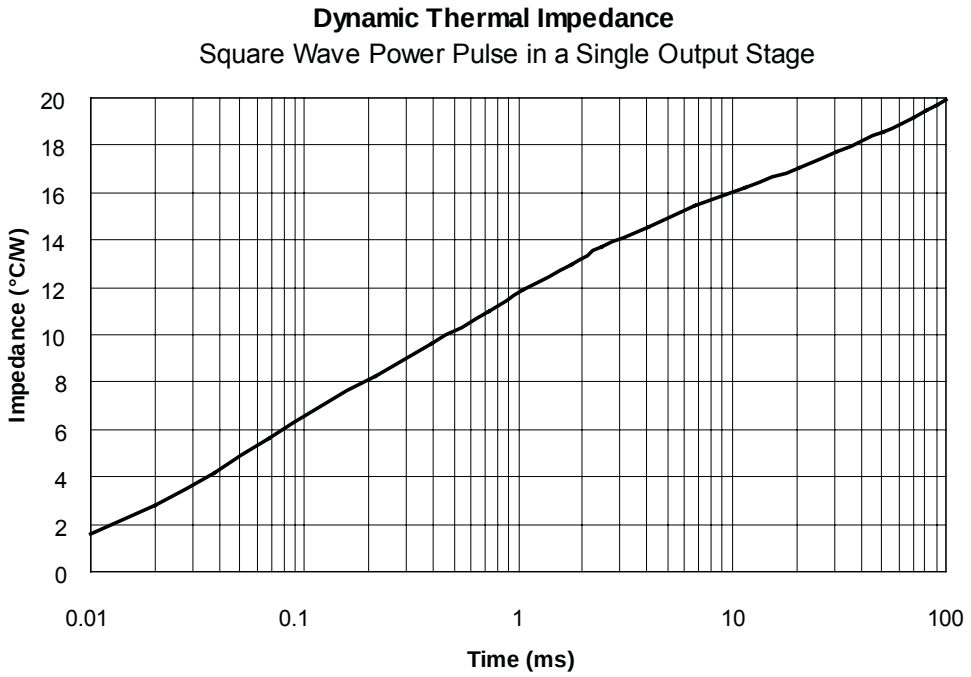


Figure 1. Dynamic thermal impedance of an individual output stage during active clamp of an inductive load

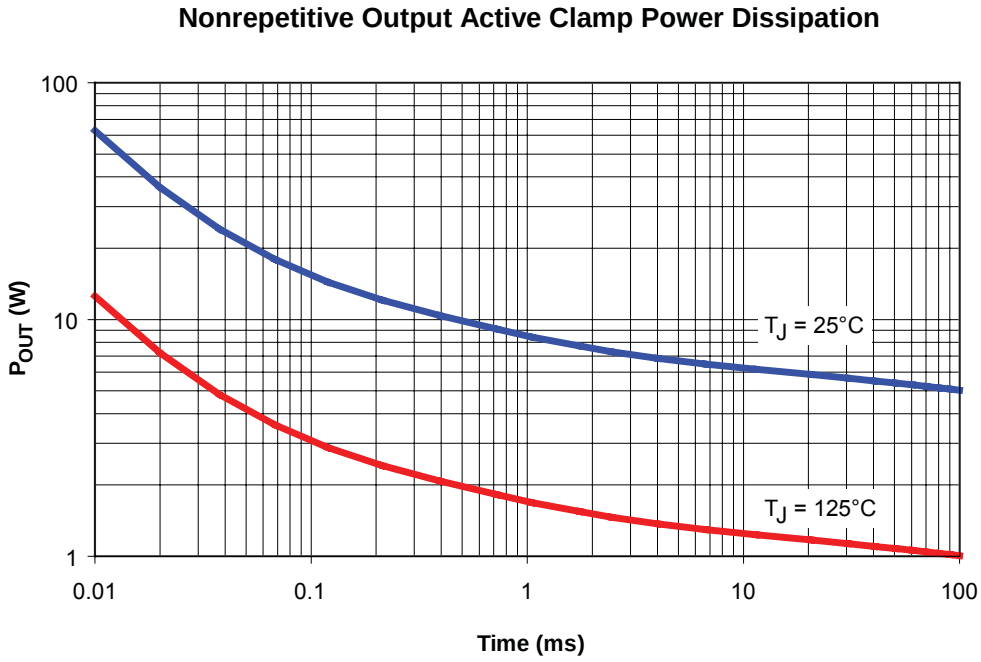
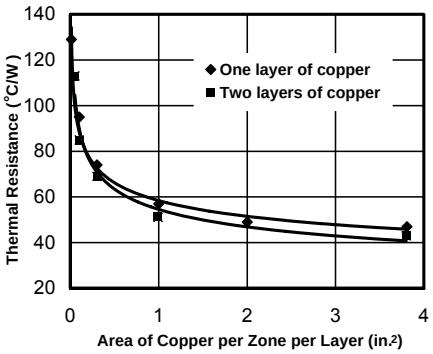


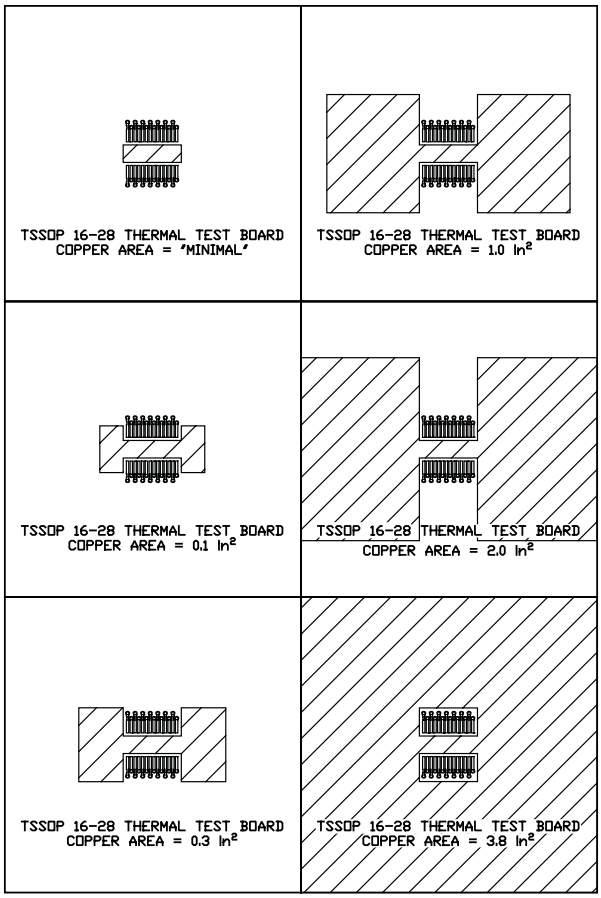
Figure 2. Peak power dissipation curves for nonrepetitive clamped outputs. Output voltage is clamped during turn-off of inductive loads while current decays.

Thermal Resistance with 2 oz. Copper

(Additional thermal information is available on the Allegro Web site)

Thermal Resistance ($R_{\theta JA}$) vs. Copper Area on PWB





The exposed copper area must be soldered to the exposed thermal pad of the device. For the board with two layers of copper, the copper areas on both sides of the substrate are identical. The two layers are thermally connected by vias placed on each ground lead. See JEDEC Standard JESD 51-5 for recommended via geometry.

Functional Description

Pin Descriptions

EN Enable pin; logical OR with ENBAT. This logic-level input enables the A2550. If there are no faults, the regulator is live and outputs can be switched. When both the EN and ENBAT pins are held low, the A2550 enters Sleep mode.

ENBAT Enable pin; logical OR with EN. Same as EN, except that this pin is high-voltage protected, and specified up to V_{BB} so it can be tied to the battery or power source. Not to exceed V_{BB} because the ESD structure places a diode between the ENBAT and VBB pins.

WDI Watchdog Input. Monitors the microcontroller to detect when it stops functioning. This pin is connected to an edge trigger. To avoid a fault, the latter must be triggered before CWD times-out. When not used, WDI is defeated by tying it to NPOR and shorting CWD.

CWD Watchdog timer capacitor terminal. Used with WDI. A current source charges the external capacitor tied to this pin. A reverse current source discharges the capacitor when either WDI transitions or the high Trip Voltage, $V_{TRIP(H)}$, is reached (see specification table for values). The charge-up time defines the maximum period allowed WDI to toggle before a fault is issued; the charge-down time defines the width of NPOR pulses issued to wake-up the microcontroller.

NPOR NOT Power On Reset. This active-low pin indicates a fault. Except for watchdog faults, NPOR is held low during the fault state. Refer to the Fault Logic table to determine which faults are latched. Watchdog faults generate a train of pulses to "wake up" the microcontroller.

CPOR Power-On Reset timer capacitor terminal. Whenever VREG5 first charges up (at start-up or when a fault is cleared) a "fault" condition remains in effect until the onboard current source drives CPOR to the high Trip Voltage, $V_{TRIP(H)}$. This allows external circuits, such as a microcontroller, to be initialized before activating the outputs. CPOR is defeated by pulling it high to VREG5 with a 50 kΩ resistor.

INx Input pin. Active-high CMOS input. Internally tied to 200 kΩ pull-down resistors.

OUTx Output pin. Open drain DMOS. Clamps to a voltage greater than V_{BB} when an inductive load is switched off. Includes current mirror for overcurrent protection.

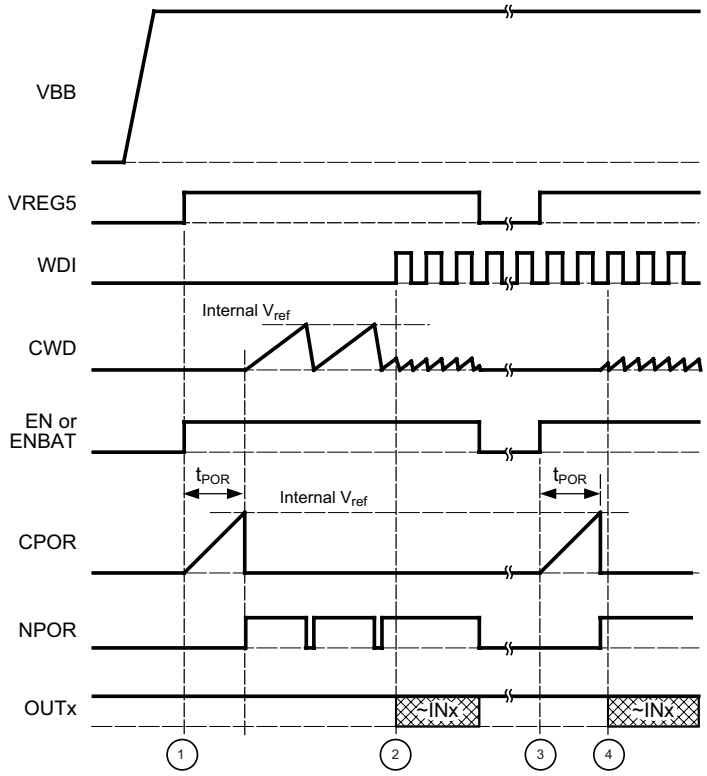
VBB Power pin, or "battery." Specified for automotive voltages.

VREG5 5 V Regulator output. Clamped at the Current Limit Level ($I_{REG5Lim}$) for excessive loads. As load resistance decreases, VREG5 is pulled below the UVLO level. In that case, a fault is generated (NPOR low).

LGND Logic Ground. The reference pin for the logic circuits. Must be connected to PGND externally.

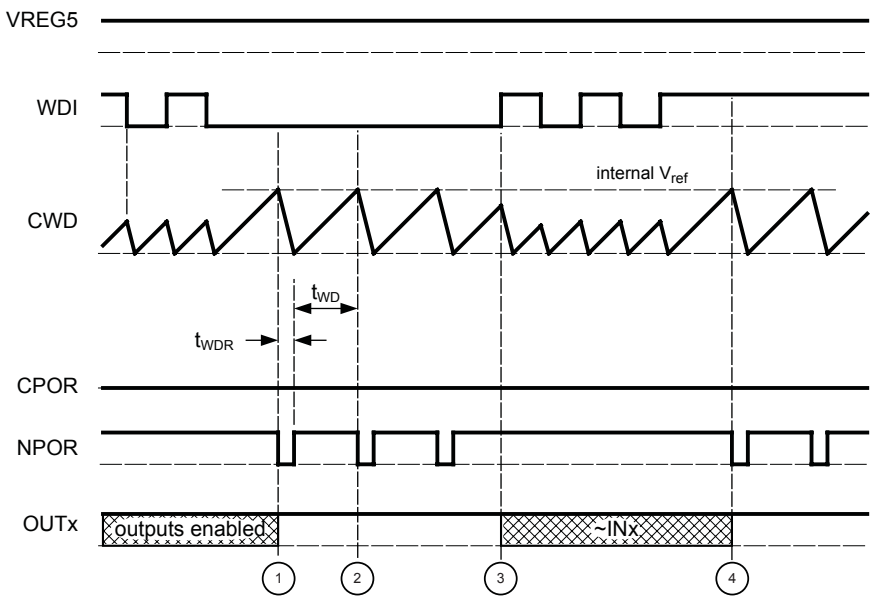
PGND Power Ground. The reference pin for the outputs (OUTx). Must be connected to LGND externally.

Timing Diagram: Initial Start-up and Exiting Sleep Mode



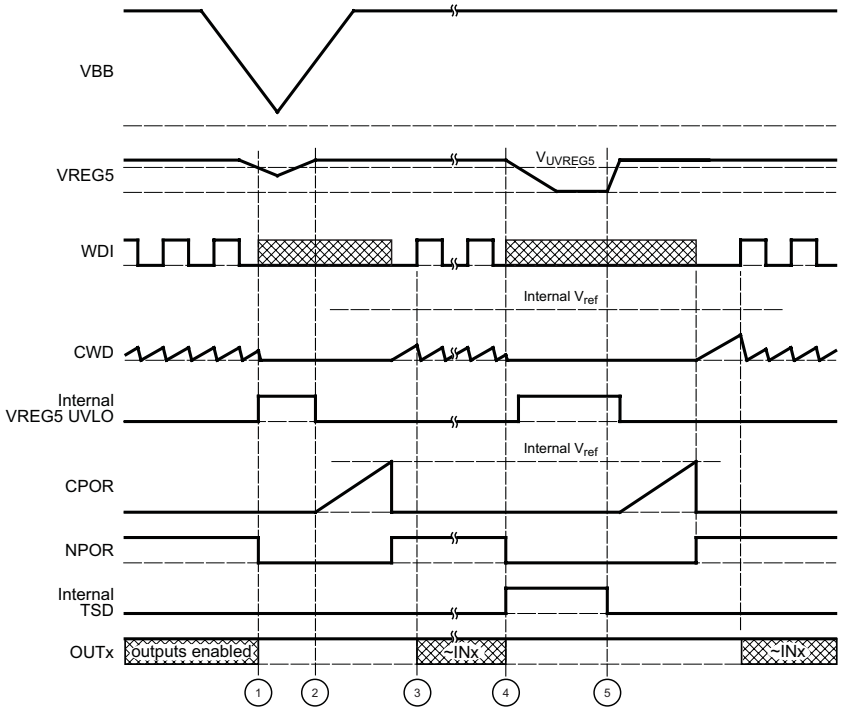
1. 5 V signal to wake up microcontroller.
2. OUTx enabled with first watchdog pulse.
3. Power ramp-up sequence with watchdog active.
4. NPOR inactive, but outputs not enabled until watchdog detected.

Timing Diagram: Watchdog Monitoring



1. Missing watchdog detected (WDI low).
2. NPOR pulses generated periodically.
3. NPOR inactive, but outputs not enabled until watchdog detected.
4. Missing watchdog detected (WDI low, steps 2 and 3 repeat).

Timing Diagram: VREG5 UVLO and TSD Monitoring



1. VREG5 undervoltage detected.
2. VREG5 recovers, and after it rises above $V_{UVREG5} + V_{UVREG5(Hys)}$, UVLO flag is deactivated and CPOR recharges.
3. NPOR inactive, but outputs not enabled until watchdog detected.
4. TSD event detected and NPOR is activated. When $V_{REG5} \leq V_{UVREG5}$, VREG5 shuts down.
5. TSD flag deactivated (VREG5 allowed to rise; steps 2 and 3 repeat)

Applications Information

Dropout Voltage

For operation with V_{BB} below the specified range of operating voltages, use the Pass Transistor On-Resistance R_{REG5} to determine the maximum allowed regulator current, $I_{REG5(max)}$. This current is limited by the difference between V_{BB} and V_{REG5}, according to the following equation:

$$I_{REG5} < \frac{V_{BB} - V_{REG5}}{R_{REG5}} \quad (1)$$

Figure 3 shows the results of this condition combined with the rated regulator current, in normal operation.

Note that, although the regulator is specified for normal operation with V_{BB} well above normal automotive voltages, in general thermal constraints will limit maximum operational V_{BB}.

Fault Logic

The A2550 offers several protection and fault detection features. The operation of thermal shutdown, watchdog monitoring of the microcontroller, and regulated voltage undervoltage lockout are described in the Timing Diagrams section. The fault logic is described in table 1.

NPOR

The following faults generate a RESET state:

- watchdog alarm
- VREG5 falls below the UVLO level

In addition, the following conditions cause a low NPOR signal *if* the NPOR pin is pulled up by VREG5 (because these conditions disable VREG5):

- overtemperature (Thermal Shut Down)
- no ENABLE signal (EN = ENBAT = 0)

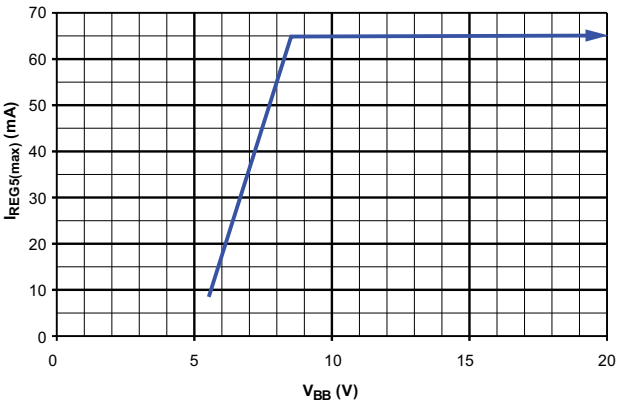


Figure 3. Current Capability of the 5 V Regulator (VREG5)

Table 1. Fault Logic[a]

Inputs					Outputs				Mode of Operation
EN OR ENBAT[b]	TSD	UVLO	Watchdog alarm	OCx	Internal 5V	VREG5	NPOR	OUTx	
1	0	0	0	0	1	1	1	INx	Normal Operation: OUTx active for INx active.
1	0	0	0	1	1	1	1	Z	OCx disables OUTx only. OUTx latched OFF until INx removed and reapplied.
1	0	0	1	X	1	1	Pulse	Z	NPOR periodically pulses to attempt RESET of microcontroller.
1	0	1	X	X	1	1	0	Z	NPOR remains active after UVLO recovers until POR delay expires.
1	1	X	X	X	1	0	0	Z	
0	X	X	X	X	0	0	Off	Z	Sleep mode. NPOR = 0 when pulled up by VREG5 because VREG5 = 0.

[a]X indicates "don't care," Z indicates high impedence.
[b]This entry is a logical OR of the EN and ENBAT pins.

Applications Information

NPOR is pulsed for a watchdog fault. For the remaining faults, NPOR is held low for the duration of the fault. After the fault condition is removed, NPOR remains low during the t_{POR} period. The latter is set by the value of the external capacitor fed by a current source at the CPOR pin, according to the following formula:

$$t_{POR} = \left(200 \frac{ms}{\mu F}\right) \times C_{POR} \quad (2)$$

The scaling factor is simply derived from the specifications using the typical value of I_{POR}:

$$\frac{t_{POR}}{C_{POR}} = \frac{V_{REF} - V_{TRIP(L)}}{I_{POR}} \quad (3)$$

Watchdog

The watchdog monitors the microcontroller to detect if it locks up. To do so, the watchdog checks for pulses on the Watchdog Input pin (WDI), and if they are absent for longer than the timeout period, t_{WD}, the watchdog activates NPOR, which pulses periodically. t_{WD} is proportional to the external capacitor fed by a current source at the CWD pin. The voltage change is 1 V, so using the typical value of I_{CWD}(charging) we have:

$$t_{WD} = \left(200 \frac{ms}{\mu F}\right) \times C_{WD} \quad (4)$$

The pulse width for NPOR active, t_{WDR}, also scales proportionally to the value of the external capacitor at the CWD pin. Using the typical value of I_{CWD}(discharging) we have:

$$t_{WDR} = \left(14 \frac{ms}{\mu F}\right) \times C_{WD} \quad (5)$$

See the specification tables for tolerances.

When not used, disable watchdog by tying WDI to NPOR and tying CWD low. Table 2 shows watchdog timing for the nominal capacitances listed.

Table 2. Timing Set by Capacitors

C (µF)	t_{POR} (ms)	t_{WD} (ms)	t_{WDR} (ms)
0.1	20	20	1
0.22	44	44	3
0.47	94	94	7
1	200	200	14

Output Overcurrent

When the OC (overcurrent) protection is triggered in a driver, that driver is disabled for self-protection. No other functions are affected; NPOR and VREG5 operate normally. A disabled output driver remains shut down until the respective INx is brought low, then high again; at which time OUTx turns on. OUTx will switch on again the next time INx is applied. If a short-to-battery still exists, the overcurrent will trip each time INx is reapplied.

Sleep

The A2550 is put to sleep by holding both EN and ENBAT low. In sleep mode all functions are shut down, including VREG5. If the VREG5 regulator is required at all times, disable sleep mode by tying ENBAT to VBB.

Power Limits

Power dissipation, P_D, is limited by thermal constraints. The maximum allowed power dissipation, $P_{D(max)}$, is found from the formula:

$$T_J = (P_{D(max)} \times R_{\theta JA} + T_A) \le T_{J(max)} \quad (6)$$

The maximum junction temperature, $T_{J(max)}$, and the thermal resistance, $R_{\theta JA}$, are given in the specification tables.

The three main contributors to power dissipation are:

- P_{BIAS} from the supply bias current
- P_{REG} from the linear regulator voltage drop
- P_{LS} from low-side driver conduction

For example, to determine if T_J is in an acceptable range, given:

$R_{\theta JA}$ = 55°C/W , and
T_A = 125°C ; and

$$P_{BIAS} = V_{BB} \times I_{BBQ} \quad (7)$$
$$= 14\ V \times 3\ mA = 42\ mW\ , \text{and}$$

$$P_{REG} = (V_{BB} - V_{REG5(min)}) \times I_{REG5} \quad (8)$$
$$= (14\ V - 4.9\ V) \times 20\ mA = 182\ mW\ , \text{and}$$

$$P_{LS} = (R_{DS(on)} \times I^2_{LS1}) + (R_{DS(on)} \times I^2_{LS2}) + (R_{DS(on)} \times I^2_{LS3}) \quad (9)$$

Because $I_{LS1} = I_{LS2} = I_{LS3} = 110$ mA, and given that $R_{DS(on)} = 5\ \Omega$, then

$$P_{LS} = 3(5\ \Omega) * (110\ \text{mA})^2 = 182\ \text{mW}.$$

Given also:

$$P_D = P_{BIAS} + P_{REG} + P_{LS} \quad (10)$$
$$= 42\ \text{mW} + 182\ \text{mW} + 182\ \text{mW} = 406\ \text{mW}.$$

T_J can be calculated by substitution into equation 6:

$$T_J = 0.406\ \text{W} \times 55°\text{C/W} + 125°\text{C} = 147°\text{C}.$$

Reverse Battery

The low-side driver outputs can withstand reverse battery when the load (R_{LOADx}) is connected to limit current. Power dissipation ($P_D = P_{LS(rvrs)}$) is limited by thermal constraints, according to the following formula:

$$P_{LS(rvrs)} = V_{F1} \times I_{F1} + V_{F2} \times I_{F2} + V_{F3} \times I_{F3}, \quad (11)$$

where:

$$I_{Fx} = \frac{V_{BB(rvrs)} - V_{Fx}}{R_{LOADx}}. \quad (12)$$

Active Clamp on Outputs

The driver section includes an active clamp that prevents an overvoltage when an inductive load is switched off. Zener diodes are connected at the output pins. This removes the need for external freewheeling diodes across inductive loads.

The coil current, I_{COIL}, is quenched by allowing the output pin voltage, V_{OUTx}, to exceed the battery voltage at the load, V_{dc}. This applies a negative voltage drop across the load. Therefore the current gradient is driven negative, as shown in the following formula:

$$\frac{dI_{COIL}}{dt} = \frac{V_{dc} - V_{OUT} - I_{COIL} \times R_{COIL}}{L_{COIL}} < 0. \quad (13)$$

The output voltage is clamped to protect the driver. The active clamp works as follows. The voltage at the driver output is pushed high by the inductive current. Once the clamp voltage, V_{CL}, is reached, a Zener diode conducts current to the internal FET gate driver block. Therefore, the FET turns partially on, in order to limit any further increase in voltage at the output pin. The output is then held at this clamp voltage until the current decays to zero, as shown in figure 4.

Energy loss in the chip, E, may be calculated as follows. Load coil resistance, R_{COIL}, is usually a significant value, but a worst case scenario takes $R_{COIL} = 0$ for simplicity. With active clamping at V_{CL}, the output current (with initial value I_{OUT0}) is driven low and the upper limit on energy loss in the driver is calculated as:

$$E_{max} = \frac{1}{2} I_{OUT0} V_{CL} \Delta t. \quad (14)$$

From figure 4:

$$\Delta t = \frac{L_{COIL} I_{OUT0}}{V_{CL} - V_{dc}}, \quad (15)$$

and

$$E_{max} = \frac{1}{2} L_{COIL} I^2_{OUT0} (1 - V_{dc}/V_{CL})^{-1}. \quad (16)$$

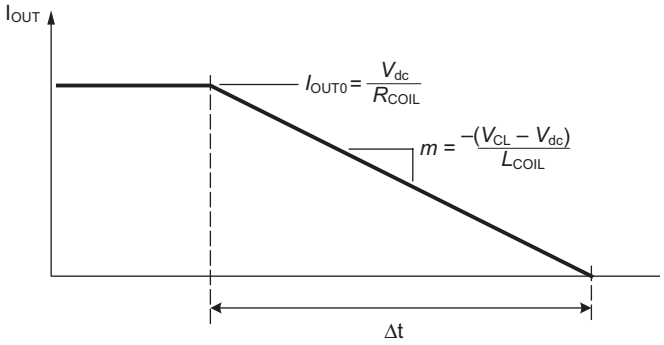


Figure 4. Output Voltage Clamping

A more rigorous derivation, including R_{COIL} during the exponential current decay results in:

$$i(t) = \frac{V_{dc}}{R_{COIL}} - \frac{V_{CL}}{R_{COIL}} \left[1 - \exp\left(-t \frac{R_{COIL}}{L_{COIL}}\right)\right] , \quad (17)$$

and

$$\Delta t = \frac{L_{COIL}}{R_{COIL}} \ln\left(1 - V_{dc} / V_{CL}\right)^{-1} . \quad (18)$$

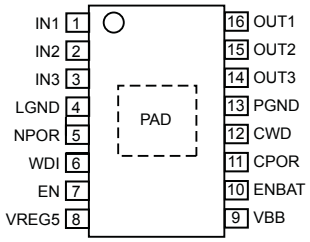
Energy loss in the driver is:

$$E = \frac{V_{CL}\, V_{DC}\, L_{COIL}}{R_{COIL}^2} [1 + (V_{CL} / V_{dc} - 1) \ln\,(1 - V_{dc} / V_{CL})] . \quad (19)$$

Capacitive Loads

When capacitive loads are applied to the outputs, the constraint described below applies. Such is the case, for example, when capacitors are attached to the outputs to protect against ESD. Larger capacitors protect against larger ESD voltages. However, the upper limit on capacitance is determined by the blanking time. The latter allows for spurious current spikes and capacitor discharges to be completed before the overcurrent detection circuit senses the output current (see t_{BLANK} in the Electrical Characteristics table). The blanking time allows a 47 nF capacitor with 20% tolerance and nominal 12 V automotive voltages.

Pin-out Diagram



Terminal List Table

No.	Name	Description
1	IN1	Activate driver 1
2	IN2	Activate driver 2
3	IN3	Activate driver 3
4	LGND	Logic ground; must be connected to PGND externally
5	NPOR	Not Power-On Reset
6	WDI	WatchDog Input
7	EN	Enable (low voltage)
8	VREG5	5V regulator
9	VBB	Supply voltage
10	ENBAT	Enable (high voltage)
11	CPOR	Capacitor terminal for Power-On Reset cycle time
12	CWD	Capacitor terminal for WatchDog timing
13	PGND	Power ground; must be connected to LGND externally
14	OUT3	Low side driver 3
15	OUT2	Low side driver 2
16	OUT1	Low side driver 1
–	PAD	Exposed pad for enhanced thermal performance

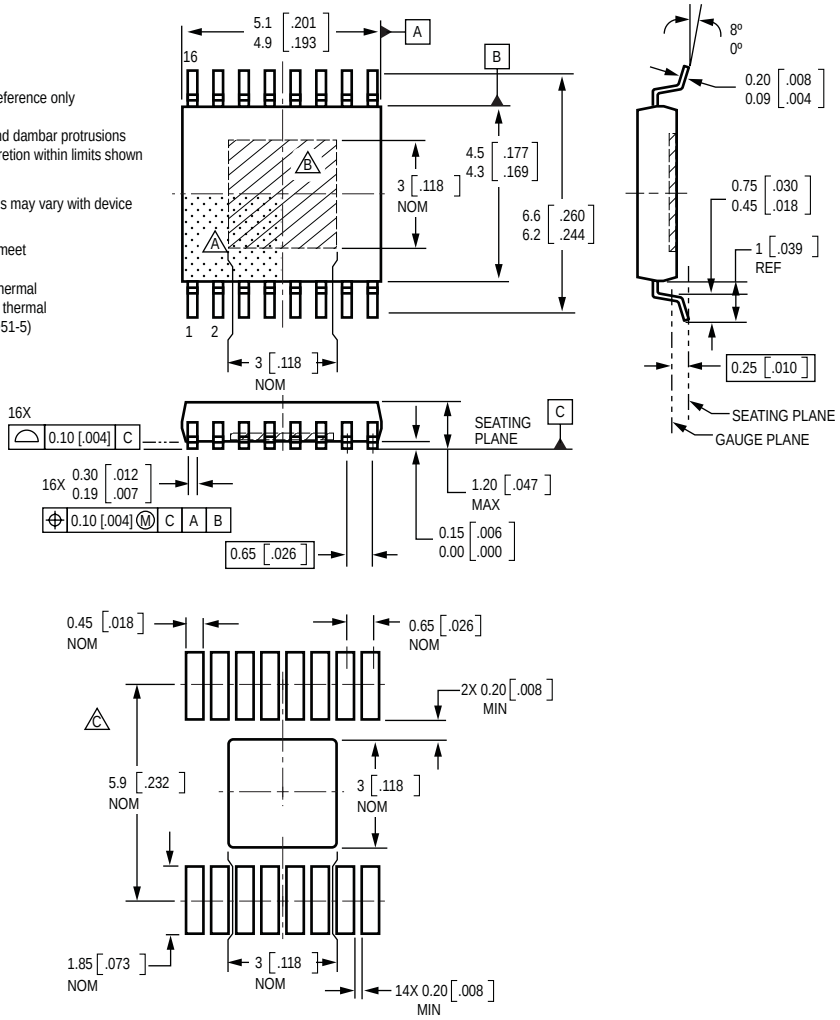
16-Pin TSSOP (Suffix LP) with Exposed Pad

All dimensions reference only, not for tooling use
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
(reference JEDEC MO-153 ABT)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-17M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)



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