Final data

SPI07N60S5
SPP07N60S5, SPB07N60S5

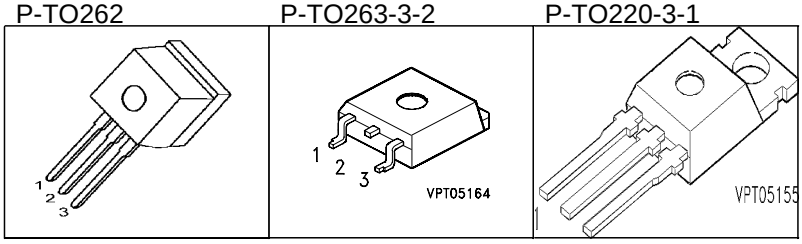
Cool MOS™ Power Transistor

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- Optimized capacitances
- Improved noise immunity

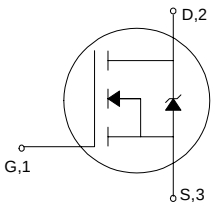
Product Summary

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	0.6	Ω
I_D	7.3	A

P-TO262 P-TO263-3-2 P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP07N60S5	P-TO220-3-1	Q67040-S4172	07N60S5
SPB07N60S5	P-TO263-3-2	Q67040-S4185	07N60S5
SPI07N60S5	P-TO262	Q67040-S4328	07N60S5



Maximum Ratings, at T_C = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D		A
T_C=25°C		7.3	
T_C=100°C		4.6	
Pulsed drain current [1]	$I_{D\ puls}$	14.6	
T_C=25°C			
Avalanche energy, single pulse	E_{AS}	230	mJ
I_D = 5.5 A, V_{DD} = 50 V			
Avalanche energy (repetitive, limited by T_{jmax})	E_{AR}	0.5	
I_D = 7.3 A , V_{DD} = 50 V			
Avalanche current (repetitive, limited by T_{jmax})	I_{AR}	7.3	A
Reverse diode d*v*/d*t*	d*v*/d*t*	6	kV/µs
I_S=7.3A, V_{DS}<V_{DSS}, d*i*/d*t*=100A/µs, T_{jmax}=150°C			
Gate source voltage	V_{GS}	±20	V
Power dissipation	P_{tot}	83	W
T_C=25°C			
Operating and storage temperature	T_j , T_{stg}	-55... +150	°C

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	-	-	62	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm^2 cooling area [2)]		-	35	-	

Static Characteristics, at T_j = 25 °C, unless otherwise specified

Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 350 µA, T_j = 25 °C	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, V_{DS}=V_{DSS}	I_{DSS}				µA
V_{GS} = 0 V, T_j = 25 °C		-	0.5	1	
V_{GS} = 0 V, T_j = 150 °C		-	-	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	-	100	nA
Drain-source on-state resistance V_{GS} = 10 V, I_D = 4.6 A	$R_{DS(on)}$	-	0.54	0.6	Ω

[1] current limited by T_{jmax}

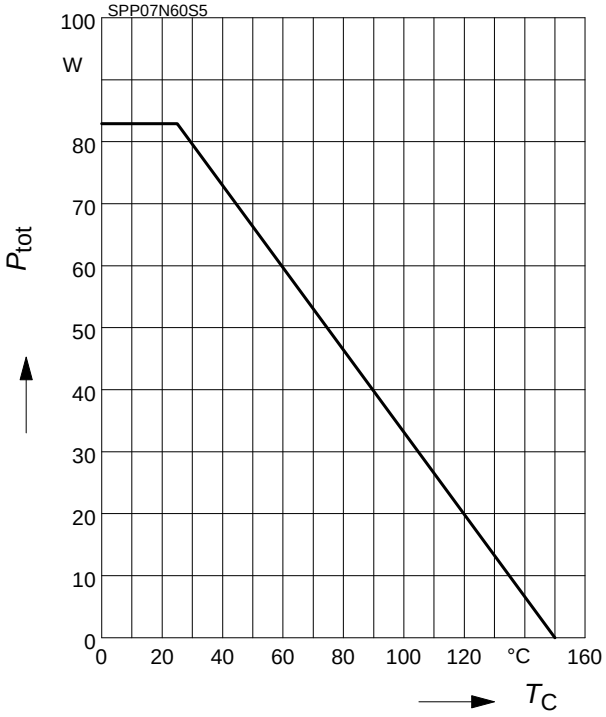
[2] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6 cm^2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=4.6A	-	4	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	970	-	pF
Output capacitance	C_{oss}		-	370	-	
Reverse transfer capacitance	C_{rss}		-	10	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=350V, V_{GS}=10V, I_D=7.3A, R_G=12Ω	-	120	-	ns
Rise time	t_r		-	40	-	
Turn-off delay time	$t_{d(off)}$		-	170	255	
Fall time	t_f		-	20	30	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=350V, I_D=7.3A	-	7.5	-	nC
Gate to drain charge	Q_{gd}		-	16.5	-	
Total gate charge	Q_g	V_{DD}=350V, I_D=7.3A, V_{GS}=0 to 10V	-	27	35	
Reverse Diode						
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	7.3	A
Inverse diode direct current,pulsed	I_{SM}		-	-	14.6	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=7.3A	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=350V, I_F=I_S, di_F/dt=100A/µs	-	750	1275	ns
Reverse recovery charge	Q_{rr}		-	4.9	-	µC

Power dissipation

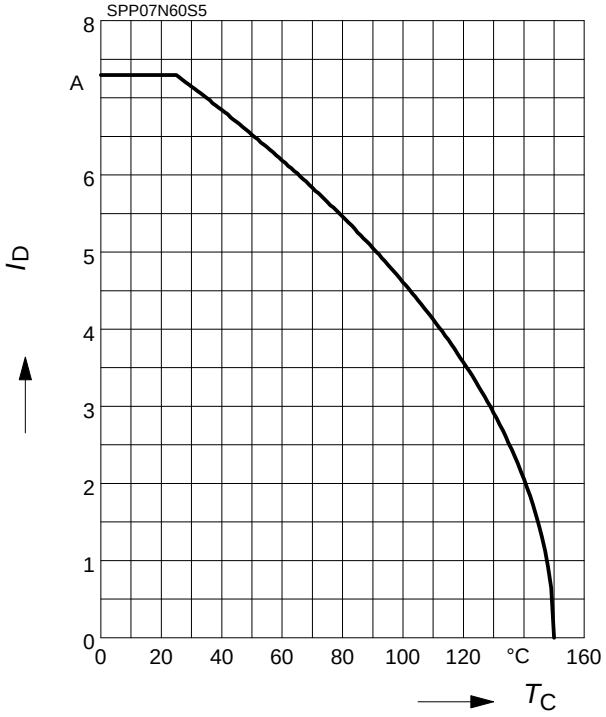
$P_{tot} = f(T_C)$



Drain current

$I_D = f(T_C)$

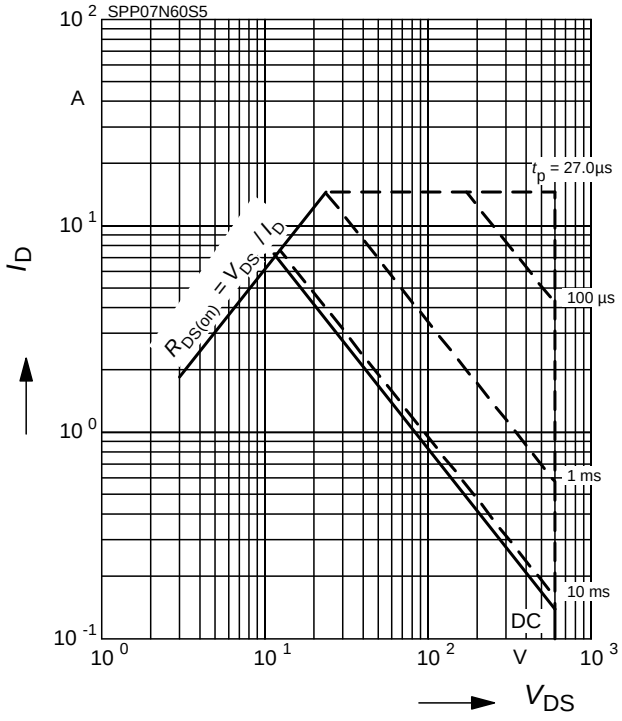
parameter: $V_{GS} \geq 10$ V



Safe operating area

$I_D = f(V_{DS})$

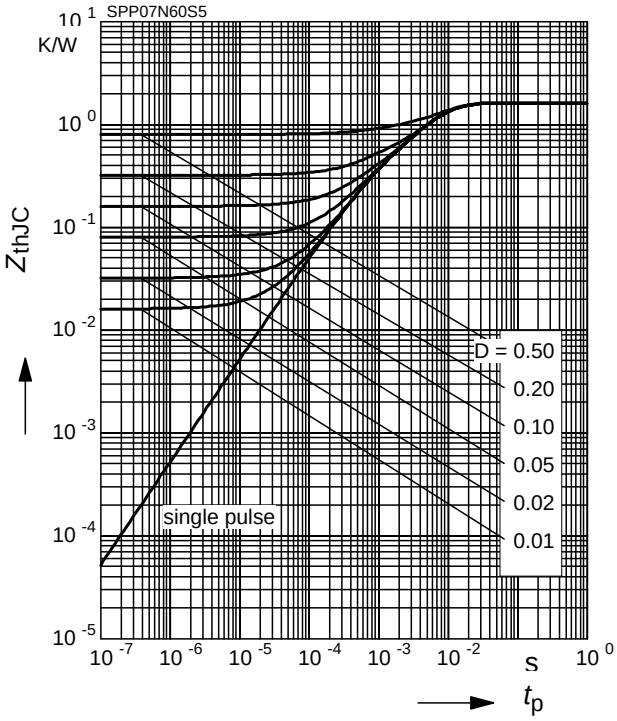
parameter: D=0.01, T_C=25°C



Transient thermal impedance

$Z_{thJC} = f(t_p)$

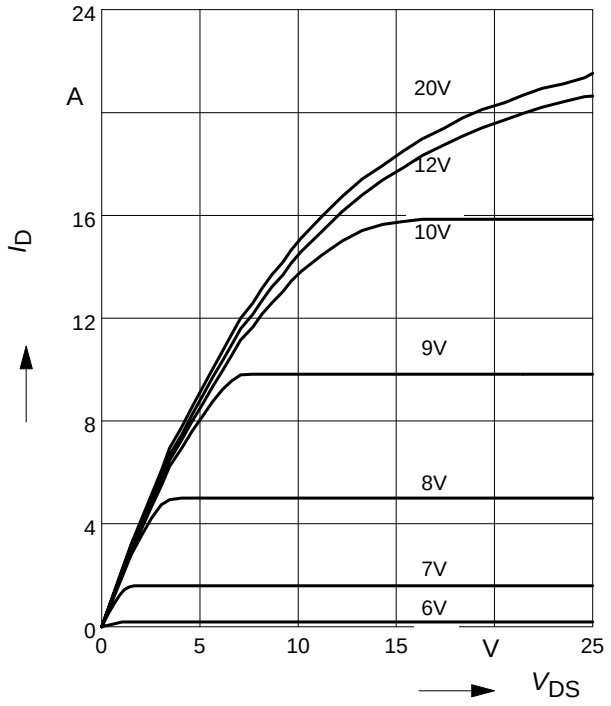
parameter : $D = t_p/T$



Typ. output characteristic

I_D = f (V_{DS})

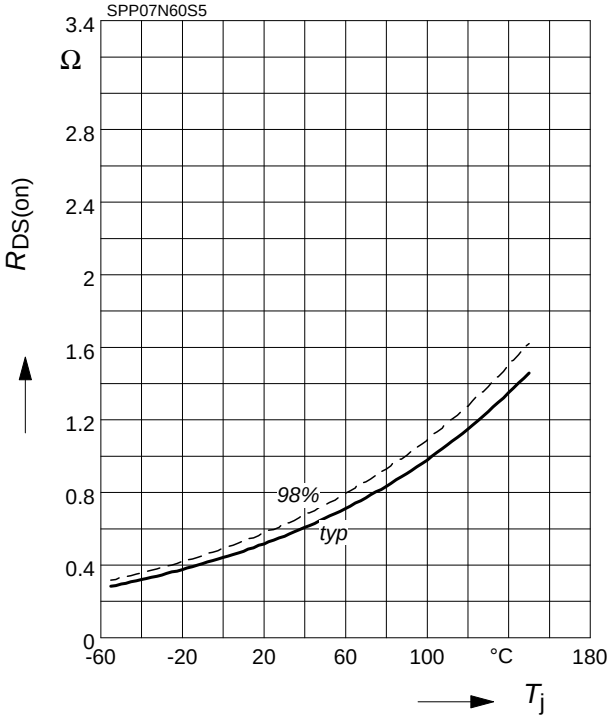
Parameter: V_{GS}, T_j = 25 °C



Drain-source on-resistance

$R_{DS(on)}$ = f (T_j)

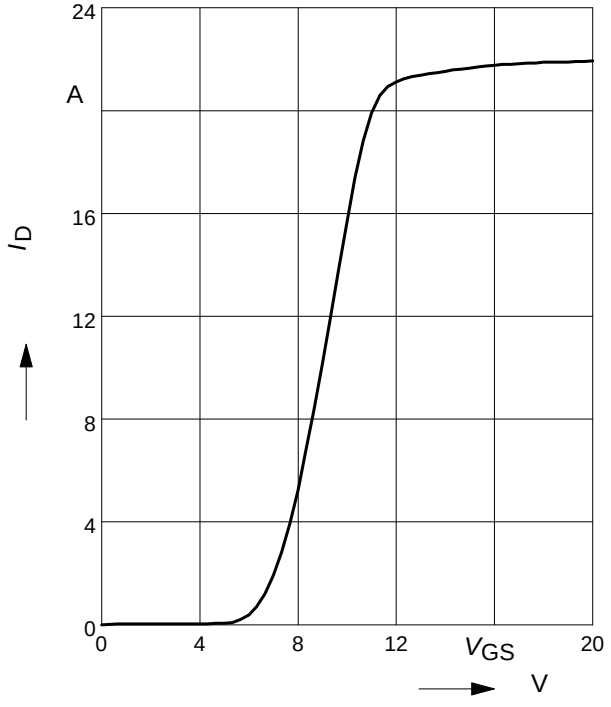
parameter : I_D = 4.6 A, V_{GS} = 10 V



Typ. transfer characteristics

I_D= f (V_{GS})

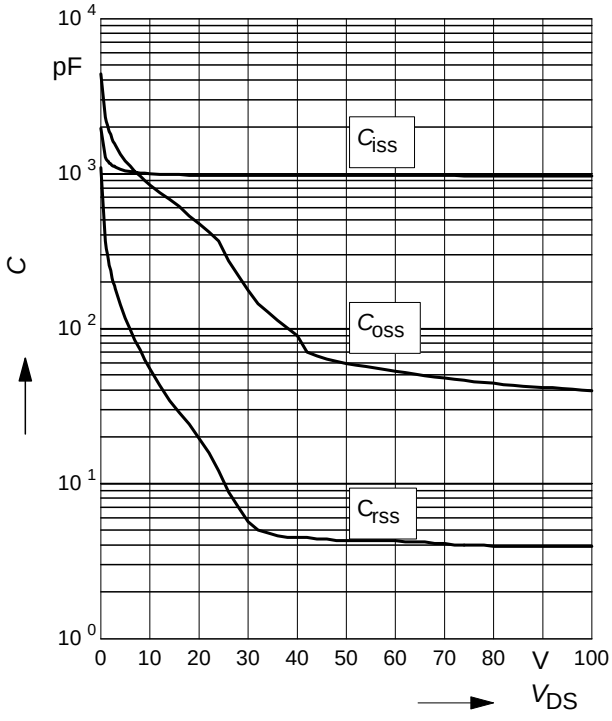
V_{DS}≥ 2 x I_D x $R_{DS(on)max}$



Typ. capacitances

C = f (V_{DS})

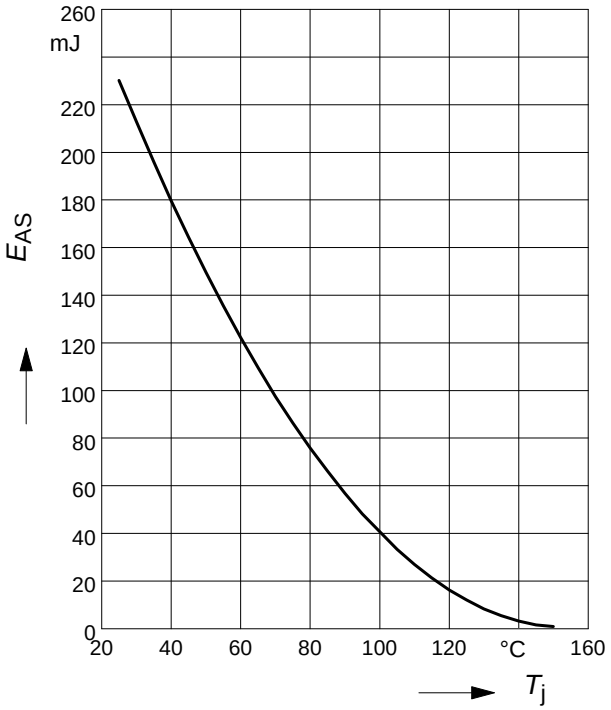
parameter: V_{GS}=0 V, f=1 MHz



Avalanche energy

$E_{AS} = f(T_j)$

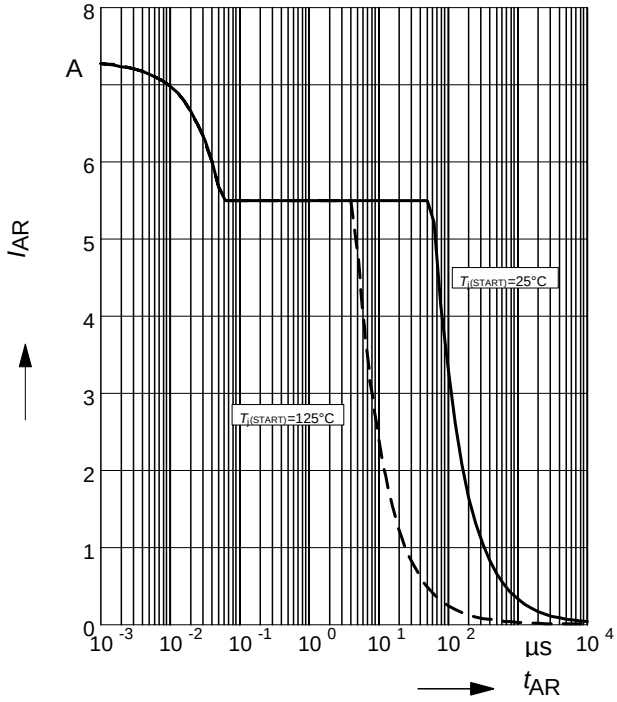
par.: I_D=5.5A, V_{DD}=50V



Avalanche SOA

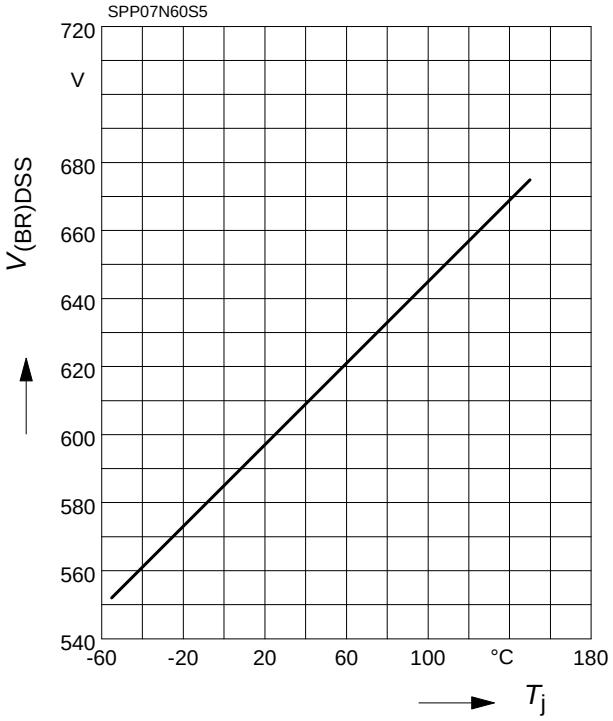
$I_{AR} = f(t_{AR})$

par.: $T_j \leq 150$ °C



Drain-source breakdown voltage

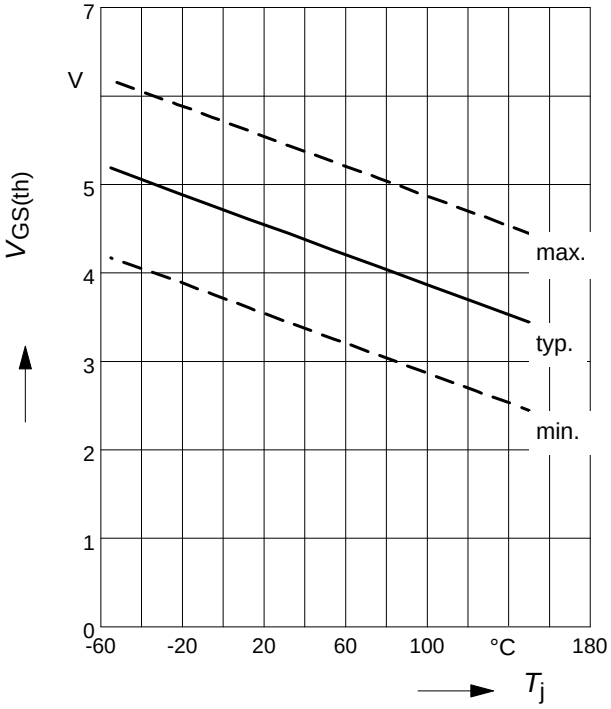
$V_{(BR)DSS} = f(T_j)$



Gate threshold voltage

$V_{GS(th)} = f(T_j)$

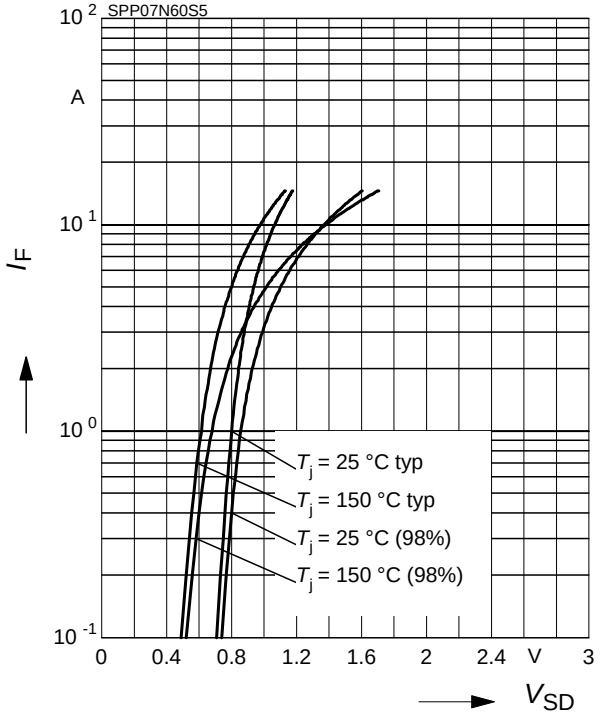
parameter: $V_{GS} = V_{DS}$, I_D = 350 µA



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

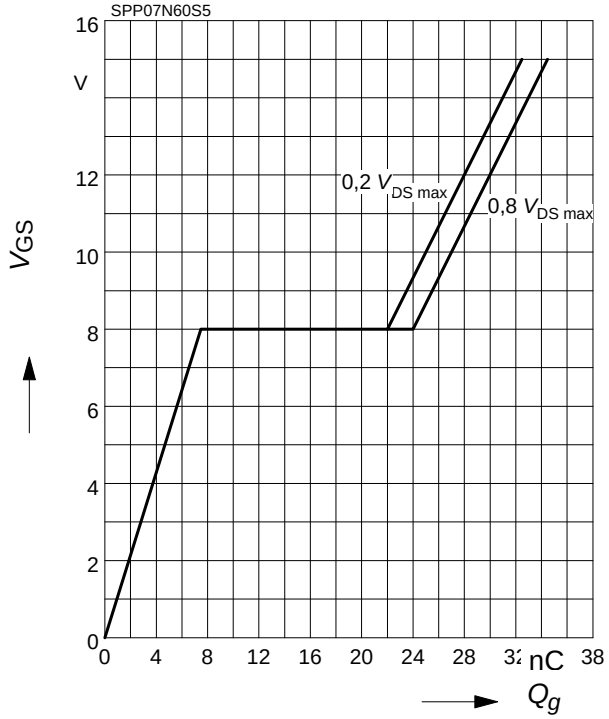
parameter: T_j , tp = 10 µs



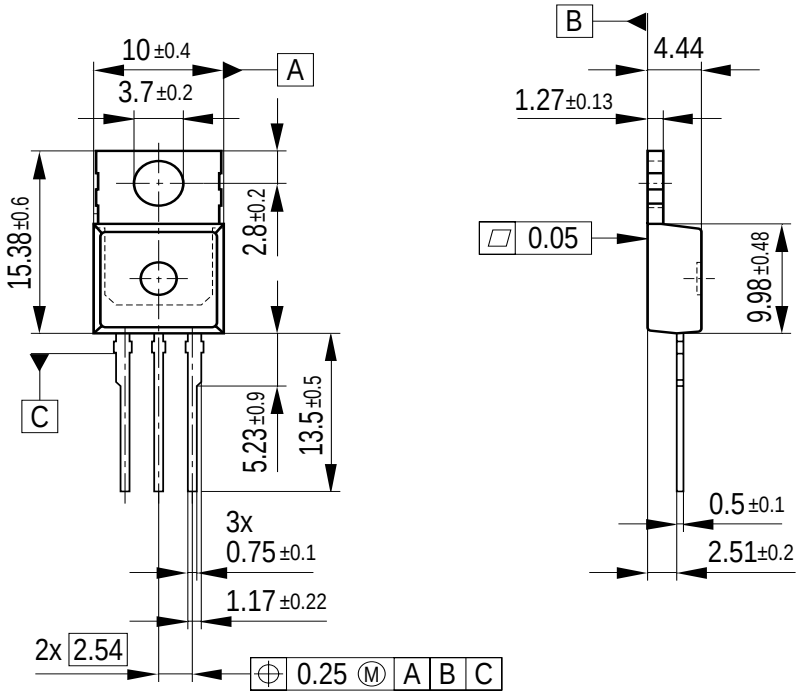
Typ. gate charge

$V_{GS} = f\ (Q_{Gate})$

parameter: I_D = 7.3 A pulsed

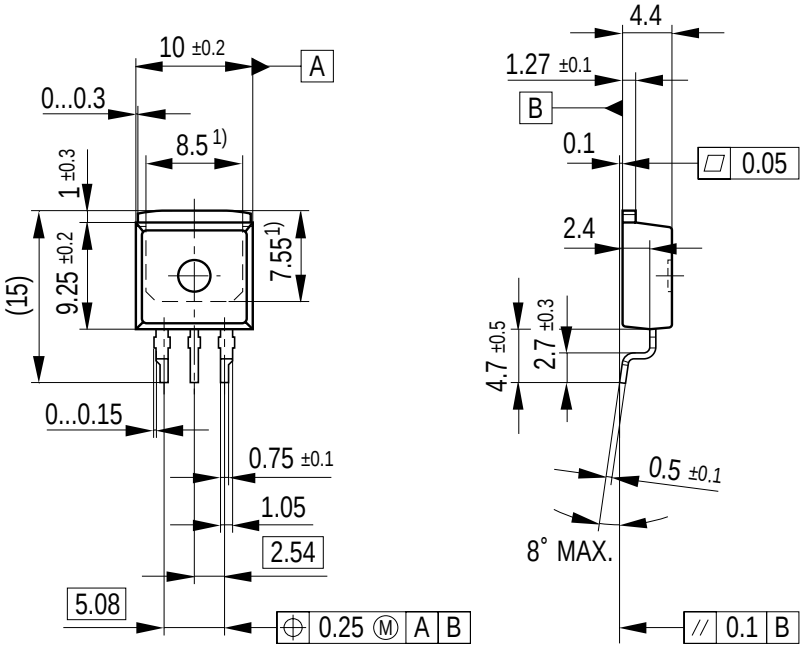


P-TO-220-3-1



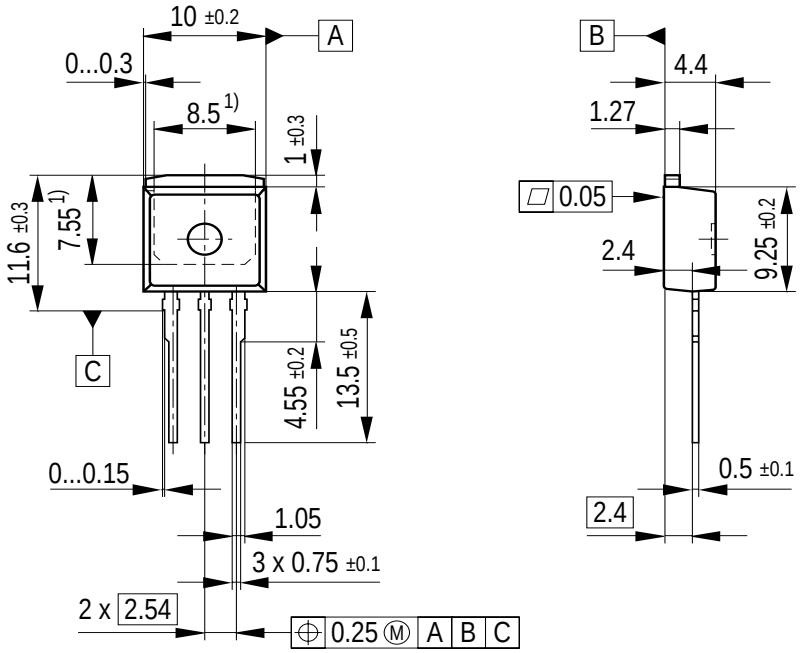
All metal surfaces tin plated, except area of cut.
Metal surface min. x=7.25, y=12.3

P-TO-263-3-1 (D^2-PAK)



1) Typical
All metal surfaces: tin plated, except area of cut.
Metal surface min. x=7.25, y=6.9

P-TO-262-3-1 (I^2-PAK)



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

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