

Digital Attenuator
31.0 dB, 5-Bit, TTL Driver, DC-2.0 GHz

**MAATCC0007
V3**

Features

- Attenuation: 1.0 dB Steps to 31 dB
- Low DC Power Consumption
- Plastic SOW, Wide Body, SMT Package
- Integral TTL Driver
- 50 ohm Impedance
- Test Boards are Available
- Tape and Reel Packaging Available
- Lead-Free SOW-16 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free "Green" Mold Compound
- 260°C Reflow Compatible
- RoHS* Compliant Version of AT65-0263

Description

M/A-COM's MAATCC0007 is a GaAs FET 5-bit digital attenuator with integral TTL driver. Step size is 1.0 dB providing 31 dB total attenuation range. This device is in a SOW-16 plastic surface mount package. The MAATCC0007 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

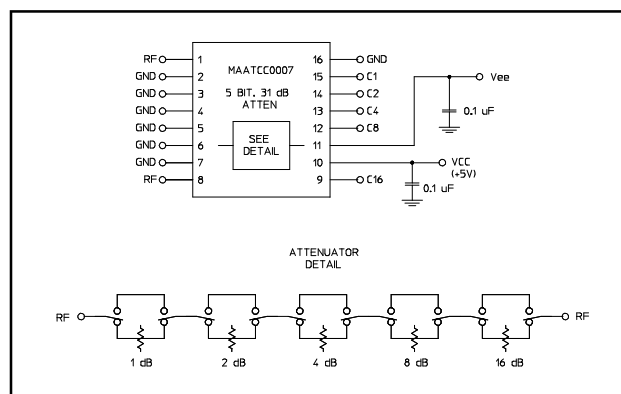
Ordering Information

Part Number	Package
MAATCC0007	Bulk Packaging
MAATCC0007TR	1000 piece reel
MAATCC0007-TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

Note: Die quantity varies.

Schematic with Off-Chip Components



Pin Configuration

Pin No.	Function	Pin No.	Function
1	RF	9	C16
2	GND	10	Vcc
3	GND	11	Vee
4	GND	12	C8
5	GND	13	C4
6	GND	14	C2
7	GND	15	C1
8	RF	16	GND

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC-2.0 GHz	dB	—	2.8	3.2
Attenuation Accuracy	Individual Bits 1-2-4-8-16	DC-2.0 GHz	dB	—	—	$\pm(.5 + 5\% \text{ of atten setting})$
	Any Combination of bits 3 - 29 dB	DC-2.0 GHz	dB	—	—	$\pm(.5 + 5\% \text{ of atten setting})$
	Any Combination of bits 30 - 31 dB	DC-2.0 GHz	dB	—	—	$\pm(.7 + 7\% \text{ of atten setting})$
VSWR	Full Range	DC-2.0 GHz	Ratio	—	1.5:1	1.8:1
Switching Speed	50% Cntl to 90%/10% RF	—	nS	—	75	150
	10% to 90% or 90% to 10%	—	nS	—	20	50
1 dB Compression	—	50 MHz	dBm	—	+21	—
	—	0.5-2.0 GHz	dBm	—	+24	—
Input IP_3	Two-tone inputs up to +5 dBm	50 MHz	dB	—	+35	—
		0.5-2.0 GHz	dB	—	+48	—
V_{CC}^1	—	—	V	4.75	5.0	5.25
V_{EE}^1	—	—	V	-8.0	-5.0	-4.75
V_{IL} V_{IH}	LOW-level input voltage	—	V	0.0	—	0.8
	HIGH-level input voltage	—	V	2.0	—	5.0
lin (Input Leakage Current)	$V_{in} = V_{CC}$ or GND	—	μA	-1.0	—	1.0
I_{CC} (Quiescent Supply Current)	$V_{cntrl} = V_{CC}$ or GND	—	μA	—	250	400
ΔI_{CC}^2 (Additional Supply Current Per TTL Input Pin)	$V_{CC} = \text{Max}$, $V_{cntrl} = V_{CC} - 2.1 \text{ V}$	—	mA	—	—	1.0
I_{EE}	V_{EE} min to max, $V_{in} = V_{IL}$ or V_{IH}	—	mA	-1.0	-0.2	—
Thermal Resistance θ_{JA}	PCB mount on FR4 material, copper trace, still air at +25°C	—	$^\circ\text{C/W}$	—	90-130	—

1. Decoupling capacitors (.1 μF) are required on power supply lines.

2. For calculating ΔI_{CC} , the number of TTL input pins is 6.

Absolute Maximum Ratings^{3,4}

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 2.0 GHz	+27 dBm +34 dBm
V_{CC}	$-0.5\text{V} \leq V_{CC} \leq +7.0\text{V}$
V_{EE}	$-8.5\text{V} \leq V_{EE} \leq +0.5\text{V}$
$V_{CC} - V_{EE}$	$-0.5\text{V} \leq V_{CC} - V_{EE} \leq 14.5\text{V}$
V_{in}^5	$-0.5\text{V} \leq V_{in} \leq V_{CC} + 0.5\text{V}$
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

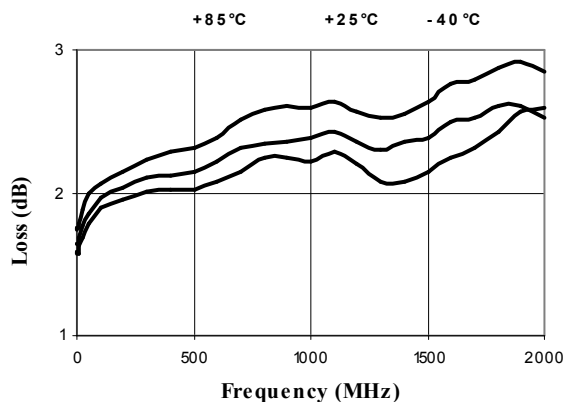
Truth Table (Digital Attenuator)

C16	C8	C4	C2	C1	Attenuation
0	0	0	0	0	Loss, Reference
0	0	0	0	1	1.0 dB
0	0	0	1	0	2.0 dB
0	0	1	0	0	4.0 dB
0	1	0	0	0	8.0 dB
1	0	0	0	0	16.0 dB
1	1	1	1	1	31.0 dB

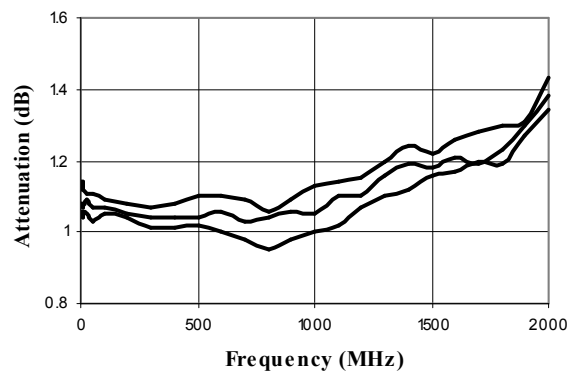
0 = TTL Low; 1 = TTL High

Typical Performance Curves

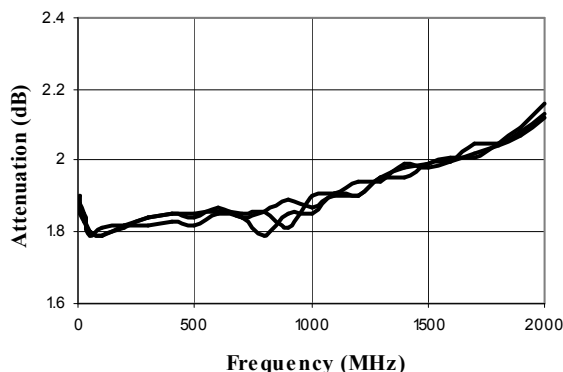
Insertion Loss @ R, H & C



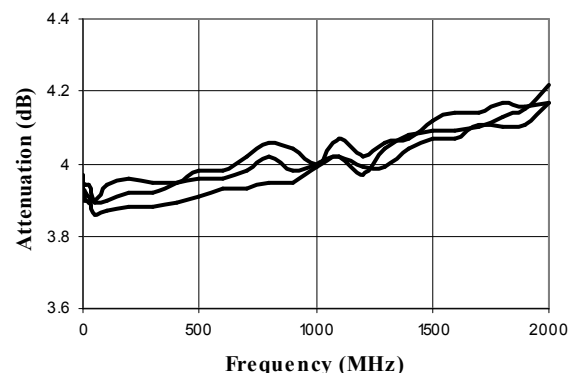
1 dB Bit @ R, H & C



2 dB Bit @ R, H & C



4 dB Bit @ R, H & C

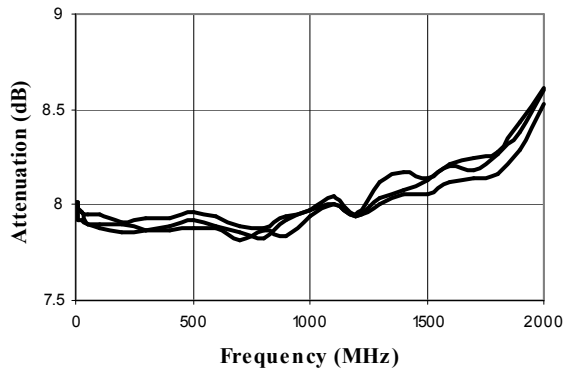


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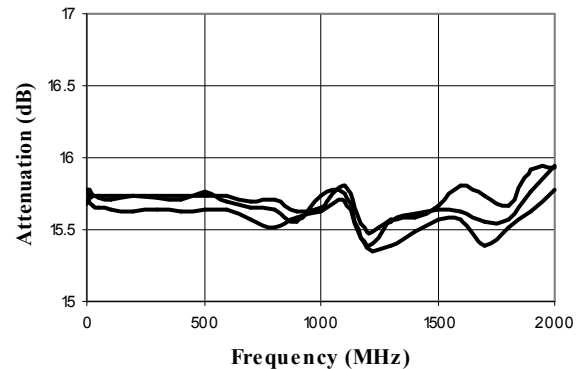
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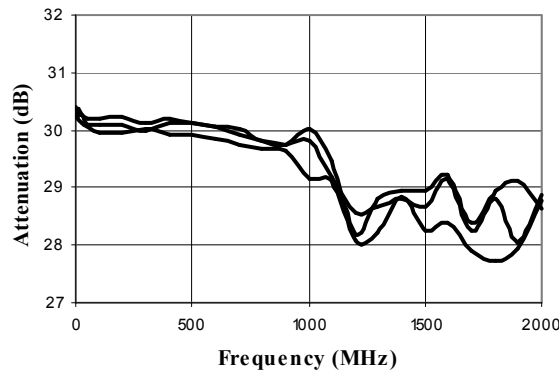
8 dB Bit @ R, H & C



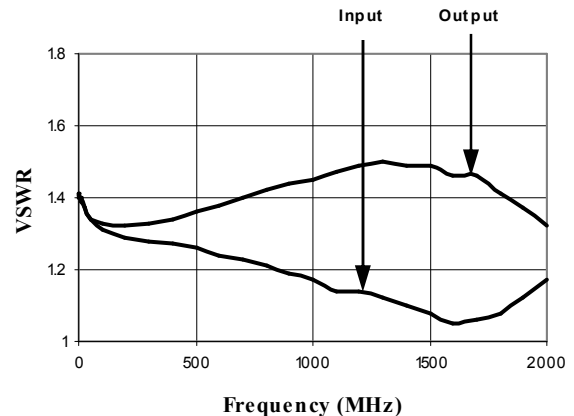
16 dB Bit @ R, H & C



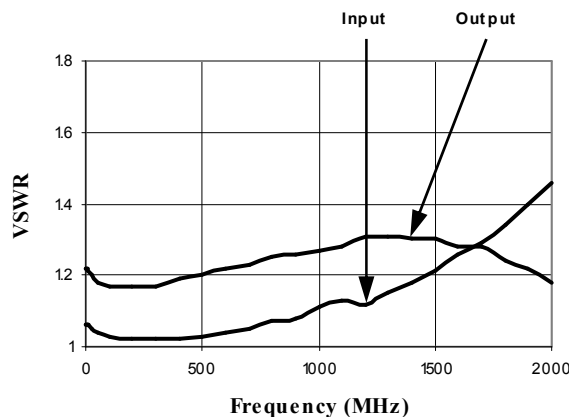
Max Attenuation @ R, H & C



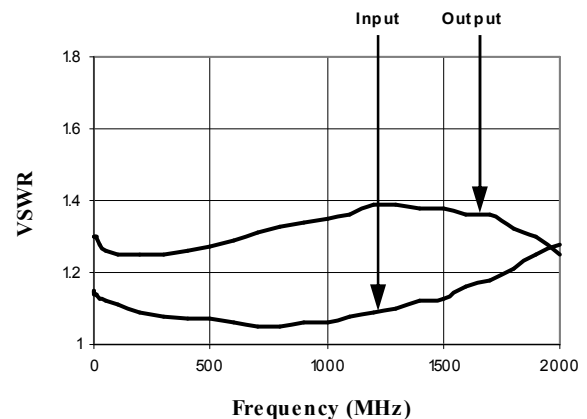
Maximum VSWR over Temp, Loss



Maximum VSWR over Temp, 1 dB Bit



Maximum VSWR over Temp, 2 dB Bit

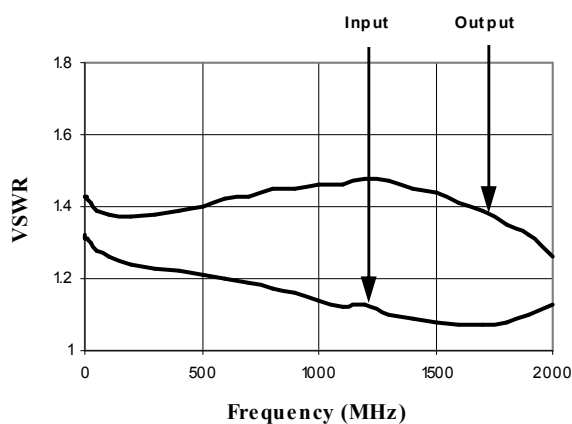


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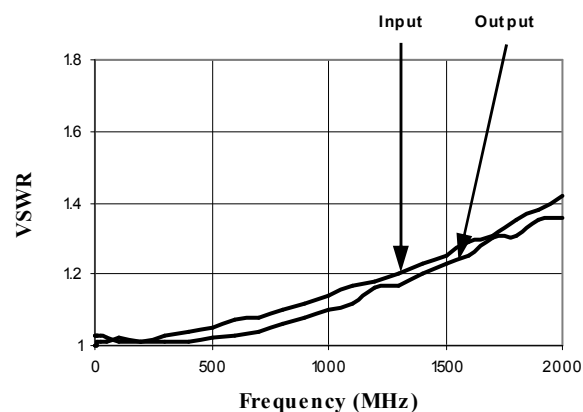
MAATCC0007
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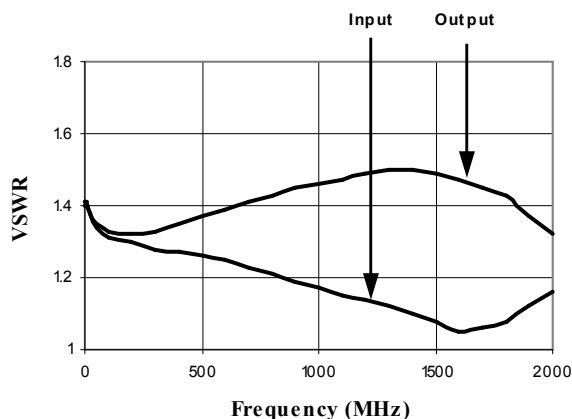
Maximum VSWR over Temp, 4 dB Bit



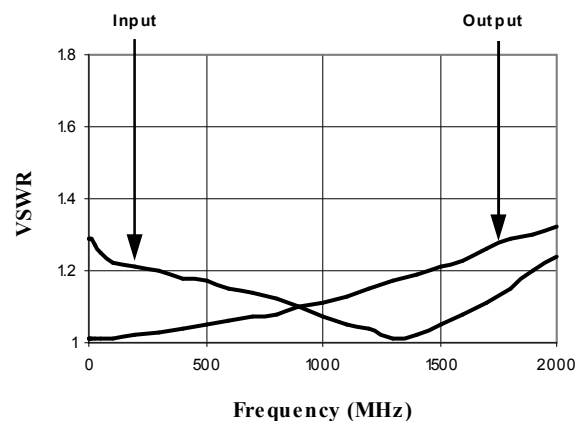
Maximum VSWR over Temp, 8 dB Bit



Maximum VSWR over Temp, 16 dB Bit



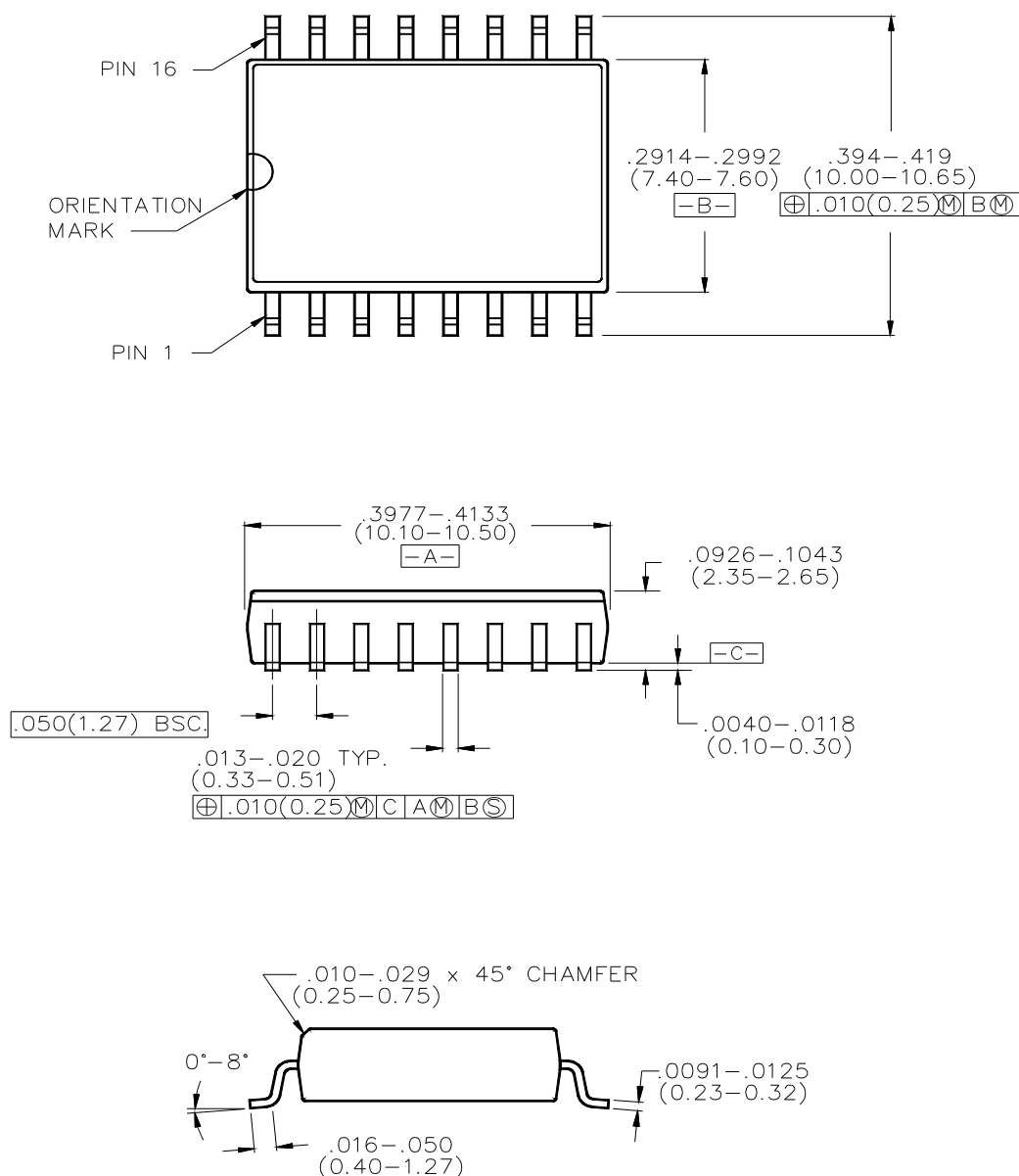
Maximum VSWR over Temp, Max Attenuation



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Lead-Free, SOW-16†



Package outline conforms to JEDEC standard MS-013AA.

† Reference Application Note M538 for lead-free solder reflow recommendations.